VHDL Polynomial

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

VHDL Polynomial
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Goals

- Implement a module with a known algorithm in VHDL.
- Implement a sequential module.
- Develop a test bench for the module.

Setup

A template code is provided on the GitHub System in the repository:

```
polynomial.vdhl
```

Please clone this repository to a working directory. You will find template code for this task there.

The folder contains the following files:

- `poly.vhd` contains the polynomial evaluation module.
- `poly_tb.vhd` contains the testbench for the module.

Task Description

1) Provide a fully functional module in `poly.vhd` that calculates the value of a polynomial $f(x) = \sum_{i=0}^{n}(a_i * x^i)$ with a fixed degree and fixed coefficients a_i and variable x-coordinate. Use Integer types for calculating the result.

2) Develop a test bench in `poly_tb.vhd` that verifies the correctness of the module you implemented in 1).
   a. Implement an algorithm that reliably calculates the correct result.
   b. Use the specified protocol to create test stimuli for the module.
   c. Retrieve the results from the module and compare them to the correct result.

3) Simulate the design with the Vivado Design Suite and make sure it runs correctly.
4) Run synthesis and implementation and check the reports. Check if the generates design corresponds to your intended architecture.

Questions

- What are the main differences between VHDL and SystemC?
- How are sequential designs described in VHDL?
- How is reliable communication implemented in VHDL?