A Multi-Channel Discriminator IC

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I**ntroduction**

This paper attempts to describe a preliminary design for a multi-channel discriminator chip. The integrated circuit (IC) will be called DISC16C, short for discriminator chip - 16 channels. Discriminators are widely used in radiation monitoring systems. The purpose of a discriminator is to mark the arrival time of an input pulse. Ideally, the discriminator's output logic signal, marking the arrival of the input pulse, should be independent of pulse amplitude and risetime.

In reality, variations in the firing time of a discriminator generally fall into two categories: time walk, tw, and time jitter, at. The term time ’’walk” is used to describe systematic variation in the rising edge of the discriminator output signal as a function of pulse height and time ’jitter” describes random variation in the rising edge of the output signal due to electronic noise in the system.

D**esign** S**pecifications**

* Support 16 detectors.
* Must support pulses of both polarities.
* Must accommodate signals with risetime constants ranging from 3 nsec to 100 nsec.
* Should exhibit excellent walk and jitter characteristics for input pulse amplitudes ranging from 20 mV to 2 V.
* Must accommodate pulse repetition rates up to 1 KHz.
* The discriminator in each of the 16 channels should be of the constant fraction type (CFD). In CFD discriminators an attenuated version of the input is subtracted from a delayed version of input waveform and the time at which the difference between the two is equal to zero is used to mark the pulse arrival time. This results in output timing signals independent of pulse amplitude.
* Each channel should have a leading-edge threshold. The threshold is programmed using a 4-bit digital value.
* While the chip must support signals with risetime constants ranging from 3 nsec to 100 nsec, performance will be optimized for the shorter time constants.
* The output pulse width from a channel will be programmable (through an external analog control voltage) in the range of 10 nsec to 100 nsec.
* The analog supply voltage for the IC will be 5 Volts while all digital signals entering and leaving the IC will obey a 3.3 Volt standard.
* Power consumption of the 16 channel IC should not exceed 450 mW i.e. 20 mW per channel with 50 mW budgeted for the circuits common to all channels.
* The IC is expected to occupy an area of aprpoximately 4 mm x 3 mm. The chip will be packaged in a 64-pin plastic package. A ground pin be be placed between the 16 analog input pins in order to reduce crosstalk.
* The chip is to be fabricated in the ON Semiconductor, 0.5 micron CMOS process. The targeted process supports two poly and 3 metal layers. A high resistance poly layer is available.

S**ystem** L**evel** D**esign** D**escription**

The design presented herein is similar to the discriminator circuit currently being used in our group’s HINP4 IC which in turn is based on a design described in [1]. The design presented in [1] describes a design carried out in 1.2 micron CMOS and boasts timing walk for 5 ns risetime signals over the dynamic range from 20 mV to 2 V of less than ± 150 ps. The reported jitter was 10 ps with an input level of 20 mV.

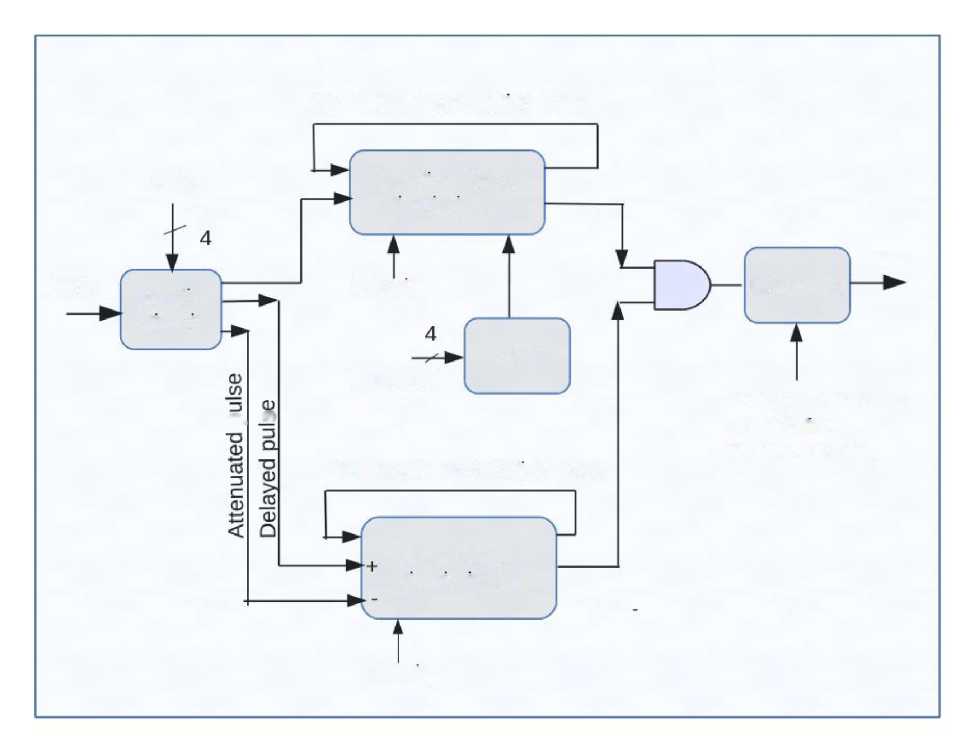
A block diagram depicting a single channel of our proposed multi-channel discriminator IC is presented in Fig. 1. The leading edge discriminator circuit shown in the figure consists of a cascade of 2 or 3 very high bandwidth (but relatively low gain) differential amplifiers. A ’’slow” DC offset cancellation loop drives the input referred offset for the cascaded amplifier to the sub- mV level. The amplified (offset-free) output is then compared with a programmable threshold using a continuous-time comparator. The output from the leading edge circuit qualifies the output from the zero-cross circuit. The leading edge comparator transitions first followed by the firing of the zero-cross discriminator, thereby accurately marking input pulse arrival time.

The Nowlin circuit is shown in greater detail in Fig. 2. The capacitor C0 in the Nowlin cicuit along with the series resistance of R1 and R2 implement a ”fast” shaper. The output of this highpass filter is applied to the leading edge discriminator. Also, a fraction, ( rR+2r ), of the ”fast” shaper output is applied to the inverting input of the zero-cross discriminator circuit along with a delayed version of the input pulse connected to the non-inverting input. It is well-known that the time at which the differential voltage crosses through zero is independent of the input pulse amplitude.

It is important that the slope (which we shall refer to as the ”slew rate” or SR) of the differential signal when crossing through zero be maximized. A delay (determined by the time constant R3 ■ C1) which when very short will produce maximum SR but at the expense of underdrive voltage. In Fig. 3 the input pulse risetime constant is 3 ns (in other words, a 10 - 90 % rise time of 6.6 ns). When the time constant in the Nowlin circuit is 300 ps, the SR is high but the underdrive is quite small. The underdrive must be sufficiently large so as to drive the comparator output to the logic false state. Remember, that Fig. 3 remains essentially unchanged when the peak pulse amplitude is reduced to 20 mV except all amplitudes are 1 % of the values shown in the figure. When the time constant in the Nowlin circuit is 6 ns, the underdrive voltage is high but the SR suffers. Clearly, when the time constant is 1.5 ns, a good compromise between SR and underdrive voltage is achieved. In the proposed design, capacitor C1 and/or resistor R3 will be programmable. In this way, the delay can be matched to the risetime of the input pulse and we can accommodate a wide range of input rise time constants.

The zero-cross circuit is constructed by cacading N differential amplifier stages (N « 6) each

**DC Offset Cancellation Loop**



**Leading Edge**

**Delay**

**Discriminator**

HIT

**Pulse**

**Nowlin**

**Circuit**

Q\_ W

**Polarity**

**Threshold**

**One-Shot**

**DAC**

**Voltage Controlled**

**Pulse Width**

**DC Offset Cancellation Loop**

**(10 ns - 100ns)**

**Zero Cross**

**Discriminator**

**Polarity**

Fig. 1. Leading edge circuit qualifies output of zero-cross discriminator. Leading edge and zero-cross circuits consists of a cascade of low-gain, high-bandwidth simple differential amplifiers driving a very high gain-bandwidth product (GBW) comparator

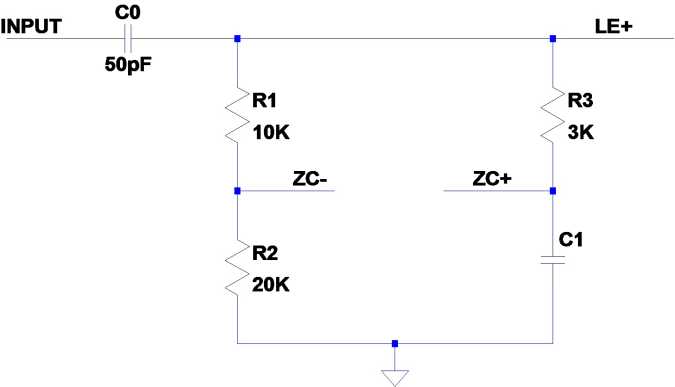


Fig. 2. Nowlin circit using lumped components, R3 amd Ci, to implement delay. Here the fraction is « 0.7.

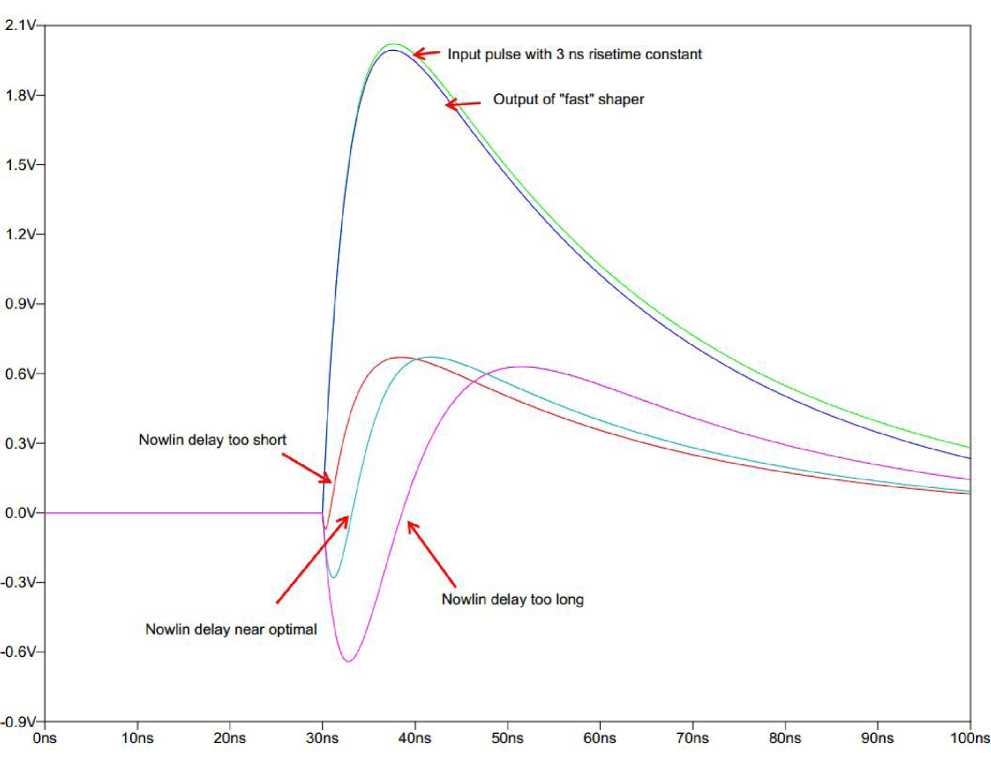


Fig. 3. Input signal with 3 ns risetime constant. A programmable delay allows matching of the delay provided by the Nowlin circuit to the risetime constant of the input signal.

possessing a very wide bandwidth, but relatively low-gain (4X - 7X) with the final output stage driving a very fast analog comparator. The purpose of cascading a relatively large number of high bandwidth gain stages is to force linear operation where delay is independent of amplitude. In short, the cascaded amplifier serves as a SR enhancer. For a first-order system, it is well-known that if the input risetime is not to be severely degraded, the bandwidth, BW, of the amplifier must obey the following equation

0 35

BW > « 50 MHz

^10-90

Since we are cascading N stages, the BW of each stage must be increased by vN « 2.5 resulting in a differential amplifier bandwidth of 125 MHz if the overall BW is to be 50 MHz. If the stage gain, G, is 5 then the GBW of a single differential amplifier stage needs to be around 625 MHz, clearly achievable in 0.5 micron CMOS.

Jitter and Time Walk Analyses For an input pulse with a risetime constant of 3 nsec, we require that

* the walk not exceed +/- 150 ps over the entire 2 mV - 2 V input amplitude range,
* and the jitter should not exceed 300 ps at an input level of 2 mV.

We analyze jitter first. Jitter is a consequence of the electronics noise associated with the Nowlin circuit as well as the noise of the first differential amplifier in the zero-cross discriminator circuit (where we assume the noise of succeeding stages when referred to the input is negligible).

Time jitter can be estimated by taking the total integrated noise at the output of the Nowlin circuit and then dividing by the sR.

gv

Gt = SR

From Fig. 3, one observes a SR of 200V when the input pulse amplitude is 2 Volts. Because of the exponential nature of the input signal, sR is proportional to pulse amplitude but inversely proportional to the input risetime constant, Tr. In other words, when the pulse amplitude is reduced to 20 mV, the SR is 2 V .If Tr is 30 ns rather than 3 ns, then SR will go down by a factor of ten. A conservative estimate of total integrated noise, gv , at the output of the Nowlin circuit is 200 ^V. Table I below summarizes the expected jitter performance of the proposed IC.

|  |  |  |  |
| --- | --- | --- | --- |
| Amplitude (V) | at (Tr = 3ns) (ps) | <rt (Tr = 15ns) (ps) | <rt (Tr = 100ns) (ps) |
| 2.0 | 1 | 5 | 33 |
| 0.2 | 10 | 50 | 330 |
| 0.02 | 100 | 500 | 3300 |

table I

Time jitter as function of pulse amplitude and risetime constant.

We analyze time walk next. Time walk is is used to describe systematic variation in the rising edge of the discriminator output signal as a function of pulse height. if we assume a single-pole response for the analog comparator with a gain-bandwidth-product of GBWc, it is not difficult to show that the variation in propagation delay, Atpd, due to input pulse amplitude is

*Vdd*

A tpd ~

2 ■ n ■ GBW*c* ■ G*N* ■ SR*m*m where VDD is the supply voltage, G is the gain of a single differential amplifier stage, N is the number of stages, and *SRmin* is the SR with a pulse amplitude of 20 mV. Table II summarizes the expected walk performance (over the dynamic range of 2 mV - 2 V) for three representative risetime constants.

in reality, the time walk may increase at low amplitudes because of residual offset. ultimately, how well the discriminator performs at low amplitude will depend on the effectiveness of the

dynamic offset cancellation loop, shown in Fig. 1. It can be shown that residual offset alters the time at which one crosses zero as given by

At

cross

a 2.2 ■ Tr ■

)

where VOs is the residual input referred offset and A is the amplitude of the input pulse. It is important that the residual offset be driven to the sub-mV level. The ’’slow” DC offset cancellation loop has to be ”slow” enough so as not to interfere with the pulse as it passes through the zero-cross discriminator but yet fast enough so that pulse repetition rates as high as 1 kHz can be accommodated. This will require significant design effort but is certainly feasible, as demonstrated in [1]. The wide range of pulse risetime constants we wish to support makes this problem more difficult but not impossible.

|  |  |
| --- | --- |
| tr (ns) | Time Walk (ps) |
| 3 | ± 160 |
| 15 | ± 360 |
| 100 | ± 920 |

TABLE II

Time walk as function of risetime constant, rr for G = 5, N = 6 and GBWc = 250MHz.

T**imeline**

A timeline for the major development tasks is presented in Fig. 4. A top-down design strategy will be employed. Behavioral simulations written in MATLAB will be used to validate the design specifications and to develop an effective and stable DC offset cancellation loop for both the zero and leading edge circuits. This will be followed by drawing a complete set of schematics for the IC using Cadence’s Virtuoso Schematic Editor. A VerilogA behavioral description will be developed for each of the circuit symbols. After successful simulation of this behavioral description each VerilogA block will be replaced with a transistor level description. As the transistor level descriptions are validated, they will committed to physical layout and verification. Extensive simulations on the parasitically extracted netlist will be performed before submitting the IC for fabrication. upon returning from fab, a prototype system will be constructed. A small number of systems will then be constructed and distributed to interested users. The success of the project will be assessed and conveyed to NsF via a final report.

C**onclusions**

The design of a multi-channel discriminator design for a dynamic range from 2 mV to 2 V and rise time constants ranging from 3 ns to 100 ns is feasible. The wide range of pulse risetime constants which must be supported, makes the design challenging but yet quite doable.

R**eferences**

[1] M. Simpson, G. Young, R. Jackson, and M. Xu, “A monolithic, constant-fraction discriminator using distributed r-c delay line shaping,” Nuclear Science, IEEE Transactions on, vol. 43, no. 3, pp. 1695-1699, Jun 1996.

Fig. 4. Timeline of major tasks.

Perform MATLAB simulations

Create VerliogA model for chip

Perform detailed circuit design

Layout and verify DISC16C

Fabricate and test DISC16C

Assemble prototype system

Assemble small number of systems

Distribute systems and train users

Evaluate success of project

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