

D



Tit



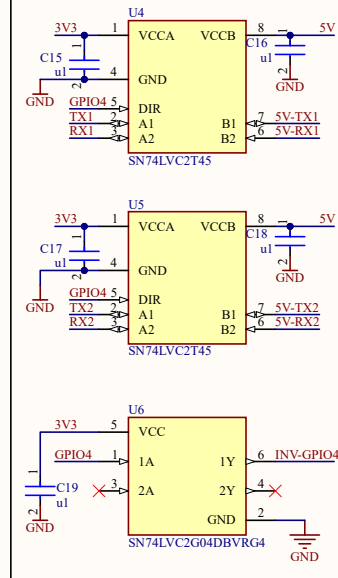
			PWR
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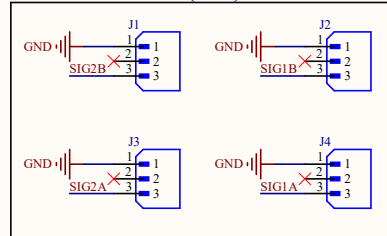
BLINK

D

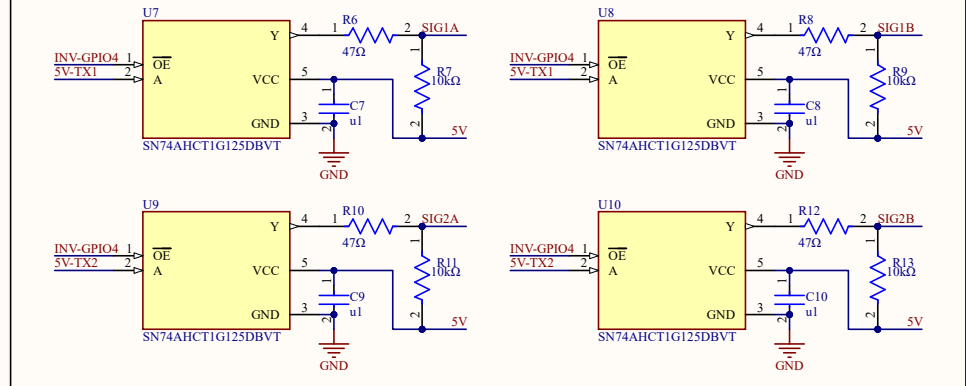
Logic Shifter + Inverter



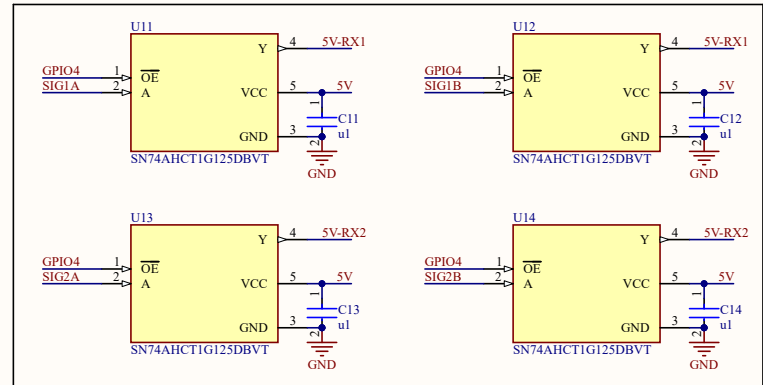
Servo Connectors (SIG)



TX Gate Buffers

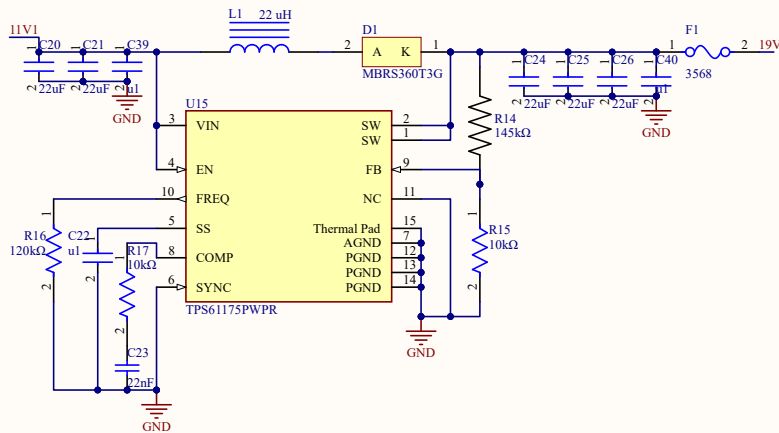


RX Gate Buffers

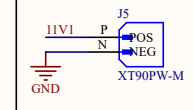


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File:	C:\Users\U\UART LOGIC.SchDoc	Drawn By:

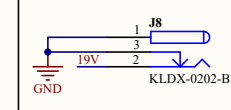
Jetson Regulator



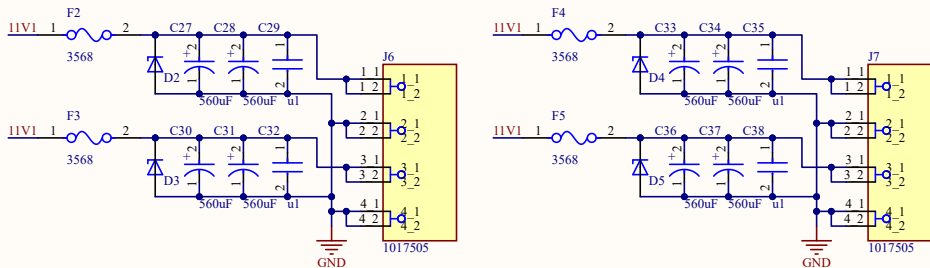
Battery Connector



Jetson Connector



Servo Connectors (PWR)



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