Circuit Analysis using Monotone+Skew Splitting

Thomas Chaffey[1], Sebastian Banert[2], Pontus Giselsson[2] and Richard Pates[2]

***Abstract*— It is shown that the behavior of an m-port circuit of maximal monotone elements can be expressed as a zero of the sum of a maximal monotone operator containing the circuit elements, and a structured skew-symmetric linear operator representing the interconnection structure, together with a linear output transformation. The Condat–Vũ algorithm solves inclusion problems of this form, and may be used to solve for the periodic steady-state behavior, given a periodic excitation at each port, using an iteration in the space of periodic trajectories.**

I. INTRODUCTION

The study of monotone operators originated in attempts to generalize classical electrical network theory from circuits of linear, time invariant elements to circuits containing nonlinear elements. Building on the "quasi-linear resistor" of Duffin [1], Minty defined a monotone operator as an incremental, nonlinear generalization of a passive LTI circuit component [2], [3]. The theory of monotone operators has since become central to several lines of research. Following the influential work of Rockafellar [4], [5], monotone operators have become a pillar of optimization theory, the essential observation being that the subdifferential of a closed, convex and proper function is a maximal monotone operator. *Splitting algorithms* for solving convex optimization problems have seen a surge in interest in the last decade, due to their amenability to large-scale and distributed problems [6], [7], [8], [9], [10], [11]. There is a large body of literature exploiting the property of monotonicity in the time-stepping simulation of discontinuous dynamical systems [12], [13], [14], [15], and a circuit interpretation of monotonicity has been used to study consensus [16].

The use of monotone operators in circuit analysis has recently been revisited by Chaffey and Sepulchre [17]. A one-port circuit consisting of a collection of monotone operators connected in series and parallel defines a monotone current–voltage relation. A splitting algorithm is constructed which solves the steady-state behavior of the circuit, where the structure of the algorithm is in direct correspondence with the circuit topology. This gives a method for solving the forced periodic response of a nonlinear circuit using an iteration in the space of periodic trajectories, rather than forwards in time.

Alternative methods for finding the periodic response of nonlinear circuits are either approximate (for instance, the describing function method [18]), or involve integrating a differential equation forwards in time and waiting for convergence to steady state [19], [20]. Specialized methods for circuits containing monotone elements may be found in the literature on non-smooth differential inclusions [21]. The methods of Heemels *et al.* [22] involve iteratively computing the resolvent of the transition map of a differential inclusion, and most closely resemble the method presented in this paper. For circuits modelled as linear complementarity systems, methods have been developed by Ianelli *et al.* [23] and Meingast *et al.* [24].

In this paper, we generalize the signal space approach of [17] to circuits with an arbitrary number of ports and an arbitrary interconnection structure. For such a circuit, the mapping between any two voltages or currents is not necessarily monotone. However, the circuit can be described by a monotone mapping from a set of external excitations to a set of internal currents and voltages, together with a linear mapping from the internal currents and voltages to a set of external responses. We use a splitting algorithm to solve for the internal signals in terms of the excitations, and then apply the output mapping to obtain the responses. The interconnection structure of the circuit is described by a skew-symmetric linear operator (the graph of which defines a Dirac structure [25, §2.2.2]), and the collection of elements is described by a diagonal monotone operator. Partitioning the elements into admittances (mapping voltages to currents) and impedances (mapping currents to voltages) expresses the circuit as precisely the *monotone+skew form* [26] of zero inclusion which may be solved using the Condat–Vũ algorithm [27], [28], a generalization of the Chambolle–Pock algorithm [29]. In fact the pairing between optimization problem and electrical circuit is stronger, and the solutions to any zero inclusion problem of this form define the behavior of an electrical circuit that can be synthesized with passive and reciprocal components. To the best of the authors' knowledge, the method of [17] and the generalization we present in this paper represent the first use of splitting algorithms to explicitly partition a circuit simulation problem according to the interconnection structure. This gives a method of circuit simulation which is readily distributed and comes pre-equipped with an algorithmic complexity theory. A further advantage is that set-valued elements, such as the ideal diode, are handled via their resolvents, which are continuous functions.

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[1]T. Chaffey is with Pembroke College, University of Cambridge, United Kingdom, tlc37@cam.ac.uk

[2]S. Banert, P. Giselsson and R. Pates are with the Department of Automatic Control, Lund University, Lund, Sweden {sebastian.banert, pontusg, richard.pates}@control.lth.se

The remainder of this paper is structured as follows. Section II introduces the class of m-port circuits and the problem considered in this paper, solving the periodic behavior of an m-port circuit. Section III describes how the behavior of an m-port circuit of monotone elements may be expressed as a monotone+skew zero inclusion: this is captured in Theorem 1, which represents the main theoretical contribution of this paper. Section IV gives an overview of the Condat–Vũ algorithm, which we use in Section V to two detailed examples of the proposed method.

II. PRELIMINARIES AND PROBLEM STATEMENT

Let $\mathcal{H}$ denote an arbitrary Hilbert space, and $\langle \cdot, \cdot \rangle$ denote its inner product. We will focus in particular on the Hilbert space $L^m_{2,T}$ of square-integrable signals defined on the time axis $[0, T]$ and taking values in $\mathbb{R}^m$, with inner product

$$\langle u, y \rangle = \int_0^T u(t)^\top y(t) \, \mathrm{d}t.$$

T-periodic signals may be represented as signals in $L^m_{2,T}$ by considering only a single period. The reason for using the space $L_{2,T}$ is that it allows our method to be made computational via discretization, as demonstrated in Section V. The representation of a circuit introduced in Section III is equally valid on any Hilbert space.

By an *operator* on a Hilbert space $\mathcal{H}$, we will mean a (possibly) multi-valued mapping on $\mathcal{H}$, that is, a function $\mathcal{H} \to 2^{\mathcal{H}}$, where $2^{\mathcal{H}}$ denotes the power set of $\mathcal{H}$. Given an operator $A : \mathcal{H} \to 2^{\mathcal{H}}$, the *relation* of A, denoted $\mathrm{rel}(A)$, is defined to be the set $\{(u, y) \mid y \in A(y)\} \subseteq \mathcal{H} \times \mathcal{H}$. An operator is said to be *monotone*[1] if, for any $(u_1, y_1), (u_2, y_2) \in \mathrm{rel}(A)$,

$$\langle u_1 - u_2, y_1 - y_2 \rangle \geq 0. \tag{1}$$

A monotone operator is said to be *skew* or *lossless* if (1) holds with equality. A monotone operator is said to be *maximal* if its relation is not properly contained in the graph of any other monotone operator.

The identity operator, $x \mapsto x$, is denoted Id. The *(relational) inverse* of an operator A is the operator A^{-1} with relation $\mathrm{rel}(A^{-1}) = \{(y, u) \mid (u, y) \in \mathrm{rel}(A)\}$. The *$\alpha$-resolvent* of an operator A is the operator $(\mathrm{Id} + \alpha A)^{-1}$.

By an operator on $L^m_{2,T}$, we will mean an operator which maps a T-periodic signal into another T-periodic signal, both of which have a finite integral over $[0, T]$. This mapping can be completely described by considering a single period of the input and a single period of the output, giving a mapping on $L^m_{2,T}$.

A *one-port circuit* is a circuit with two terminals, described by a relation between the voltage between the two terminals, and the current through them. We will model circuit elements as one-port circuits described by a maximal monotone operator on $L_{2,T}$, either from voltage to current (admittance form) or current to voltage (impedance form). Particular examples include the admittance of a nonnegative, LTI capacitor, the impedance of a nonnegative, LTI inductor, and any maximal monotone nonlinear resistor [17, §VI]. The relations for these elements are defined respectively through laws of the form

$$\begin{aligned} i(t) &= \frac{\mathrm{d}}{\mathrm{d}t} C v(t) \\ v(t) &= \frac{\mathrm{d}}{\mathrm{d}t} L i(t) \\ v(t) &= R(i(t)), \end{aligned}$$

where $C \geq 0$, $L \geq 0$ and $R(\cdot)$ is non-decreasing and defines a continuous curve in the plane, with no endpoints.

An ideal $(m+n)$-port transformer is a device with a hybrid representation of the following form

$$\begin{pmatrix} \mathbf{i}_1(t) \\ \mathbf{v}_2(t) \end{pmatrix} = \begin{pmatrix} 0 & T^\top \\ -T & 0 \end{pmatrix} \begin{pmatrix} \mathbf{v}_1(t) \\ \mathbf{i}_2(t) \end{pmatrix}, \tag{2}$$

where $T \in \mathbb{R}^{n+m}$ is the *turns ratio matrix*, and each entry a_{pq} of T gives the ratio of windings between driving point p and driving point q.

We define a *monotone m-port circuit with n elements* to be a circuit constructed in the following way. Begin with a box of wires and ideal transformers, connected arbitrarily. From this box, draw m pairs of terminals to form m external *driving points*. Draw a further n pairs of terminals, and across each of these pairs, connect a monotone one-port circuit element. This structure is shown in Figure 1. Throughout the paper, we will orient the voltage and current at a terminal pair of the box of wires so that $i(t)v(t)$ represents the instantaneous power *extracted* from the box (this is opposite to the usual orientation, but means we can choose the usual orientation for the circuit elements when we perform element extraction in Section III). An excitation at a driving point refers to an applied voltage (respectively, current), the response refers to the resulting observed current (voltage).

If we collect the driving point currents and current through each device in a vector $\iota \in L^{m+n}_{2,T}$ and the driving point voltages and voltage across each component into a vector $\nu \in L^{m+n}_{2,T}$, the *behavior* [31] of an m-port circuit $\mathcal{C}$ on $L_{2,T}$ is the set of all $\{(\iota, \nu) \in L^{m+n}_{2,T} \times L^{m+n}_{2,T}\}$ that obey the circuit interconnection constraints and device laws of $\mathcal{C}$.

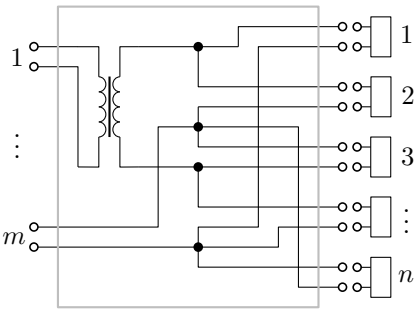

Fig. 1. An m port circuit modelled using the element extraction approach. The m terminal pairs on the left represent external driving points. The grey box contains wires and ideal transformers, governed by Kirchoff's laws and the ideal transformer relation (2). The n one-port elements are connected to n internal ports, shown on the right.

[1]Monotonicity on $L_{2,T}$ for all T is equivalent to incremental passivity [30].

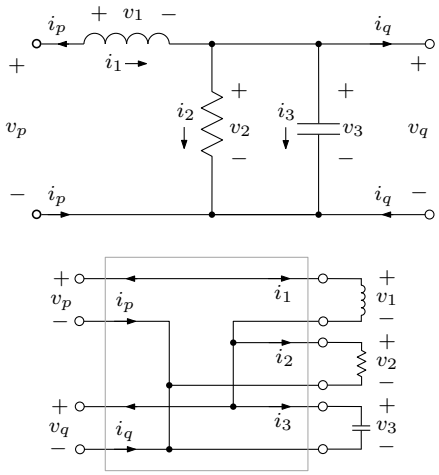

Fig. 2. Above: a two-port RLC circuit. Below: the same circuit, with the elements extracted.

Theorem 1 of Section III will give a precise mathematical formulation for this informal definition of a circuit and its behavior. The problem considered in the remainder of this paper is the following:

> *given a monotone m-port circuit $\mathcal{C}$, and a T-periodic excitation signal at each driving point, find a set of steady-state periodic responses, if such a set exists.*

It will be shown in Theorem 1 that this problem is equivalent to finding a zero to a sum of monotone operators and applying a linear transformation (Equations (5) and (6)).

We conclude this preliminary section with a simple example, which illustrates the circuit modelling approach formalized in Section III.

Example 1. Consider the RLC circuit shown in the top of Figure 2. Assume all signals are T-periodic for some fixed $T > 0$, and belong to $L_{2,T}$. Suppose we want to determine the mapping from v_p to v_q, assuming that $i_q(t) = 0$ for all t and i_p is free. The bottom of Figure 2 shows the same circuit, with the elements on one side, the external ports on the other, and a collection of wires joining them, enclosed in the grey dashed box. Kirchoff's current and voltage laws for the grey box can be written as

$$\begin{pmatrix} i_p(t) \\ v_q(t) \\ v_1(t) \\ v_2(t) \\ i_3(t) \end{pmatrix} = \left(\begin{array}{cc|ccc} 0 & 0 & 0 & -1 & -1 \\ 0 & 0 & -1 & 0 & 0 \\ \hline 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & -1 & 1 & -1 & 0 \end{array}\right) \begin{pmatrix} v_p(t) \\ i_q(t) \\ i_1(t) \\ i_2(t) \\ v_3(t) \end{pmatrix}. \quad (3)$$

This is a *hybrid representation* for the subcircuit contained in the grey box. A partition of the circuit variables which admit a hybrid representation is guaranteed to exist, but in general is not unique. The standard methods of loop and cut-set analysis can be used to find a hybrid representation [32]. Here, we have put the variables we would like to solve, v_q and i_p, on the left, in the *response* vector, and the variables we would like to treat as inputs, v_p and i_q, on the right, in the *excitation* vector.

Suppose $L, R, C \geq 0$ are the inductance, resistance and capacitance respectively, of the elements in Figure 2. Let $\hat{L}$ and $\hat{R}$ denote the impedances of the inductor and resistor respectively, as operators on $L_{2,T}$. Similarly, let $\hat{C}$ denote the admittance of the capacitor, as an operator on $L_{2,T}$. Substituting the device laws into Equation (3) then gives a complete description of the circuit behavior, as the sum of a monotone operator (offset by the inputs v_p and i_q) and a skew operator, together with a linear output transformation:

$$0 \in \begin{pmatrix} \hat{L}(i_1) \\ \hat{R}(i_2) \\ \hat{C}(v_3) \end{pmatrix} + \begin{pmatrix} 0 & 0 & -1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \end{pmatrix} \otimes \mathrm{Id} \begin{pmatrix} i_1 \\ i_2 \\ v_3 \end{pmatrix} + \begin{pmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \end{pmatrix} \otimes \mathrm{Id} \begin{pmatrix} v_p \\ i_q \end{pmatrix}, \quad (4)$$

$$\begin{pmatrix} i_p \\ v_q \end{pmatrix} = \begin{pmatrix} 0 & -1 & -1 \\ -1 & 0 & 0 \end{pmatrix} \otimes \mathrm{Id} \begin{pmatrix} v_1 \\ i_2 \\ i_3 \end{pmatrix},$$

where Id is the identity mapping on $L_{2,T}$. ⌟

III. FROM CIRCUITS TO MONOTONE INCLUSIONS

In this section, we formalize the modelling approach of Example 1. We adopt the element extraction approach of Hughes [33], which builds on the approach of Anderson and Newcomb [34]. This allows us to express the behavior of an m-port circuit as the zeros of the sum of a skew-symmetric linear operator, representing the interconnection structure, and a diagonal monotone operator, representing the circuit elements, together with a linear mapping from the internal signals to the response signals. This representation is formalized in the following theorem.

Theorem 1. *Let $\mathcal{C}$ be a monotone m-port circuit with n elements. Then there exist:*

1) *a partition of the driving point voltages $\{v_k\}_{k=1\ldots m}$ and driving point currents $\{i_k\}_{k=1\ldots m}$ into vectors $\mathbf{u}, \mathbf{y} \in L^m_{2,T}$,*
2) *vectors $\mathbf{i} \in L^p_{2,T}$ and $\mathbf{v} \in L^q_{2,T}$, $p + q = n$, such that for each element either the voltage across it is in $\mathbf{v}$ or the current through it is in $\mathbf{i}$,*
3) *matrices $\tilde{M} \in \mathbb{R}^{q\times p}$, $\tilde{B}_R \in \mathbb{R}^{p\times m}$, $\tilde{B}_G \in \mathbb{R}^{q\times m}$ and $\tilde{D} \in \mathbb{R}^{m\times m}$, and*
4) *monotone operators $R : L^p_{2,T} \to L^p_{2,T}$, and $G : L^q_{2,T} \to L^q_{2,T}$, which are the concatenation of the impedances of elements whose currents are in $\mathbf{i}$ and admittances of elements whose voltages are in $\mathbf{v}$,*

such that the behavior of $\mathcal{C}$ on $L_{2,T}$ is the set of solutions to

$$\begin{pmatrix} R(\mathbf{i}) \\ G(\mathbf{v}) \end{pmatrix} + \begin{pmatrix} \mathbf{0} & M^\top \\ -M & \mathbf{0} \end{pmatrix} \begin{pmatrix} \mathbf{i} \\ \mathbf{v} \end{pmatrix} - \begin{pmatrix} B_R \\ B_G \end{pmatrix} \mathbf{u} = 0, \quad (5)$$

$$\mathbf{y} = (B_R^\top\ B_G^\top) \begin{pmatrix} \mathbf{i} \\ \mathbf{v} \end{pmatrix} + D\mathbf{u}, \quad (6)$$

where $M = \tilde{M} \otimes \mathrm{Id}$, $B_R = \tilde{B}_R \otimes \mathrm{Id}$, $B_G = \tilde{B}_G \otimes \mathrm{Id}$ and $D = \tilde{D} \otimes \mathrm{Id}$.

It should be pointed out that, while Theorem 1 guarantees the existence of a partition of currents and voltages such that the circuit has a monotone+skew form, this partition may not be unique, and for any particular partition, the monotone+skew form of (5) and (6) is not guaranteed to exist.

Our general approach to solving for the steady state responses will be to first solve Equation (5) for the internal signals $\mathbf{i}$ and $\mathbf{v}$, using a monotone inclusion algorithm, and then to apply the output transformation (6) to obtain the response signals in $\mathbf{y}$.

The operators R and G contain impedances and admittances of the circuit elements. Since we have made no assumption on whether we have an impedance or admittance operator for each element, R and G may contain inverses of operators on $L_{2,T}$. The inverse is taken to be a relational inverse, and always exists, but may not have a domain equal to all of $L_{2,T}$. For example, the admittance of an LTI capacitor is an operator on $L_{2,T}$, but its impedance is a static gain cascaded with an integrator, and only maps signals whose integral on $[0, T]$ is zero into T-periodic signals. The result of this is that, while Equations (5) and (6) can always be written, for a given set of excitation signals, solutions may not exist. The algorithm we propose in Section IV is guaranteed to find a solution, if one exists, but does not guarantee its existence. It is, however, always well-posed. Despite the fact that R and G may have restricted domain, they are only ever accessed via their resolvents. As the elements are assumed to be maximal monotone, it follows from Minty's surjectivity theorem [3] that their resolvents have domain $L_{2,T}$, and the algorithm steps are always well-defined.

Proof of Theorem 1. We follow the element extraction approach described in [33, §2] and illustrated in Figure 1. We form an $m + n$ circuit $\mathcal{C}_{\text{wires}}$ by replacing each of the elements with an internal port. Denote the currents at the internal ports by $\{i_k\}_{k=m+1\ldots m+n}$ and the voltages at the internal ports by $\{v_k\}_{k=m+1\ldots n}$. The sign of the current at each driving point and internal port is chosen so that the product $i_k(t)v_k(t)$ is the instantaneous power extracted from the port. It then follows from [33, Eq. (8)] that there exist $\mathbf{u}, \mathbf{y}, \mathbf{i}, \mathbf{v}$ as specified in the theorem statement and such that, writing $\mathbf{z} = (\mathbf{i}, \mathbf{v})^\top$,

$$\left(\underbrace{\begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix}}_{H} \otimes \mathrm{Id}\right) \begin{pmatrix} \mathbf{u} \\ \mathbf{z} \end{pmatrix} = \begin{pmatrix} \mathbf{y} \\ \tilde{\mathbf{z}} \end{pmatrix}, \tag{7}$$

where $\tilde{\mathbf{z}}$ contains the dual variables to $\mathbf{z}$, that is, if for index k and port j, $\mathbf{z}_k = v_j$, then $\tilde{\mathbf{z}}_k = i_j$, and if $\mathbf{z}_k = i_j$, then $\tilde{\mathbf{z}}_k = v_j$. Since $\mathcal{C}_{\text{wires}}$ is lossless and contains no dynamic components, for any fixed time t, $\mathbf{u}^\top(t)\mathbf{y}(t) + \mathbf{z}^\top(t)\tilde{\mathbf{z}}(t) = \sum_{k=1}^{n+m} i_k(t)v_k(t) = 0$. It follows that H is skew-symmetric. Furthermore, because $\mathbf{z}$ is partitioned into $(\mathbf{i}, \mathbf{v})^\top$, H_{22} has the form $\begin{pmatrix} \mathbf{0} & -\tilde{M}^\top \\ \tilde{M} & \mathbf{0} \end{pmatrix}$, where $\tilde{M} \in \mathbb{R}^{q\times p}$ (this follows from the independence of Kirchoff's voltage and current laws, see, for example, [35, Thm. 6-3]).

The circuit elements give n relations between the entries of $\mathbf{z}$ and the entries of $\tilde{\mathbf{z}}$. Collecting those that map currents to voltages in a single operator $R : L^p_{2,T} \to L^p_{2,T}$, and those that map voltages to currents in a single operator $G : L^q_{2,T} \to L^q_{2,T}$, and substituting $(R(\mathbf{i}), G(\mathbf{v}))^\top$ for $\tilde{\mathbf{z}}$ in Equation (7), gives the equations

$$\begin{pmatrix} R(\mathbf{i}) \\ G(\mathbf{v}) \end{pmatrix} + \left(\begin{pmatrix} \mathbf{0} & \tilde{M}^\top \\ -\tilde{M} & \mathbf{0} \end{pmatrix} \otimes \mathrm{Id}\right) \begin{pmatrix} \mathbf{i} \\ \mathbf{v} \end{pmatrix} - (H_{21} \otimes \mathrm{Id})\mathbf{u} = 0,$$

$$\mathbf{y} = (H_{12} \otimes \mathrm{Id}) \begin{pmatrix} \mathbf{i} \\ \mathbf{v} \end{pmatrix} + (H_{11} \otimes \mathrm{Id})\mathbf{u}.$$

The proof concludes by noting that skew-symmetry of H implies $H_{12} = -H_{21}^\top$, and writing $\tilde{B} = H_{21}$ and $\tilde{D} = H_{11}$ to obtain Equations (5) and (6). □

Remark 1. Theorem 1 shows that the behavior of any monotone m-port circuit may be written in the form of (5) and (6). The opposite is also true: the solutions to any set of equations in the form of (5) and (6) correspond to the behavior of a monotone m-port circuit, constructed in the following manner. Firstly, the matrix H is synthesized using the method of [36, Ch. 10]. The elements in R and G are then connected across n of the terminal pairs of this realization; the remaining m terminal pairs are the external driving points. ⌟

IV. MONOTONE INCLUSION ALGORITHMS

Equation (5) expresses the relation between excitations, internal currents and internal voltages as the zero of the sum of two maximal monotone operators, one of which is a structured skew-symmetric matrix. There are many algorithms for finding the zero of the sum of two maximal monotone operators, including the Douglas-Rachford method and its special case the alternating direction method of multipliers (ADMM), forward-backward splitting (assuming one of the operators is cocoercive), and forward-backward-forward splitting (assuming one of the operators is Lipschitz continuous). A method that exploits the particular block monotone+skew structure of (5) is the Condat–Vũ algorithm [27], [28], which we will use in this paper. A benefit of this method is that it evaluates M only using forward evaluations, rather than through any sort of inverse. This gives low-cost iterations that make it suitable for solving large-scale problems. A second benefit is that the device operators G and R are only evaluated via their resolvents, allowing multi-valued elements such as diodes to be used. This will be further illustrated in Section V. For our problem (5), the Condat–Vũ iteration is given by Algorithm 1. The algorithm alternately updates the internal currents and internal voltages. The fixed points of this iteration are the solutions to (5). Convergence to a fixed point is guaranteed if τ and σ satisfy $\tau\sigma < \frac{1}{\|M\|^2}$, where $\|M\|$ denotes the operator norm of M [27], [28].

Algorithm 1 The Condat–Vũ algorithm.

Given: zero inclusion of the form (5), step sizes $\sigma, \tau > 0$, initial values $\mathbf{i_0}, \mathbf{v_0}$, tolerance $\varepsilon > 0$.

Define: $\bar{R}(\mathbf{i}) \coloneqq R(\mathbf{i}) - B_R\mathbf{u}$, $\bar{G}(\mathbf{v}) \coloneqq G(\mathbf{v}) - B_G\mathbf{u}$.
Iterate:

$$\mathbf{i}_{k+1} = (\mathrm{Id} + \tau\bar{R})^{-1}(\mathbf{i}_k - \tau M^\top \mathbf{v}_k)$$
$$\mathbf{v}_{k+1} = (\mathrm{Id} + \sigma\bar{G})^{-1}(\mathbf{v}_k + \sigma M(2\mathbf{i}_{k+1} - \mathbf{i}_k))$$

while $\|\mathbf{v}_{k+1} - \mathbf{v}_k\| > \varepsilon$.

V. EXAMPLES

In this section, we apply our computational method to two examples: the RLC circuit of Example 1, and a bridge rectifier. Code for both examples can be found at `https://github.com/ThomasChaffey/circuit-analysis-using-monotone-skew-splitting`.

Example 2. In this example, we revisit the RLC circuit of Example 1, and apply the Condat–Vũ algorithm to compute the voltage response v_q when driving point p is connected to a sinusoidal voltage source, and driving point q is open, so $i_q(t) = 0$ for all t. Voltage and current signals are discretized at a regular interval Δt to produce discrete signals of length N. The differential operator $\frac{\mathrm{d}}{\mathrm{d}t}$ is replaced by the periodic backwards finite difference operator, $\nabla(u)(k) \coloneqq (u(k) - u(k-1))/\Delta t$, where $u(-1) \coloneqq u(N)$. The operators $\hat{C}$ and $\hat{L}$ then have a matrix representation of CD and LD respectively, where D is the $N \times N$ matrix

$$\begin{pmatrix} 1 & 0 & 0 & \dots & -1 \\ -1 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & 1 \end{pmatrix}.$$

In order to apply the Condat–Vũ algorithm, the resolvents of each element must be calculated. The resolvents $(\mathrm{Id} + \sigma\hat{C})^{-1}$ and $(\mathrm{Id} + \tau\hat{L})^{-1}$ are given by the matrices $(I + \sigma CD)^{-1}$ and $(I + \tau LD)^{-1}$, which are precomputed and stored in memory. The resolvent $(\mathrm{Id} + \tau\hat{R})^{-1}$ is equivalent to scalar multiplication by $1/(1 + \tau R)$. The input offsets v_p and $-i_q$ are incorporated into the resolvents by offsetting their inputs: $(\mathrm{Id} + \tau\bar{L})^{-1}(i_1) = (\mathrm{Id} + \tau\hat{L})^{-1}(i_1 - \tau v_p)$ and $(\mathrm{Id} + \sigma\bar{R})^{-1}(v_3) = (\mathrm{Id} + \sigma\hat{R})^{-1}(v_3 + \tau i_q)$. To compute v_q, given v_p and assuming $i_q(t) = 0$ for all t, Algorithm 1 is applied to solve Equation (5), and Equation (6) is then computed. Example input and output signals are plotted in Figure 3. ⌟

Example 3. This example considers the filtered bridge rectifier shown in Figure 4. We will consider the voltage response v_q when driving point p is connected to a sinusoidal voltage source, and driving point q is connected to a constant current source. We begin by using the element extraction approach of Theorem 1 to express the circuit in monotone+skew form.

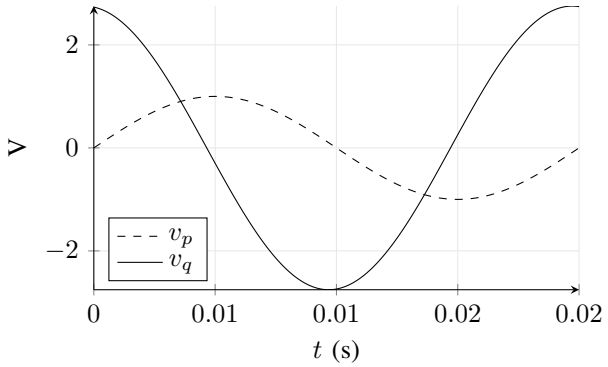

Fig. 3. Input voltage v_p and output voltage v_q for the RLC circuit of Figure 2, computed using the Condat–Vũ algorithm. Circuit parameters are $R = 1\,\Omega$, $L = 0.001\,\mathrm{H}$ and $C = 0.01\,\mathrm{F}$, algorithm parameters are $\Delta t = 1 \times 10^{-4}$ s (200 samples) and step sizes of $\tau = \sigma = 0.05$.

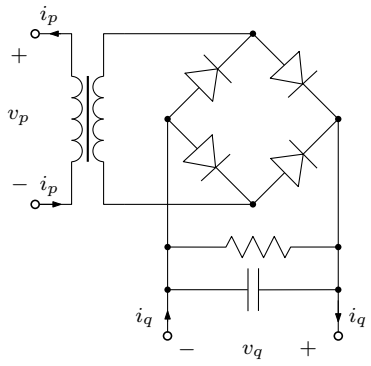

Fig. 4. A bridge rectifier with filtering capacitor (capacitance C) and nominal load resistor (resistance R). The transformer is a $1:24$ step-down transformer.

Figure 5 shows the circuit of Figure 4 with the elements replaced by internal ports. The resistor and capacitor are combined into a single subcircuit, and replaced by port 0. The transformer results in extra factors of 24 at driving point p. Following the procedure of Section III, we select an excitation and response variable at each driving point, and derive a hybrid representation for the circuit of wires. v_p is selected as the excitation at driving point p and v_q is selected as the response at driving point q. The other variables may be partitioned arbitrarily, provided a hybrid representation exists for the partition. For example, we can choose the currents at ports 0, 1 and 2, and the voltages at ports 3 and 4, to be excitation variables. This gives the hybrid representation

$$\begin{pmatrix} i_p \\ v_q \\ v_0 \\ v_1 \\ v_2 \\ i_3 \\ i_4 \end{pmatrix} = \left(\begin{array}{cc|ccccc} 0 & 0 & 0 & \frac{1}{24} & \frac{-1}{24} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & -1 \\ \hline 0 & 0 & 0 & 0 & 0 & -1 & -1 \\ \frac{-1}{24} & 0 & 0 & 0 & 0 & 0 & 1 \\ \frac{1}{24} & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 1 & -1 & 0 & 0 & 0 \end{array}\right) \begin{pmatrix} v_p \\ i_q \\ i_0 \\ i_1 \\ i_2 \\ v_3 \\ v_4 \end{pmatrix} \quad (8)$$

where the time dependence of each signal has been

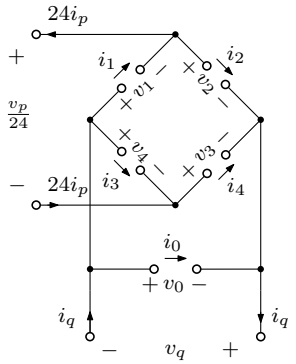

Fig. 5. The bridge rectifier of Figure 4 with elements replaced by internal ports. Polarities at the ports are chosen so that the product $i_k v_k$ represents power extracted from the circuit.

dropped. The devices are described by

$$\begin{pmatrix} v_0 \\ v_1 \\ v_2 \\ i_3 \\ i_4 \end{pmatrix} = \begin{pmatrix} R(\mathbf{i}) \\ G(\mathbf{v}) \end{pmatrix} \coloneqq \begin{pmatrix} R_{RC}(i_0) \\ R_D(i_1) \\ R_D(i_2) \\ G_D(v_3) \\ G_D(v_4) \end{pmatrix}, \tag{9}$$

where $\mathbf{i} \coloneqq (i_0, i_1, i_2)^\top$ and $\mathbf{v} \coloneqq (v_3, v_4)^\top$. R_{RC} is the convolution operator of the RC filter in impedance form, described by the operator $R(RC\frac{\mathrm{d}}{\mathrm{d}t}+1)^{-1}$, where $\frac{\mathrm{d}}{\mathrm{d}t}$ represents the differential operator on $L_{2,T}$. R_D is the impedance of an ideal diode:

$$(R_D i)(t) = \begin{cases} \{0\} & i(t) > 0 \\ (-\infty, 0] & i(t) = 0. \end{cases}$$

G_D is the admittance of an ideal diode, given by the relational inverse of R_D:

$$(G_D v)(t) = \begin{cases} \{0\} & v(t) < 0 \\ [0, \infty) & v(t) = 0. \end{cases}$$

Substituting Equation (9) in Equation (8) gives

$$\begin{pmatrix} R(\mathbf{i}) \\ G(\mathbf{v}) \end{pmatrix} + \begin{pmatrix} \mathbf{0}_{3\times 3} & M^\top \\ -M & \mathbf{0}_{2\times 2} \end{pmatrix} \begin{pmatrix} \mathbf{i} \\ \mathbf{v} \end{pmatrix} - \begin{pmatrix} B_R \\ B_G \end{pmatrix} \mathbf{u} = 0, \tag{10}$$

where

$$\mathbf{u} \coloneqq \begin{pmatrix} v_p \\ i_q \end{pmatrix}, \qquad M \coloneqq \begin{pmatrix} 1 & 0 & -1 \\ 1 & -1 & 0 \end{pmatrix} \otimes \mathrm{Id},$$
$$B_R \coloneqq \begin{pmatrix} 0 & 0 \\ \frac{-1}{24} & 0 \\ \frac{1}{24} & 0 \end{pmatrix} \otimes \mathrm{Id}, \qquad B_G \coloneqq \begin{pmatrix} 0 & 1 \\ 0 & 1 \end{pmatrix} \otimes \mathrm{Id}.$$

v_q and i_p are then obtained by the output equations $v_q = -v_0 = -v_3 - v_4$ and $i_p = i_1 - i_2$.

Similarly to Example 2, the voltage and current signals are discretized at a regular interval Δt to produce discrete signals of length N, and the differential operator $\frac{\mathrm{d}}{\mathrm{d}t}$ is replaced by the periodic backwards finite difference operator. In order to apply the Condat–Vũ algorithm, the resolvents $(\mathrm{Id}+\tau\bar{R})^{-1}$ and $(\mathrm{Id}+\sigma\bar{G})^{-1}$ must be calculated. It follows from [37, Prop. 23.16] that the resolvents can be calculated elementwise. Specifically, we have:

$$\begin{pmatrix} (\mathrm{Id}+\tau R)^{-1} \\ (\mathrm{Id}+\sigma G)^{-1} \end{pmatrix} = \begin{pmatrix} (\mathrm{Id}+\tau R_{RC})^{-1} \\ (\mathrm{Id}+\tau R_D)^{-1} \\ (\mathrm{Id}+\tau R_D)^{-1} \\ (\mathrm{Id}+\sigma G_D)^{-1} \\ (\mathrm{Id}+\sigma G_D)^{-1} \end{pmatrix}.$$

The offsets are dealt with by offsetting the inputs to the resolvent operators: $(\mathrm{Id}+\tau\bar{R})^{-1}(\mathbf{i}) = (\mathrm{Id}+\tau R)^{-1}(\mathbf{i}+B_R\mathbf{u})$, and similarly for $\bar{G}$.

The resolvent of the RC circuit impedance has an explicit form as multiplication by a matrix: $(\mathrm{Id}+\tau R_{RC})^{-1}(i) = (I+\tau R(RC\nabla+1)^{-1})^{-1}i$. The resolvent of the impedance of a diode is a rectified linear unit (ReLU):

$$(\mathrm{Id}+\tau R_D)^{-1}(i)(t) = \mathrm{ReLU}(i(t)) \coloneqq \begin{cases} i(t) & i(t) > 0 \\ 0 & \text{otherwise.} \end{cases}$$

This can be most easily seen graphically by plotting the current-voltage characteristic (Figure 6). Similarly, the resolvent of the admittance of a diode is given by $(\mathrm{Id} + \sigma G_D)^{-1}(v)(t) = -\mathrm{ReLU}(-v(t))$.

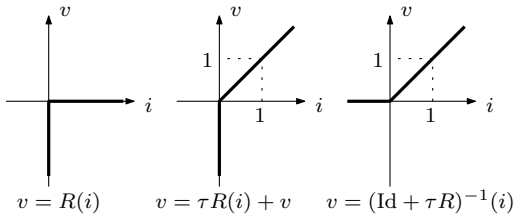

Fig. 6. The τ-resolvent of the impedance of a diode is a rectified linear unit (ReLU).

Applying the Condat–Vũ algorithm, with a resistance of $R = 1 \times 10^3\,\Omega$, a capacitance of $C = 10\,\mu$F, a 50 Hz sinuosidal input voltage $v_p(t) = 240.0\sin(100\pi)$ V, a constant input current $i_q(t) = -5$ mA, a discretization interval of $\Delta t = 1 \times 10^{-4}$ s (200 samples) and step sizes of $\tau = \sigma = 0.005$ gives the output shown in Figures 7 and 8. ⌟

VI. CONCLUSIONS

We have demonstrated that the behavior of a nonlinear m-port circuit composed of monotone elements may be expressed as the zero of the sum of a structured skew linear operator and a monotone operator. This is precisely the form of zero inclusion which may be solved using the Condat–Vũ algorithm. We have used this correspondence to develop a method for solving the periodic forced behavior of a monotone m-port circuit, extending the method of [17] to arbitrary numbers of ports and arbitrary interconnection structures.

The method of [17] has been adapted to solve for unforced periodic solutions in one-port circuits composed of the *difference* of monotone elements by Das, Chaffey and Sepulchre [38]. Such circuits include the van der Pol and FitzHugh–Nagumo oscillators. An interesting avenue for future work

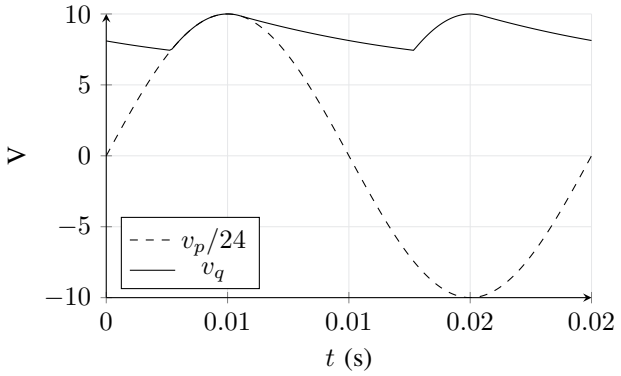

Fig. 7. Input voltage v_p and output voltage v_q for the filtered bridge rectifier of Figure 4, computed using the Condat–Vũ algorithm. Circuit parameters are $R = 1 \times 10^3\,\Omega$ and $C = 10\,\mu$F, algorithm parameters are $\Delta t = 1 \times 10^{-4}$ s (200 samples) and step sizes of $\tau = \sigma = 0.005$.

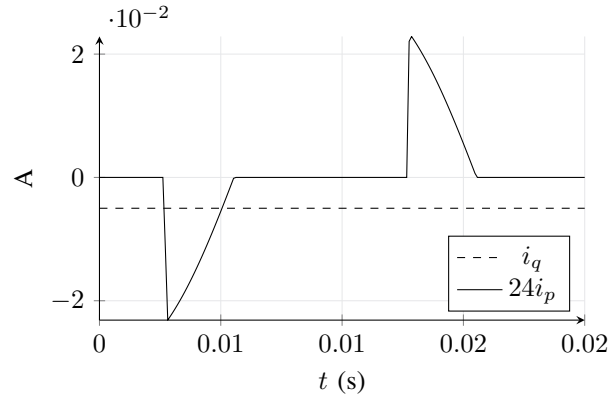

Fig. 8. Input current i_q and output current i_p for the filtered bridge rectifier of Figure 4. Algorithm and circuit parameters as for Figure 7.

is to extend the the skew+monotone method we present here in a similar manner, to differences of monotone m-port circuits. A second avenue for future research is the extension to circuits containing active components, such as ideal operational amplifiers.

A final question for future is whether the monotone+skew form of a nonlinear circuit allows for algorithmic solutions to problems other than operator inversion or simulation. For example, are there optimal control problems that can be solved using a splitting method similar to that used in this paper?

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