Yicong (Bryce) Chen

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EDUCATION

University of Washington — Seattle, WA
Ph.D. in Electrical & Computer Engineering — *Sep. 2024 – Present*
- Advisor: Mari Ostendorf

University of Wisconsin-Madison — Madison, WI
B.S. in Computer Engineering: Machine Learning and Data Science — *Sep. 2020 – May 2024*
B.S. in Computer Science
- Advisor: Kangwook Lee
- GPA: 3.98/4.00

RESEARCH INTEREST

My current research has two threads: (1) modeling and evaluating speech behavioral signals, with an emphasis on pausing and prosody as representations for child speech disorder screening; and (2) alignment, generalization, and controllable generation in **multimodal foundation models** involving speech, text, and image modalities. Prior to this, I have also worked on continual federated learning, image generation, and in-context learning.

EXPERIENCE

Research Assistant — Sep. 2024 – Present
Advisor: Mari Ostendorf — *Seattle, WA*
- Developed an evaluation pipeline for an automated sentence recall screener for child speech language disorders.
- Designed and assessed pause-based screening features (pause rate, duration, atypicality) using multiple ASR models, alignment tools, and **speech LLMs** (Qwen-audio, Phi-4), with age-normalized standard scores showing correlations between pause typicality and clinical screening outcomes.
- (In progress) LLM-based typical pause pattern modeling: leading a project to **finetune Qwen3** on pause labels derived from **forced alignment** to predict likely pause positions, derive pause atypicality scores from token-level perplexities, and benchmark them for automatic detection of atypical child speech patterns.

Undergraduate Researcher — May 2022 – May 2024
Advisor: Kangwook Lee — *Madison, WI*
- Established a benchmark to evaluate the **in-context learning** capabilities of **Multimodal** Large Language Models (MLLMs) for mapping text inputs to image outputs.
- Introduced **coded prompts**, inspired by coding theory, to process multiple inputs simultaneously in large language models (LLMs), enhancing task performance.
- Designed a novel algorithm that mitigates forgetting by leveraging aggregated buffer gradients, ensuring the retention of prior knowledge across clients in **Continual Federated Learning (CFL)**.
- Developed a zero-shot technique to improve **CLIP's object counting** accuracy by extracting a counting-specific vector from its text embedding space, improving both counting tasks and **text-to-image generation**.
- Enhanced the efficacy of Mixed Sample Data Augmentation (MSDA) by introducing self-distillation for relabeling, providing more accurate labels for the mixed samples in MSDA.
- Enhanced low-resolution cosmic data into high-resolution images using diffusion to aid dark matter research.

Undergraduate Researcher — Jan. 2022 – May 2022
Advisor: Dane Morgan — *Madison, WI*
- Accelerated molecular machine learning by integrating nystroem into the kernel training process with Faber–Christensen–Huang–Lilienfeld (FCHL) representation and kernel ridge regression.

Publications

[1] Can MLLMs Perform Text-to-Image In-Context Learning?
Yuchen Zeng*, Wonjun Kang*, **Yicong Chen**, Hyung Il Koo, Kangwook Lee
Conference on Language Modeling (COLM) 2024

[2] Zero-shot Improvement of Object Counting with CLIP
Ruisu Zhang*, **Yicong Chen***, Kangwook Lee
Robustness of Few-shot and Zero-shot Learning in Foundation Models (R0-FoMo) Workshop @ NeurIPS 2023

[3] Coded Prompts for Large Language Models
Ziqian Lin, **Yicong Chen**, Yuchen Zeng, Kangwook Lee
Robustness of Few-shot and Zero-shot Learning in Foundation Models (R0-FoMo) Workshop @ NeurIPS 2023

[4] FedGP: Buffer-based Gradient Projection for Continual Federated Learning
Shenghong Dai, **Yicong Chen**, Jy-yong Sohn, S M Iftekharul Alam, Ravikumar Balakrishnan, Suman Banerjee, Nageen Himayat, Kangwook Lee
Federated Learning Systems (FLSys) Workshop @ MLSys 2023 • Oral Presentation • Best Paper Award

Projects

Run Right: Mobile App Design for Personal Running Coach Spring 2024
- Developed a mobile app using TensorFlow MoveNet to analyze running form via smartphone video.
- Enabled users to capture video, receive detailed feedback, and improve running mechanics through an intuitive interface, helping reduce injury risk and enhance running efficiency.

WISC-SP23 architecture microprocessor design Spring 2023
- Designed and implemented a 16-bit, 5-stage pipelined processor (WISC-SP23) using Verilog.
- Developed a two-way set associative instruction cache, a multi-cycle main memory, and other optimizations.

Skills

Languages: Python, Java, C++, C, MATLAB, Verilog, HTML/CSS, JavaScript
Tools: Latex, Wandb, AWS, Git, Docker, Google Cloud
Libraries: PyTorch, TensorFlow, Hugging Face, Scikit-learn, Pandas, NumPy, Matplotlib