Theoretical Analysis of RF-DC Conversion Efficiency for Class-F Rectifiers

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***Abstract*—In this paper, an analytical model for the Class-F rectifier RF-dc conversion efficiency is presented. This model analyzes each kind of diode power losses in the rectifier due to the diode series resistor, junction capacitor, built-in potential, and breakdown voltage based on the time-domain diode voltage and current waveforms. The model provides a simple calculation routine to determine the threshold input power at which the peak reverse voltage across the diode starts to exceed the diode breakdown voltage and cause the diode efficiency to decrease. Two sets of closed-form equations are derived to calculate the Class-F rectifier efficiency in the input power region where the input power is either smaller or larger than the determined threshold input power, respectively. The implementation of a MATLAB code for the model calculation is also presented. Using this tool, the diode efficiency in Class-F rectifiers of different diode parameters can be easily determined, which provides a useful guideline for the optimal diode selection in various applications. The calculated diode efficiency using this model is compared with the Class-F rectifier ADS simulation at different load conditions, and all the results agree well with the model. To verify the model at different frequencies, two Class-F rectifiers working at 900 MHz and 5.8 GHz, respectively, are designed with the highest measured efficiency of 80.4% for the 900-MHz rectifier and 79.5% for the 5.8-GHz rectifier. Both of the measurement results agree well with the model prediction, which further verified the accuracy of the proposed model.**

***Index Terms*—Conversion efficiency, harmonic analysis, rectifiers, Schottky diodes.**

I. Introduction

MICROWAVE power transmission (MPT) is a promising technology and has potential applications where the power transmission through wires is inconvenient or impossible. Modern applications of the MPT system include high-power solar-power satellites (SPSs) [1] and low-power RF energy harvesters [2]. An MPT system usually consists of a microwave generator, a transmitting antenna or array, a receiving antenna or array, a microwave rectifier and a power management unit. To minimize the power loss during the power transmission, the total MPT system efficiency, which is largely determined by the RF-dc conversion efficiency of the microwave rectifier, must be as high as possible. Therefore, the optimal design of a high-efficiency microwave rectifier is crucial to improve the whole MPT system performance.

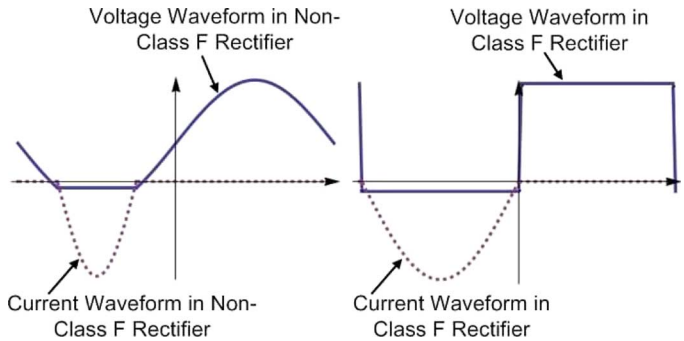

Fig. 1. Diode voltage and current waveforms in non-Class-F rectifier (*left*) and Class-F rectifier (*right*).

Harmonic termination techniques, such as Class-F harmonic termination, are widely used in power amplifier designs to boost its efficiency [3]. In a high-efficiency Class-F power amplifier, the harmonic termination circuit with low impedance at even harmonics and high impedance at odd harmonics is used to shape the current and voltage waveforms across the transistor to minimize their overlap and improve the circuit efficiency. In a microwave rectifier, the nonlinear rectifying diode also generates current and voltage at the harmonics of the operating frequency [4]. Using the same principle as the power amplifier, the rectifier conversion efficiency can also be improved by terminating its harmonic components across the diode. The use of Class-F harmonic termination network theoretically presents the diode with zero impedance at even harmonics and infinite impedance at odd harmonics, which will shape the current waveform to half sine wave and voltage waveform to square wave (the ideal diode current and voltage waveforms in the Class-F rectifier are shown in Fig. 1). With this wave-shaping mechanism, the overlap of voltage and current waveforms is minimized and the rectifier efficiency is thus improved. Some of the reported high conversion efficiency Class-F rectifiers are 77.9% at 2.45 GHz [5] and 65.6% at 24 GHz [6].

The microwave rectifier RF-dc conversion efficiency (η) is defined as the ratio of the rectified dc output power and the RF incident power as follows:

$$\eta = \frac{\text{DC output power}}{\text{RF input power}} = \frac{P_{\text{DC}}}{P_{\text{RF}}}. \tag{1}$$

Manuscript received September 06, 2013; revised December 19, 2013; accepted December 20, 2013. Date of publication January 14, 2014; date of current version April 02, 2014.

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Digital Object Identifier 10.1109/TMTT.2014.2298368

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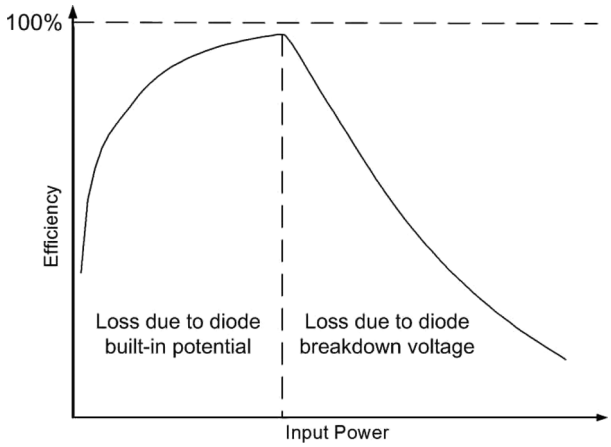

Fig. 2. General microwave rectifier conversion efficiency at different input power levels.

The rectifier conversion efficiency is determined by the diode loss, the impedance mismatch loss, and the substrate and conductor loss in the printed circuit board (PCB), where the diode loss dominates among all the losses. For a well-matched rectifier fabricated on a low-loss PCB, the rectifier conversion efficiency is approximately equal to its diode efficiency (η_D). Fig. 2 shows a general microwave rectifier conversion efficiency curve at different input power, where the efficiency firstly increases monotonically to its maximum value at a specific input power level and then decreases as the input power becomes larger. This change of the rectifier conversion efficiency can be observed in some reported work [7], [8]. The diode efficiency change at the low input power region and the high input power region are caused by the following two different mechanisms, respectively,

- loss due to forward diode build-in potential ($V_{\rm bi}$) in the low input power region;
- loss due to diode breakdown voltage ($V_{\rm br}$) in the high input power region.

When the input power is low, the diode dc reverse bias voltage (V_0), which is introduced by the rectifier load resistor voltage along the dc path, is smaller than or comparable with $V_{\rm bi}$. V_0, as the dc component of diode voltage, is equal to the load dc voltage. The diode efficiency loss due to the $V_{\rm bi}$ can be approximated by (2) as follows [9]:

$$\text{Diode Loss} = \frac{V_{\rm bi}}{V_0 + V_{\rm bi}}. \tag{2}$$

In this case, the calculated diode efficiency loss is from 0.5 to 1, which results in a total rectifier conversion efficiency less than 50%. When the input power increases, V_0 increases as well, then the diode efficiency loss in (2) decreases. The conversion efficiency is thus improved, as shown in Fig. 2, and a theoretical maximum efficiency of 100% can be achieved if the input power is approaching infinite.

However, when the input power is high, the reverse peak voltage across the diode will exceed the diode breakdown voltage. In this situation, a large amount of current will pass through the diode, causing a significant loss in the dc output power. Therefore, the resultant conversion efficiency is greatly decreased, as presented in Fig. 2.

In [7], an analytical model for rectifier conversion efficiency was proposed with good agreement to measurement results, in which the ideal sinusoidal diode voltage waveform is assumed with the voltage clamped by the diode built-in potential during the turn on time (shown on the left-hand side of Fig. 1). Also, in [10], an analytical model for rectifier conversion efficiency in both low input power and high input power regions was proposed with good agreement to measurement results when the diode is working in the region with diode voltage larger than the breakdown voltage, where the similar diode voltage waveform assumption is used. However, this assumption of diode voltage waveform is only proper when no specific harmonic termination is applied to the diode in rectifier. In the case of the Class-F rectifier, the voltage and current waveforms across the diode are shaped to be square wave and half sine wave due to the zero impedance at even harmonics and infinite impedance at odd harmonics in the harmonic termination network (shown in the right of Fig. 1), where the waveforms of Class-F and non-harmonic terminated rectifiers are quite different. Therefore, an analytical model specifically based on the diode voltage and current waveforms in the Class-F rectifier is needed to include the wave-shaping effects on the diode efficiency.

A preliminary work has shown a theoretical analysis for Class-F rectifiers in the low-power region only [11], where the effect of diode breakdown voltage is not included. This work extends the analysis to accurately predict the Class-F rectifier conversion efficiency both in low input power and high input power regions (including diode breakdown voltage effect), as well as a detailed analysis on the load effects, frequency effects, and other circuit loss effects on the rectifier efficiency. An analytical model specifically based on the time domain of the Class-F voltage and current waveform analysis is presented in this paper. Two groups of closed-form equations are presented in this paper for diode efficiency calculation in the low input power and high input power regions, respectively. These nonlinear equations can be solved using the MATLAB software, in which the implementation is presented step by step. Using this code, the diode efficiency in different Class-F rectifier designs can be easily determined, which gives a useful guideline for the optimal diode selection in different applications. Two Class-F rectifiers working at 900 MHz and 5.8 GHz are then designed and fabricated to verify the model calculation.

II. Class-F Rectifier Efficiency Analysis

The single shunt diode Class-F rectifier topology is used in the model analysis of this work (shown in Fig. 3), which consists of matching network, harmonic termination network, rectifying diode, RF choke, and resistive load.

The diode equivalent circuit used in this analysis is also shown in Fig. 3, which consists of a series resistor (R_S), a nonlinear junction resistor (R_j), and a nonlinear junction capacitor (C_j). The nonlinear capacitance of C_j can be calculated using (3) as follows:

$$C_j = C_{j0}\left(1 - \frac{V_0}{V_{\rm bi}}\right)^{-M} \tag{3}$$

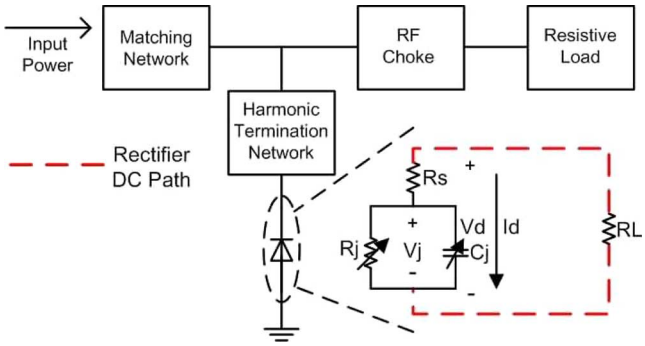

Fig. 3. Circuit topology of the Class-F rectifier.

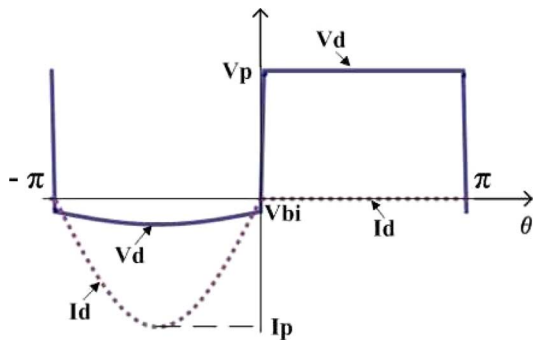

Fig. 4. Assumed diode voltage and current waveforms in the low input power region.

where C_{j0} is the diode zero-bias junction capacitance; V_0 is the diode reverse bias voltage; $V_{\rm bi}$ is the diode built-in potential, and M is the diode grading coefficient.

A. Diode Efficiency Analysis in Low Input Power Region

The analysis assumes an ideal Class-F termination network up to infinite harmonics, which gives a perfect square voltage waveform and a half sine current waveform in time domain across the diode junction. When the input power is low, the reverse peak voltage on the diode is less than the diode breakdown voltage. In this case, the diode efficiency is derived with the assumed diode voltage (V_d) and current (I_d) waveforms shown in Fig. 4 and explicitly expressed in (4) and (5). V_d is the summation of the diode junction voltage (V_j) and the voltage on R_S (V_{R_s}), where the V_j is limited to $V_{\rm bi}$ during the diode ON period (from $-\pi$ to 0) and V_{R_s} can be calculated by $V_{R_S} = I_d \cdot R_S$,

$$V_d = \begin{cases} -V_{\rm bi} + I_P R_S \sin(\theta), & -\pi < \theta < 0 \\ V_P, & 0 < \theta < \pi \end{cases} \tag{4}$$

$$I_d = \begin{cases} I_P \sin(\theta), & -\pi < \theta < 0 \\ 0, & 0 < \theta < \pi. \end{cases} \tag{5}$$

The dc components of the voltage and current across the diode during one period (V_0 and I_0) can be calculated using (6) and (7) as follows:

$$V_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_d \, d\theta = \frac{-2I_P R_S - \pi V_{\rm bi} + \pi V_P}{2\pi} \tag{6}$$

$$I_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_d \, d\theta = -\frac{I_P}{\pi}. \tag{7}$$

The analysis along the dc path (the dashed line in Fig. 3) shows that load resistor has the same dc voltage and the opposite dc current as that of the diode. The load resistance and the dc output power can then be related to the diode dc voltage and current using (8) and (9) as follows:

$$R_L = -\frac{V_0}{I_0} = \frac{-2I_P R_S - \pi V_{\rm bi} + \pi V_P}{2I_P} \tag{8}$$

$$P_{\rm OUT} = -V_0 I_0 = \frac{I_P(-2I_P R_S - \pi V_{\rm bi} + \pi V_P)}{2\pi^2}. \tag{9}$$

The diode loss is mainly introduced by the diode parameters of C_j, R_S, and $V_{\rm bi}$. In the voltage waveform transition region (at $\theta = 0$ and $\theta = \pi$ in Fig. 4), the diode losses are caused by the voltage and current overlap on the diode junction and on R_S, as the voltage across C_j changes dramatically. At the voltage rising edge ($\theta = 0$ in Fig. 4), the power loss on the diode junction can be calculated using (10)–(12), where f is the rectifier operating frequency and δ is the Dirac delta function,

$$V_d|_{t=0} = \frac{1}{2}(V_d|_{t=0^-} + V_d|_{t=0^+}) = \frac{\Delta V}{2} = \frac{V_P}{2} \tag{10}$$

$$I_d|_{t=0} = C_j \frac{dV_d}{dt}|_{t=0} = C_j \Delta V \delta(t-0) = C_j V_P \delta(t-0) \tag{11}$$

$$P_{{\rm LOSS},C_j 1} = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_d I_d \, d\theta = \frac{1}{2} f C_j V_P^2. \tag{12}$$

Similarly, at the voltage falling edge ($\theta = \pi$ in Fig. 4), the power loss on the diode junction has the same magnitude, but with opposite sign. This result indicates that the total power losses on the diode junction due to C_j are canceled at the two transition periods. However, the power losses on R_S due to C_j at voltage rising and falling edges are not canceled. To calculate this loss, the ratio α of rising and falling time with respect to half the period has to be assumed. The loss on R_S can then be calculated using (13) by integrating it at both transition edges,

$$\begin{aligned} P_{{\rm LOSS},C_j 2} &= \frac{1}{2\pi}\int_0^{\alpha\pi} \left(C_j \frac{dV_d}{d\theta}\frac{d\theta}{dt}\right)^2 R_S \, d\theta \\ &\quad + \frac{1}{2\pi}\int_{(1-\alpha)\pi}^{\pi} \left(C_j \frac{dV_d}{d\theta}\frac{d\theta}{dt}\right)^2 R_S \, d\theta \\ &= \frac{4f^2 C_j^2 V_P^2 R_S}{\alpha}. \end{aligned} \tag{13}$$

The diode loss due to R_S and $V_{\rm bi}$ during the ON period can be calculated by integrating the instantaneous voltage and current across the diode over that time using (14) as follows:

$$P_{{\rm LOSS},R_S,V_{\rm bi}} = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_d I_d \, d\theta = \frac{I_P(I_P \pi R_S + 4V_{\rm bi})}{4\pi}. \tag{14}$$

The diode efficiency in the low input power region can first be calculated by its definition as the ratio of the dc output power to the RF input power using (15) as follows:

$$\eta = \frac{P_{\rm OUT}}{P_{\rm IN}} = \frac{I_P(-2I_P R_S - \pi V_{\rm bi} + \pi V_P)}{2\pi^2 P_{\rm IN}}. \tag{15}$$

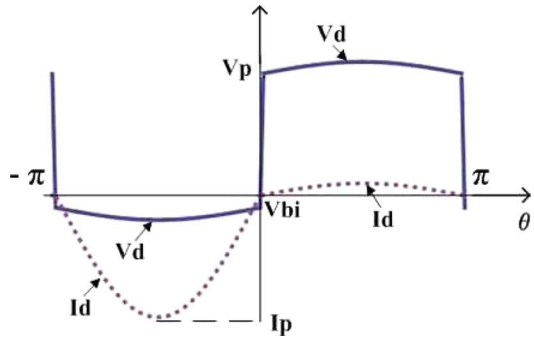

Fig. 5. Assumed diode voltage and current waveforms in the high input power region.

As the total input power is equivalent to the summation of the rectified dc power and the diode power loss, the diode efficiency can also be calculated using (16), shown at the bottom of this page.

For a specific rectifier, C_{j0}, R_S, and $V_{\rm bi}$ are the diode parameters provided by the device manufacturer; R_L, $P_{\rm IN}$, and f are the rectifier design parameters specified by the designer; and α is assumed to be 0.1 in this work according to experience. Therefore, by calculating (8), (15), and (16) simultaneously, the three unknowns of diode efficiency (η), V_P and I_P can be solved. Using these equations, the diode efficiency of different diode parameters in the low input power region can be determined.

The input power level at which the diode efficiency reaches its highest point can also be determined using these equations. In this case, $P_{\rm IN}$ (the input power level at which the diode efficiency starts to decrease) becomes the unknown variable and V_P is equal to $V_{\rm br}$, which indicates the reverse diode voltage amplitude reaches the diode breakdown voltage. Similarly, by calculating (8), (15), and (16), the three unknowns of diode efficiency (η), $P_{\rm IN}$ and I_P can be solved, where $P_{\rm IN}$ represents the input power level for the highest diode efficiency.

B. Diode Efficiency Analysis in High Input Power Region

When the input power is large and the diode reverse voltage goes beyond the diode breakdown voltage during the OFF period (from 0 to π), the diode efficiency starts to decrease due to the significant power loss in breakdown period. When the reverse voltage exceeds the diode breakdown voltage, the diode junction resistance R_j decreases quickly and the reverse current increases. In this situation, the diode voltage and current waveforms in the diode OFF period deviate from those in the ideal Class-F operation (as shown in Fig. 5), which are explicitly expressed in (17) and (18). To make a distinction of this derivation from that in Section II-A, all the notations in this section are marked with additional br subscripts,

$$V_{d\_\rm br} = \begin{cases} -V_{\rm bi} + I_P R_S \sin(\theta), & -\pi < \theta < 0 \\ V_{\rm br} + I_R R_S \sin(\theta), & 0 < \theta < \pi \end{cases} \tag{17}$$

$$I_{d\_\rm br} = \begin{cases} I_P \sin(\theta), & -\pi < \theta < 0 \\ I_R \sin(\theta), & 0 < \theta < \pi. \end{cases} \tag{18}$$

With this assumption, the dc components of the voltage and current across the diode during one period ($V_{0\_\rm br}$ and $I_{0\_\rm br}$) can be calculated using (19) and (20) as follows:

$$V_{0\_\rm br} = \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{d\_\rm br}\, d\theta = \frac{-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br}}{2\pi} \tag{19}$$

$$I_{0\_\rm br} = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_{d\_\rm br}\, d\theta = -\frac{I_P - I_R}{\pi}. \tag{20}$$

The relationships between the load resistance and the dc output power and the dc voltage and current are similar to that in Section II-A, which are expressed in (21) and (22) as follows:

$$\begin{aligned} R_{L\_\rm br} &= -\frac{V_{0\_\rm br}}{I_{0\_\rm br}} \\ &= \frac{-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br}}{2(I_P - I_R)} \end{aligned} \tag{21}$$

$$\begin{aligned} P_{\rm OUT\_br} &= -V_{0\_\rm br} I_{0\_\rm br} \\ &= \frac{(I_P - I_R)(-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br})}{2\pi^2}. \end{aligned} \tag{22}$$

Also, similar to the derivation in Section II-A, the power losses on the diode junction at the two transition periods are zero since the losses at the rising and falling edge cancel out each other. The power loss on R_S due to the current induced by C_j can be calculated by (23) as follows:

$$\begin{aligned} P_{\rm LOSS\_br,C_j} &= \frac{1}{2\pi}\int_0^{\alpha\pi}\left(C_j\frac{dV_d}{d\theta}\frac{d\theta}{dt}\right)^2 R_S\, d\theta \\ &\quad + \frac{1}{2\pi}\int_{(1-\alpha)\pi}^{\pi}\left(C_j\frac{dV_d}{d\theta}\frac{d\theta}{dt}\right)^2 R_S\, d\theta \\ &= \frac{4f^2 C_j^2 V_{\rm br}^2 R_S}{\alpha}. \end{aligned} \tag{23}$$

The diode loss during one period due to R_S and $V_{\rm bi}$ can be calculated by integrating the instantaneous voltage and current across the diode in both the diode ON and OFF period using (24) as follows:

$$\begin{aligned} P_{\rm LOSS\_br,R_S,V_{bi}} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} V_{d\_\rm br} I_{d\_\rm br}\, d\theta \\ &= \frac{I_P^2\pi R_S + I_R^2\pi R_S + 4I_P V_{\rm bi} + 4I_R V_{\rm br}}{4\pi}. \end{aligned} \tag{24}$$

The diode efficiency in the high input power region can first be calculated by its definition as the ratio of the dc output power to the RF input power using (25) as follows:

$$\begin{aligned} \eta\_\rm br &= \frac{P_{\rm OUT\_br}}{P_{\rm IN}} \\ &= \frac{(I_P - I_R)(-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br})}{2\pi^2 P_{\rm IN}}. \end{aligned} \tag{25}$$

$$\eta = \frac{P_{\rm OUT}}{P_{\rm OUT} + P_{{\rm LOSS},C_j} + P_{{\rm LOSS},R_S,V_{\rm bi}}} = \frac{2I_P(-2I_P R_S - \pi V_{\rm bi} + \pi V_P)}{2I_P(-2I_P R_S - \pi V_{\rm bi} + \pi V_P) + \pi I_P(I_P \pi R_S + 4V_{\rm bi}) + \frac{16\pi^2 f^2 C_j^2 V_P^2 R_S}{\alpha}} \tag{16}$$

As the total input power is equivalent to the summation of the rectified dc power and the diode power loss, the diode efficiency can also be calculated using (26), shown at the bottom of this page.

As explained in Section II-A, the diode parameters of C_j, R_S, $V_{\rm bi}$, and $V_{\rm br}$ and the rectifier parameters of R_L, $P_{\rm IN}$, f, and α are all the known variables and can be easily acquired. By calculating (21), (25), and (26) simultaneously, the three unknowns of diode efficiency (η_br) in the high input power region, I_P and I_R can be solved. Using these equations, the diode efficiency of different diode parameters in the high input power region can be determined. Use the equations in Sections II-A and II-B, the diode efficiency at both low and high input power can be obtained.

III. Model Calculation and Simulation Comparison

MATLAB software is used to solve the group of nonlinear equations in the proposed model. The algorithm of the MATLAB implementation is as follows.

1) Input the diode parameters of C_{j0}, R_S, $V_{\rm bi}$, and $V_{\rm br}$, and the rectifier parameters of R_L, $P_{\rm IN}$, and f into the program.
2) Calculate the input power level at which the diode reverse voltage goes beyond the diode breakdown voltage causing the rectifier efficiency to decrease, using the equations in Section II-A.
3) Calculate the rectifier efficiency in the low input power region and high input power region, respectively, using equations described in Sections II-A and II-B.
4) Combine the rectifier efficiency at different input power levels to get the complete rectifier conversion efficiency curve with respect to input power.

The diode efficiency analysis and model calculation show that the theoretically highest diode efficiency can be achieved with a diode of low R_S, low $V_{\rm bi}$, low C_{j0}, and high $V_{\rm br}$. In practice, to simultaneously obtain the optimal value of all these diode parameters is difficult due to the limitation in device material and fabrication. This tradeoffs among different diode parameters have to be carefully designed. Due to the complicated nonlinear relationship between the diode parameters and the diode efficiency, finding the optimal diode in different applications requires a lot of effort to conduct different Class-F rectifier simulations for each specific diode.

The proposed model allows one to investigate the contribution of each diode parameter to the diode efficiency, thus provides a guideline for engineers to choose the optimal diode for high-efficiency Class-F rectification at RF and microwave frequencies. A commercially available Avago HSMS8202 Schottky diode is studied here in the Class-F rectifier with

TABLE I
Diode Parameters of Different Diode Types

Diode Type	$R_S(\Omega)$	$V_{bi}(V)$	$C_{j0}(pF)$	$V_{br}(V)$
Ideal Diode	0	0	0	7.3
HSMS8202 Diode	6	0.5	0.18	7.3
Non-ideal R_S Diode	6	0	0	7.3
Non-ideal V_{bi} Diode	0	0.5	0	7.3
Non-ideal C_{j0} Diode	0	0	0.18	7.3

$R_L = 510\ \Omega$ and $f = 900$ MHz to understand how its diode parameters (R_s, C_{j0}, $V_{\rm bi}$, and $V_{\rm br}$) affect the diode efficiency. Each time one particular diode parameter is kept at its practical value in the given model while the other parameters are set to zero to exclude the effects of these parameters to the diode efficiency. The breakdown voltage is always kept at its practical value for all comparisons here, which guarantees that the efficiency drop at the high input power level is maintained. These different setups are summarized in Table I.

The efficiency of the nonideal R_S diode is shown in blue in Fig. 6(in online version) together with the ideal diode efficiency and the practical HSMS8202 diode efficiency for reference. Comparing the ideal diode efficiency and nonideal R_S diode efficiency curves, the contribution of R_S to the total diode efficiency decrease is relatively steady in all the input power range. The influence of $V_{\rm bi}$ on diode efficiency can be determined by the efficiency decrease between the ideal diode and the nonideal $V_{\rm bi}$ diode [shown in green in Fig. 6 (in online version)]. The diode loss caused by $V_{\rm bi}$ is dependent on the input power: at low input power, its contribution to the diode efficiency decrease is large; at high input power, this diode loss becomes smaller. This observation is consistent with the previous discussion using (2). C_{j0} alone contributes no power loss on the diode efficiency as the pink line (in online version) coincides with the black line (shown in Fig. 6). This is because when the diode parameters of R_S and $V_{\rm bi}$ are ideal, the junction capacitor itself is purely capacitive and introduces no power loss. However, the small value of C_{j0} is still desired, especially when the operating frequency is high, as the voltage and current waveform change caused by the C_{j0} does contribute to the power loss when the other diode parameters are not ideal (nonzero R_S and $V_{\rm bi}$). For example, in the 900-MHz rectifier ADS simulation at 20 mW, the efficiency can boost from 78.3% to 79.1% if the diode C_{j0} is set to 0.

The $V_{\rm br}$ influence to the diode efficiency is mainly on its power-handling capability. To investigate this effect, four widely used Schottky diodes: Avago HSMS8202 and HSMS2850, Skyworks SMS1546 and SMS7630, with different diode breakdown voltage, are selected and their major diode

$$\eta\_\mathrm{br} = \frac{P_{\mathrm{OUT\_br}}}{P_{\mathrm{OUT\_br}} + P_{\mathrm{LOSS\_br},C_j} + P_{\mathrm{LOSS\_br},R_S,V_{\rm bi}}} = \frac{2(I_P - I_R)(-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br})}{\pi(I_P^2 \pi R_S + I_R^2 \pi R_S + 4I_P V_{\rm bi} + 4I_R V_{\rm br}) + 2(I_P - I_R)(-2I_P R_S + 2I_R R_S - \pi V_{\rm bi} + \pi V_{\rm br}) + \frac{16\pi^2 f^2 C_j^2 V_{\rm br}^2 R_S}{\alpha}} \quad (26)$$

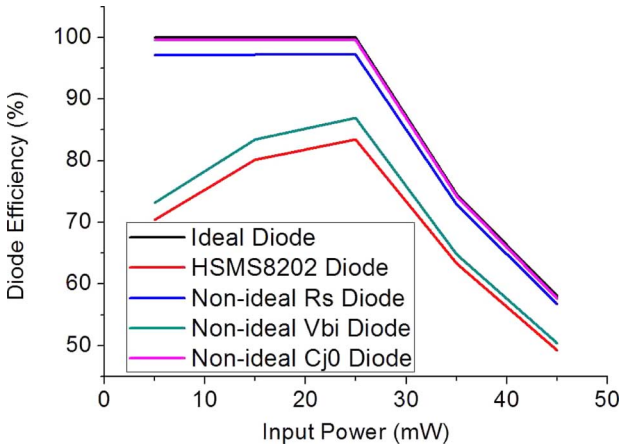

Fig. 6. Calculated diode efficiency in Class-F rectifier with different diode parameters, where the pink line (in online version) and the black line coincide with each other.

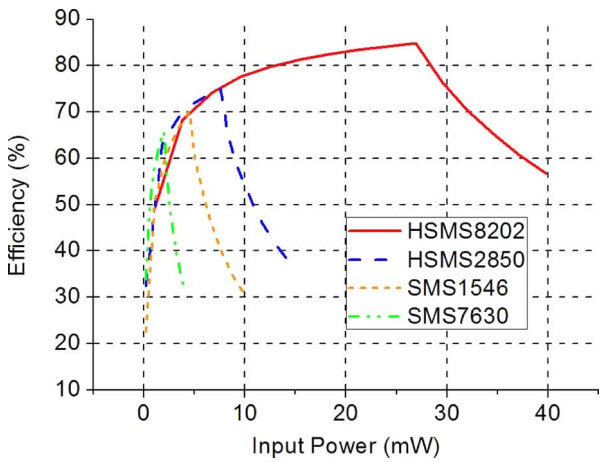

Fig. 7. Calculated diode efficiency in Class-F rectifier using the four selected diodes.

TABLE II
DIODE PARAMETERS OF THE FOUR SCHOTTKY DIODES

Diode Model	$R_S(\Omega)$	$V_{bi}(V)$	$C_{j0}(pF)$	$V_{br}(V)$
HSMS8202	6	0.5	0.18	7.3
HSMS2850	25	0.35	0.18	3.8
SMS1546	4	0.51	0.38	3
SMS7630	20	0.34	0.14	2

parameters are listed in Table II. The diode efficiencies are calculated at the same load condition, where results (shown in Fig. 7) reveal a direct relationship between the diode power handling ability and the $V_{\rm br}$. The efficiency of the diode with a larger $V_{\rm br}$ starts to decrease at a higher input power and vice versa if the resistor remains. In applications where the input power level varies over a wide range, a diode with a large enough $V_{\rm br}$ shall be selected to accommodate the highest possible input power. From the calculation results, one can determine whether the selected diode breakdown voltage is large enough for the Class-F rectifier to avoid the diode efficiency decrease.

Besides the diode breakdown voltage, the rectifier load resistance also has a significant influence on the input power level at

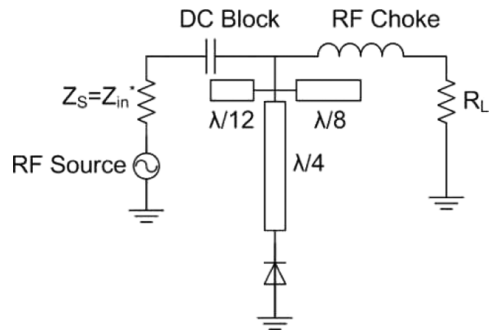

Fig. 8. Ideal Class-F rectifier topology used in circuit design.

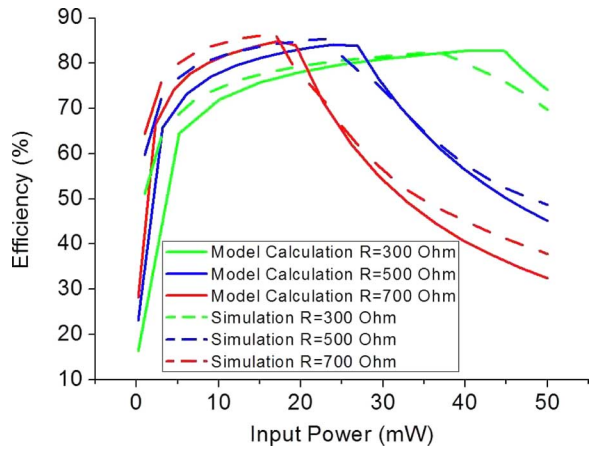

Fig. 9. Calculated and simulated Class-F rectifier efficiency at different load conditions.

which the diode efficiency starts to decrease. To accommodate the same amount of rectified dc output power, a higher resistance load presents a higher dc output voltage, and thus a higher diode dc reverse-bias voltage. Due to the Class-F termination, the voltage waveform is shaped as the square wave, where its dc component is the diode dc reverse-bias voltage and its voltage swing is due to the RF fundamental and its odd harmonics. The larger the reverse bias voltage, the larger the voltage swing across the diode, and the earlier the total reverse voltage (reverse bias voltage + voltage swing) on the diode will reach the diode breakdown voltage. In other words, the diode starts to work in the breakdown region at a lower input power level when the dc load is fixed. A Class-F rectifier is simulated in ADS software at three different load conditions to verify this prediction. This rectifier uses ideal RF choke, ideal dc block, lossless transmission line, and the source impedance is set to be conjugate match to the rectifier input impedance at various input power levels (as shown in Fig. 8). The HSMS8202 diode in ADS simulation uses the same parameters as that in the model calculation, and the simulated and calculated rectifier efficiency at load conditions of 300, 500, and 700 Ω are compared. As shown in Fig. 9, the calculation results agree well the simulation results in both the low input power and high input power regions at all the load conditions. It is clearly indicated that high power rectifiers should have a smaller dc resistor, while low power rectifiers should have a larger dc resistor.

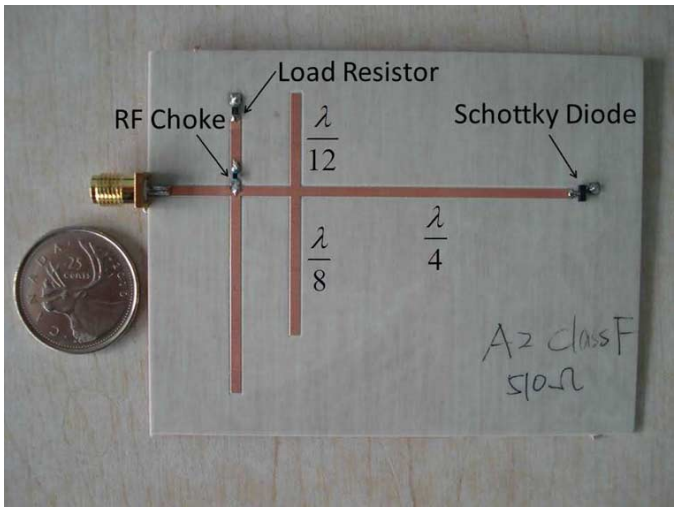

Fig. 10. Photograph of the fabricated 900-MHz Class-F rectifier.

IV. Class-F Rectifier Design and Measurement

To verify the proposed model at different microwave frequencies, two different Class-F rectifiers working at 900 MHz and 5.8 GHz are designed, fabricated, and measured, respectively. Both rectifiers are simulated in ADS and fabricated on the 32-mil-thick RO4003C substrate ($\epsilon = 3.55$). The diode's second and third harmonic components are terminated with $\lambda/8$ and $\lambda/12$ open stub, where the termination of the first two harmonics is enough to maintain the Class-F voltage and current waveforms [9]. These two rectifiers use different Schottky diodes for their optimal operation at each working frequency.

The 900-MHz Class-F rectifier (shown in Fig. 10) uses an Avago HSMS-8202 Schottky diode as the rectifying device, a 510-Ω resistor as the load, and a 470-nH inductor as the RF choke. The simulated time-domain diode voltage and current waveforms are shown in Fig. 11, which exhibits excellent Class-F operation. This rectifier is measured within the input power range from 1 to 45 mW, where the highest measured conversion efficiency is 80.4% at 22 mW. The measurement result agrees well with the model calculation in both low and high input power levels (shown in Fig. 12). The measurement result is a little lower than the proposed model calculation because the measured rectifier efficiency is not only affected by the dominant diode loss calculated by the model, but also by the mismatch loss and ohmic loss from the PCB. To show the difference between the proposed models based on Class-F operation and the model without considering the harmonic effects, the calculation results using the model in [10], which uses the voltage waveform assumption on the left-hand side of Fig. 1, is also presented for comparison. Even though the model in [10] assumes no circuit loss (no mismatch loss and PCB loss, and only diode loss is considered for the rectifier efficiency), the calculation result still gives lower rectifier efficiency compared to the measurement of the Class-F rectifier. This comparison shows that the model in [10] will underestimate the rectifier efficiency when the Class-F harmonic termination is used in the rectifier design. The Class-F rectifier model provides higher efficiency prediction compared to the model in [10], which can be well justified by the efficiency improvement due to the

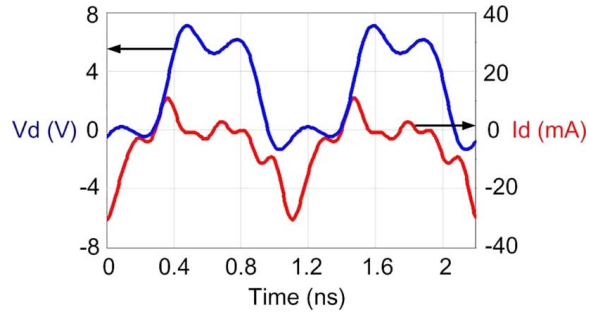

Fig. 11. Simulated diode time-domain voltage and current waveforms of the 900-MHz Class-F rectifier.

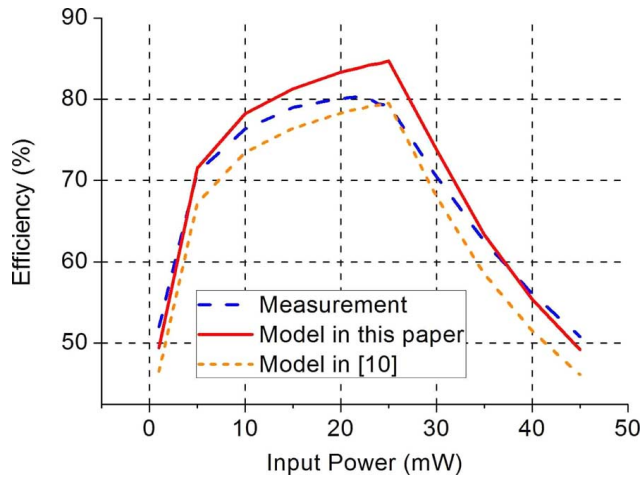

Fig. 12. Comparison of the measured and calculated 900-MHz rectifier conversion efficiency.

Class-F harmonic termination, similar to the high-efficiency Class-F power amplifier.

For the 5.8-GHz Class-F rectifier, the Avago HSMS-8202 Schottky diode is first tried in the ADS simulation, where the diode voltage and current waveforms are presented in Fig. 13. As this diode junction capacitor ($C_{j0} = 0.18$ pF) is relatively large at 5.8 GHz, the current induced by C_{j0} is too large, which severely degrades the waveforms from their ideal square voltage wave and half sine current wave. This overlap of nonzero voltage and current waveforms significantly deteriorates the rectifier efficiency. Therefore, another diode, the M/A-COM MA4E1317 Schottky diode, is used in the 5.8-GHz rectifier design for its low diode junction capacitance ($C_{j0} = 0.02$ pF), which is small enough to maintain the Class-F waveform at the working frequency. Also, as the inductor introduces losses at 5.8 GHz, the RF choke is implemented by a high-impedance microstip line and a quarter-wavelength open stub. The designed 5.8-GHz rectifier is shown in Fig. 14, and its simulated voltage and current waveforms demonstrate excellent Class-F operation at this frequency using the MA4E1317 Schottky diode (shown in Fig. 15). This rectifier is measured within the input power range from 1 to 80 mW, where the highest measured conversion efficiency is 79.5% at 58 mW (shown in Fig. 16).

In both rectifiers, the efficiency difference between the measurement and calculation using the proposed model is mainly

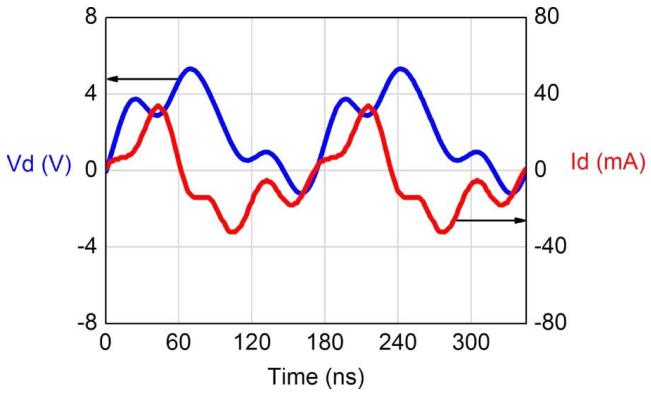

Fig. 13. Simulated HSMS8202 Schottky diode voltage and current waveforms in 5.8-GHz Class-F rectifier.

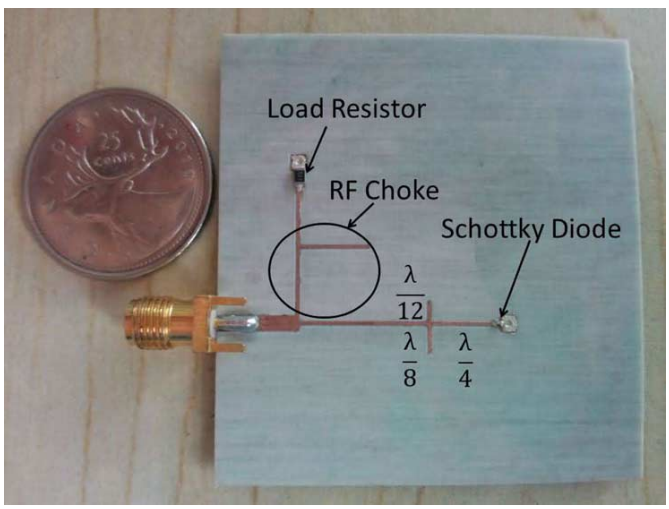

Fig. 14. Photograph of the fabricated 5.8-GHz Class-F rectifier.

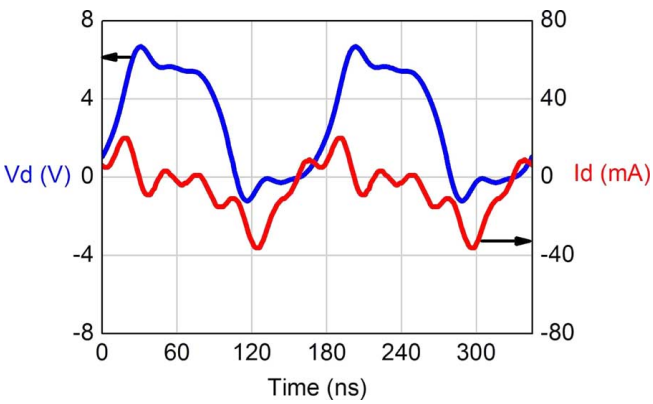

Fig. 15. Simulated MA4E1317 Schottky diode voltage and current waveforms in 5.8-GHz Class-F rectifier.

caused by the minor losses, including the substrate and conductor loss on the PCB and the mismatch loss. The proposed model is meant to study the effects of diode parameters to the conversion efficiency, which gives the upper bound of conversion efficiency for a diode.

For the 900-MHz rectifier, the weight of each power loss is determined from the ADS simulation (shown in Fig. 17). The

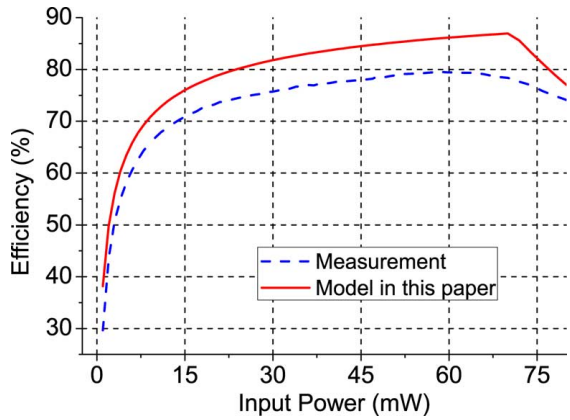

Fig. 16. Comparison of the measured and calculated 5.8-GHz rectifier conversion efficiency.

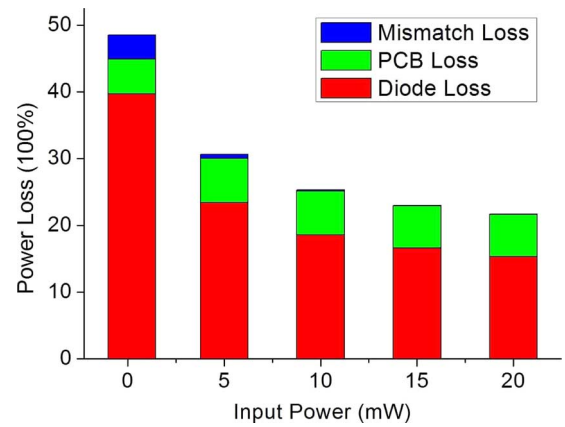

Fig. 17. Simulated weight of each power loss in the 900-MHz rectifier, where Rectifier Efficiency = 1 − Diode Loss − PCB Loss − Mismatch Loss.

diode loss is dependent on the input power and is the dominant loss among all rectifier losses. The diode loss is large when input power is low, and decreases when the input power increases, as explained in (2). The PCB loss is dependent on the board specifications, the circuit operating frequency, as well as circuit geometry, and changes little as the input power changes. For the case of 32-mil-thick RO4003C PCB under 900-MHz input power, the PCB loss causes 5%–6% of the total efficiency decrease. The mismatch loss is dependent on the input power since the rectifier impedance changes with input power. The rectifier matching network is usually designed and optimized at the optimal input power region (in this case, 5–20 mW), where the input power is neither too low that the diode is not completely turned on, nor too high that the diode goes into breakdown. In the 900-MHz rectifier design, the mismatch loss is very low from 5–20 mW, which indicates an excellent circuit impedance match.

For the 5.8-GHz rectifier, the weight of each power loss is presented in Fig. 18. The diode loss in the 5.8-GHz design is larger than that in the 900-MHz rectifier because the diode loss increases as the frequency increases. The PCB loss in the 5.8-GHz design is smaller because the size of the 5.8-GHz circuit is smaller than that of the 900 MHz, which introduces smaller substrate and conductor losses. The mismatch loss is slightly larger

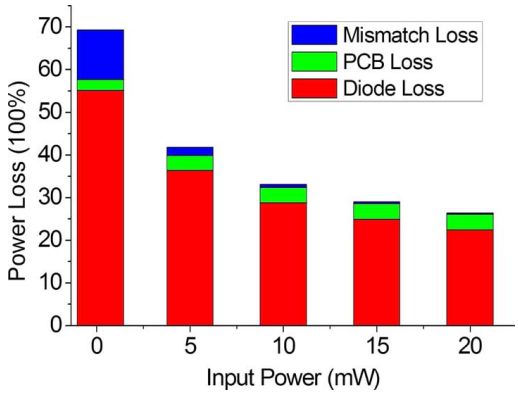

Fig. 18. Simulated weight of each power loss in the 5.8-GHz rectifier, where Rectifier Efficiency = 1 − Diode Loss − PCB Loss − Mismatch Loss.

in the 5.8-GHz rectifier because the matching network at higher frequency is more difficult to design.

V. Conclusion

In this paper, an analytical model has been derived for the diode efficiency calculation in the Class-F rectifiers at both low and high input power regions based on time-domain analysis of the diode voltage and current waveforms. In this model derivation, each of the diode losses is carefully examined. The model calculated diode efficiency agrees well with the ADS simulation at different load conditions. Two Class-F rectifiers are fabricated at different frequency to verify the proposed model. The measurement results agree well with the model calculation at both low and high input power regions.

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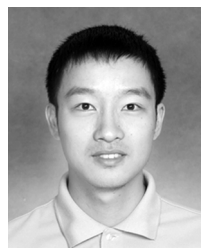

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