Optimization of a 5.8-GHz rectifier considering ripple amplitude and dc-voltage pattern

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Abstract— In this article, several aspects of the rectifier which has not been analyzed in recent rectenna related papers so far are studied. First, dc-voltage pattern is evaluated using oscilloscope and the ripple amplitude of the dc-voltage is calculated. Second, a basis for decision of capacitance as a dc-pass filter is provided, and the measurement result is obtained. Third, impedance matching condition of the rectifier with series configuration is considered and the parasitic cancellation circuits are designed at not only output but also input of the packaged Schottky diode to improve RF-to-DC conversion efficiency and decrease ripple amplitude. The proposed 5.8-GHz rectifier shows RF-to-DC conversion efficiency of 60.6 % at an input power level of 9 dBm and 1.3 kΩ load without dc-pass capacitor with 0.28 % of ripple amplitude.

Keywords - dc-voltage pattern; ripple amplitude; dc-pass capacitor; impedance matching; parasitic cancellation; RF-to-DC conversion efficiency

I. INTRODUCTION

The method using radio frequency among WPT (Wireless Power Transmission) is classified as MPT (Microwave Power Transmission), because it uses microwave frequency bands from L-band to Ka-band. A rectenna which is a system to construct MPT acts as a converter that changes the received RF power to DC power we can use like a battery. There are three reasons that microwave frequency bands are used to design a rectenna for MPT. First, it can have smaller size of system, especially antenna size, than conventional systems operating under L-band. Second, it has low losses due to less absorption and diffusion by air and moisture than losses in millimeter-wave over Ka-band. Third, it is cost effective because of development of microwave technologies when compared to the case for terahertz frequencies. Therefore, there are many research papers related to the rectenna for long distance power transmission at microwave bands, particularly at 2.45 GHz and 5.8 GHz which are among ISM band [1-2].

In recent rectenna papers that are using capacitor as a dc-pass filter, the capacitors have different values of capacitance [3-5], and capacitance values are not indicated for some papers [6-7]. Also, some papers do not use capacitor as a dc-pass filter [8]. Ripple amplitude is the only criterion to estimate dc-pass filter's performance. However, most of rectenna papers do not deal with ripple amplitude even though they use capacitor as a dc-pass filter. Also, they do not show dc voltage pattern and any basis for decision of dc-pass capacitor's value.

In this paper, therefore, we provide a basis for decision of capacitor as a dc-pass filter by calculating input impedance of capacitor, show dc-voltage pattern detected by oscilloscope, and analyze ripple amplitude of rectifier. Also, parasitic cancellation circuit is designed to cancel out not only input but also output parasitic of the packaged Schottky diode, and we provide precautions when impedance matching of rectifier is performed.

II. DESIGN TARGET AND SCHOTTKY DIODE SELECTION

A. 1.5 V supply

Incident power density and effective aperture are calculated as 16.7 mW/cm^2 and 0.24 cm^2 respectively under following conditions by using Friis formula. Power of transmitter fed to the antenna is 0.7 W. Transmitting antenna gain is 16.5 dBi. The distance between the transmitting and the receiving antennas is 1.22 m, and receiving antenna gain is 10.5 dBi. Therefore, received power (P_r) is to be 4.0 mW. If 1.3 kΩ is used as a load resistor (R_L), we need 42.3 % of RF-to-DC conversion efficiency (η_e) to obtain dc-voltage of 1.5 V without loss factors such as impedance mismatch loss and polarization loss.

B. HSMS-286B

ero-bias junction capacitance (C_{j0}) of the Schottky diode is helpful to increase RF-to-DC conversion efficiency. However, reducing C_{j0} causes the decrease of breakdown voltage (V_{br}) and increase of series resistance (R_s) of the diode. These three parameters determine RF-to-DC conversion efficiency of a rectenna and are related with one another owing to the diode material properties [9]. Many of rectenna papers use MA4E1317 as the rectifying diode [4-6, 8]. This diode has a V_{br} of 7 V, R_s of 4 Ω, and C_{j0} of 0.02 pF, while HSMS-286B has a V_{br} of 7 V, R_s of 5 Ω, and C_{j0} of 0.18 pF. HSMS-286B is selected at this work because of its cost-effectiveness.

There are two facts that should be checked after diode selection. First, it is to calculate critical input power that makes breakdown effect become dominant. The equation is given by Eq. (1). Second, it is to calculate diode cutoff frequency (f_c)

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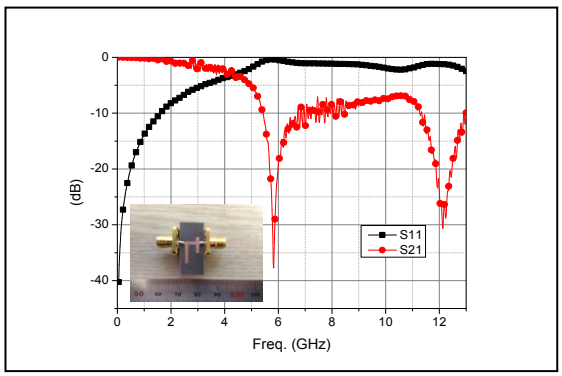

Figure 1. Measured S-parameters for the HSC

which is expressed as Eq. (2) [9]. f_c of HSMS-286B is 147 GHz.

$$\text{Critical Input Power} = \frac{V_{br}^2}{4R_L} \quad (1)$$

$$f_c = \frac{1}{2\pi R_s C_{j0}} \quad (2)$$

In this work, high resistance is needed because dc-voltage is more important issue than η_e, while the resistance is limited by V_{br} of the diode. Therefore, it is desirable to calculate critical input power after determining P_r. As maximum P_r which can be obtained in our rectenna measurement setup is 9 dBm, a load resistor is chosen as 1.3 kΩ. In this case, the critical input power is calculated as 9.7 dBm.

III. Rectifier Design

A. Harmonics Suppression Circuit Design

A fabricated harmonics suppression circuit (HSC) and its measured S-parameters are shown in Fig. 1. It consists of three open stubs: $\lambda_g/4$ at 5.8 GHz, $\lambda_g/4$ at 11.6 GHz, and $\lambda_g/4$ at 23.2 GHz. Table 1 presents EM simulation results and measurement results. From this table, we can recognize that there are resonant frequency shifts of 3rd and 5th harmonics in contrast to the ideal case due to surface wave excitation [10]. Therefore, it is hard to expect that 5th harmonic suppression is to be achieved. After EM simulation is replaced with a S2P file, we apply it to data item in Agilent ADS and then perform rectifier simulation. Simulation results are shown in Table 2.

TABLE I. EM simulation and measurement results of HSC

Freq. [GHz]	S_{21} [dB] Sim.	S_{21} [dB] Meas.	Pertinent Structure
5.8	-36.3	-33.2	$\lambda_g/4$ @ 5.8 GHz
11.6	-24.2	-14.7	$\lambda_g/4$ @ 11.6 GHz
17.4	-16.3	-	$3\lambda_g/4$ @ 17.4 GHz
23.2	-21.9	-	$\lambda_g/4$ @ 23.2 GHz
29.0	-4.2	-	$5\lambda_g/4$ @ 29.0 GHz

B. Impedance Matching & Parasitic Cancellation

Impedance matching (IM) is performed by using Large Signal S-parameters because input power level has the range from 0 dBm to 9 dBm with our measurement system. It is improper that impedance matching is carried out by using small signal S-parameters because input impedance of the diode is changed depending on the input power level. Table 2 shows simulation results of the rectifier with impedance matching circuit. Also, parasitic cancellation is performed at both output and input of the packaged Schottky diode to increase efficiency and reduce ripple amplitude of the rectifier. 50 Ω line which has 5.0 mm of length is added between HSC and the load resistor to cancel out output capacitance of zero bias Schottky diode, and then input capacitive component is also eliminated by adding the same impedance line with 5.5 mm. Simulation results are presented in Table 2. Performances of both efficiency and ripple amplitude are improved after using parasitic cancellation circuit (PCC).

C. DC Block

If a single stub is used as an impedance matching circuit, we have to choose either open stub or short stub. Whatever we select one of two stubs, it needs dc-block when measuring the rectifier. If the short stub is used, current-path for the rectified current is generated through not just short stub but also source resistor, which decreases efficiency of rectifier. If open stub is used with dc block, diode in the series configuration could not work because it does not have any dc current path. For that reason, additional circuit which gives diode dc-path such as $\lambda_g/4$ short stub at 5.8 GHz is necessary. In this work, therefore, we use a short stub for impedance matching to avoid additional circuit, and simulation results of a rectifier with dc block are shown in Table 2. From this table, a rectifier with dc block has higher efficiency and lower ripple amplitude than those of a rectifier without dc block.

D. DC-pass Capacitor

To make capacitor act as a dc-pass filter, it is necessary to use a capacitor with low impedance at harmonic frequencies to shunt harmonics. If an ideal capacitor is used, choosing properly large capacitance is desirable. For example, 100 pF of the capacitor has 0.27 Ω of impedance at 5.8 GHz. However, in real capacitor, the impedance is easy to be large at harmonic frequencies because of its self-resonant frequency (SRF). Moreover, the larger capacitance causes the lower SRF. In this work, therefore, dc-pass capacitor is designed based on impedance of the capacitor. Input impedances of the capacitors such as the ideal 100 pF, 100 pF made by American Technical Ceramics (ATC), and 0.3 pF in parallel with 68 pF made by the same vendor are shown in Table 4, respectively. As it is confirmed that 1st and 2nd harmonics are suitably suppressed from Fig. 1, harmonics beyond 3rd order are considered in designing dc-pass capacitor. Simulation results of rectifiers with dc-pass capacitor and without it are shown in Table 3. The case which is using 0.3 pF in parallel with 68 pF shows lower ripple amplitude than that of the rectifier without the dc-pass capacitor.

TABLE II. SIMULATION RESULTS FOR THE RECTIFIERS

	HSC			HSC+IM			HSC+IM+PCC$_{out}$			HSC+IM+PCC$_{out+in}$			HSC+IM+PCC+DC block		
P_{av} [dBm]	V_{dc} [V]	Eff. [%]	Ripp [%]	V_{dc} [V]	Eff. [%]	Ripp [%]	V_{dc} [V]	Eff. [%]	Ripp [%]	V_{dc} [V]	Eff. [%]	Ripp [%]	V_{dc} [V]	Eff. [%]	Ripp [%]
0	0.56	24.1	7.3	0.79	47.1	5.7	0.8	48.8	2.50	0.81	49.9	2.11	0.86	56.5	1.75
3	0.82	26.0	7.7	1.14	50.3	6.4	1.17	52.6	2.66	1.18	53.1	2.13	1.27	62.4	1.65
6	1.18	26.6	8.1	1.64	51.9	7.2	1.69	55.0	2.67	1.70	55.4	2.54	1.86	66.8	1.88
9	1.65	26.4	8.3	2.35	53.2	8.3	2.42	56.7	3.02	2.45	57.9	3.31	2.66	68.2	3.62

a. HSC (Harmonic Suppression Circuit)
b. IM (Impedance Matching)
c. PCC (Parasitic Cancellation Circuit)

TABLE III. EM SIMULATION AND MEASUREMENT RESULTS OF HSC

Freq. [GHz]	S_{21} [dB] Sim.	S_{21} [dB] Meas.	Pertinent structure
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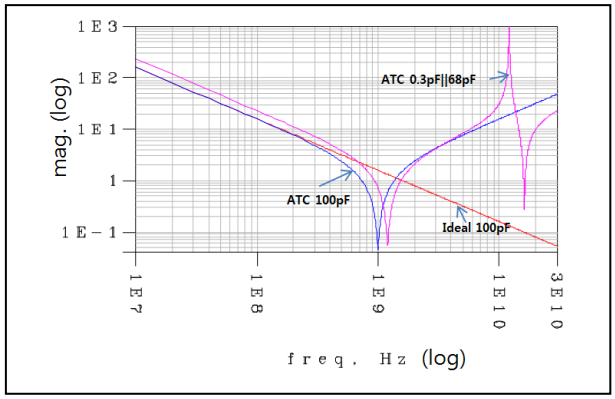

Figure 2. Magnitude of input impedance of three dc-pass capacitors

TABLE V. INPUT IMPEDANCES OF CAPACITORS AT HARMONICS

Freq. [GHz]	$\lvert Z_{ideal\ 100pF}\rvert$ [ohm]	$\lvert Z_{ATC\ 100pF}\rvert$ [ohm]	$\lvert Z_{ATC\ 0.3pF\|68pF}\rvert$ [ohm]
5.8	0.27	9.01	10.20
11.6	0.14	18.44	121.30
17.4	0.09	27.77	4.28
23.2	0.07	37.08	14.84
29.0	0.06	46.38	21.90

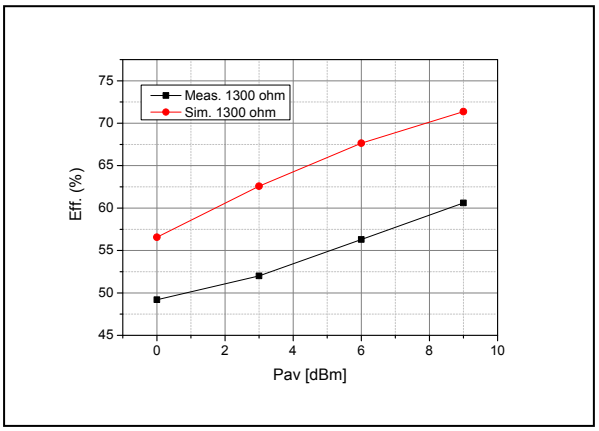

Figure 3. Simulation & measurement redults of RF-to-DC conversion efficiency

TABLE IV. DC PASS FILTERS

Pav [dBm]	Ideal 100.0pF		ATC 100A 100.0pF		ATC 100A 0.3pF||68.0pF		none	
	Eff. [%]	Ripp. [%]	Eff. [%]	Ripp. [%]	Eff. [%]	Ripp. [%]	Eff. [%]	Ripp. [%]
0	57.96	0.12	54.93	4.14	56.56	1.28	56.56	1.75
3	63.91	0.08	61.06	4.38	62.72	1.96	62.57	2.28
6	68.77	0.11	66.88	3.97	67.75	1.92	67.64	2.41
9	72.31	0.07	69.24	6.10	71.44	1.99	71.36	2.36

Fig. 2 shows magnitude of input impedance of three capacitors which are used as a dc-pass filter each in simulation. 0.3 pF parallel with 68.0 pF have lower input impedance than that of 100.0 pF of ATC at higher than 3rd order harmonics because it has the second SRF. Input impedances of capacitors at harmonics are specified in Table 4.

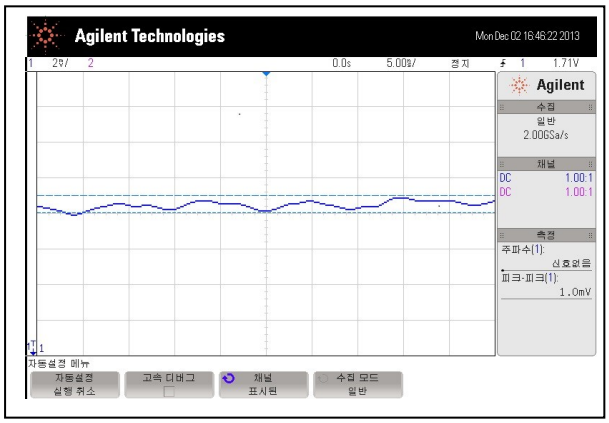

Figure 4. DC voltage pattern at R_L

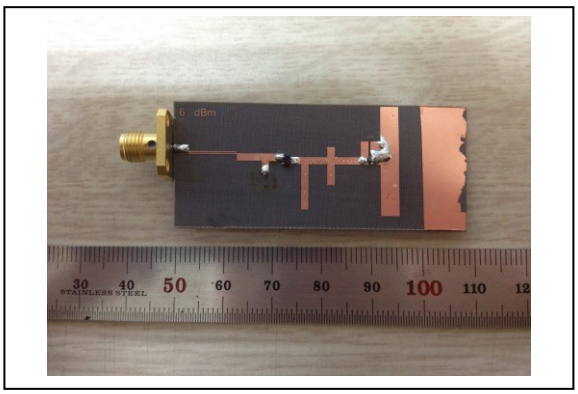

Figure 5. A proposed 6 dBm-rectifier

TABLE VI. MEASURED RESULTS (R_L=1300 Ω)

P_{av} [dBm]	0	3	6	6 0.3pF‖68pF	6 Without dc block	9
V_{dc} [V]	0.80	1.16	1.71	1.01	0.45	2.5
P_{dc} [mW]	0.49	0.94	2.25	0.78	0.16	4.81
Ripp. [%]	0.16	0.14	0.06	0.20	0.51	0.28
Eff. [%]	49.2	52.0	56.3	39.0	4.0	60.6

IV. RECTENNA MEASUREMENT

Measurement results of the rectifier are presented in Table 5, and Fig. 3 shows simulation results through optimization and measurement results of η_e with respect to input power level. 60.6 % efficiency, 2.50 V dc-voltage, and 0.28 % of ripple amplitude are obtained at input power of 9 dBm, and 56.3 % of efficiency, and 1.71 V with 0.06 % of ripple amplitude are achieved at input power of 6 dBm. DC-voltage pattern which is detected by an oscilloscope and the fabricated 6 dBm-rectifier are shown in Fig. 4 and Fig. 5, respectively.

To verify the effect of dc-block, a rectifier with the same structure of 6 dBm-rectifier is measured without dc-block. This rectifier shows 4.0 % of η_e and 0.45 V dc-voltage with 0.51 % of ripple amplitude, and these results are presented in Table 5. Also, the same rectifier above is used to confirm the performance of the dc-capacitor comprised of 0.3 pF parallel with 68.0 pF with dc block. This rectifier shows efficiency of 39.0 %, 1.0 1V dc-voltage, and 0.20 % ripple amplitude. Measured results are indicated in Table 5.

V. CONCLUSIONS

In this work, dc-voltage pattern and ripple amplitude for every fabricated rectifier are confirmed by using oscilloscope. Also, to increase η_e and reduce ripple amplitude, input parasitic cancellation is performed, and it is verified not only that dc-block is necessary when measuring rectifier but also that when using dc-pass capacitor we have to check its performance by inspecting ripple amplitude with oscilloscope compared to that of rectifier before using dc-pass capacitor. We obtain maximum η_e of 60.6 % at input power level of 9 dBm. Also, 56.3 % of η_e and 1.71 V of dc-voltage which has 0.06 % ripple amplitude are achieved at input power level of 6 dBm.

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