5.8-GHz Circularly Polarized Rectifying Antenna for Wireless Microwave Power Transmission

Berndie Strassner, *Student Member, IEEE*, and Kai Chang, *Fellow, IEEE*

***Abstract*—This paper reports a new circularly polarized (CP) high-gain high-efficiency rectifying antenna (rectenna). The CP rectenna can be rotated and still maintain a constant dc output voltage. The high-gain antenna has an advantage of reducing the total number of rectenna elements to cover a fixed area. The rectenna is etched on Rogers Duroid 5870 substrate with $\varepsilon_r = 2.33$ and 10 mil thickness. A high-gain dual-rhombic-loop antenna and a reflecting plane are used to achieve a CP antenna gain of 10.7 dB and a 2 : 1 voltage standing-wave ratio bandwidth of 10%. The rectenna's pattern has an elliptical cross section with orthogonal beamwidths of 40° and 60°. The rectenna circuit has a coplanar stripline band-reject filter that suppresses the re-radiated harmonics by 20 dB. A highly efficient Schottky diode is used for RF-to-dc conversion with an efficiency of approximately 80% for an input power level of 100 mW and a load resistance of 250 Ω.**

***Index Terms*—Circularly polarized antennas, coplanar stripline, microwave power transmission, rectifying antenna, wireless power transmission.**

I. Introduction

THE concept of wireless power transmission (WPT) began over 100 years ago when Tesla successfully lighted two light bulbs from uncollimated radiated energy formed from oscillators operating up to 100 MV at 150 kHz [1]. In the 1920s and 1930s, Japanese [2] and U.S. researchers [3] conducted feasibility studies into WPT. With the development of high-power high efficiency microwave tubes by the Raytheon Company, Waltham, MA, in the 1950s [4], the concept of WPT became a reality.

In the 1960s, Raytheon developed a rectifying antenna or rectenna that converted RF-to-dc power at 2.45 GHz. The rectenna consisted of a half-wave dipole antenna with a balanced bridge or single diode placed above a reflecting plane, as well as a resistive load. The rectenna conversion efficiency, also referred to as the percentage of power converted from RF-to-dc, increased throughout the 1960s and 1970s. The highest conversion efficiency ever recorded was achieved by Brown at Raytheon in 1977 [5]. Brown used a GaAs–Pt Schottky barrier diode and aluminum bar dipole and transmission lines to achieve a 90.6% conversion efficiency at an input microwave power level of 8 W. Later, Brown and Triner developed a printed thin-film version at 2.45 GHz with an 85% conversion efficiency [6].

In 1991, ARCO Power Technologies, Inc., Washington, DC, developed a rectenna element with a 72% conversion efficiency at 35 GHz [7]. This frequency shift from the traditional 2.45 to 35 GHz resulted in much smaller aperture areas, however, the components necessary for generating high power at 35 GHz are inefficient and expensive.

Due to the disadvantages noted at 35 GHz, a new operating frequency or 5.8 GHz was investigated. 5.8 GHz has small component sizes and greater transmission ranges than 2.45 GHz. In 1992, the first C-band rectenna yielded an 80% conversion efficiency [8]. These efficiencies were measured in a waveguide simulator with an input power level of approximately 700 mW per element. This rectenna used a printed dipole, which fed an Si Schottky diode quad bridge. In 1998, McSpadden *et al.* used a printed dipole rectenna to achieve the highest conversion efficiency for 5.8 GHz at 82% [9]. The rectenna used an MA40150-119 diode for rectification on a coplanar stripline (CPS) layout.

In the last few years, researchers have looked into the designing of circularly polarized (CP) rectennas. Circular polarization enables the receive or transmit antennas to be rotated without changing the output voltage. Suh *et al.* achieved 60% for a single-element rectenna at 5.8 GHz [10]. Another group at the Jet Propulsion Laboratory (JPL), Pasadena, CA, was able to operate a dual-polarized rectenna array around 52% at 8.51 GHz [11].

The rectenna design discussed in this paper combines high-efficiency RF-to-dc diode conversion with a wide-band high-gain CP antenna to produce large amounts of dc power regardless of the rectenna's orientation. The new rectenna is fabricated on a single thin layer using CPS transmission lines for fabrication simplicity and size reduction. This rectenna design is being done as part of a feasibility study for the National Aeronautics and Space Administration (NASA), Washington, DC, concerning space solar power. Large space solar power satellites (SPSs) that are miles across are to be put in space to collect the sun's energy with the use of solar cells. The solar cell dc power is then converted to microwave energy using magnetrons located on antennas in a phased array. The phased-array beams the collected 5.8-GHz microwave energy to the terrestrial rectenna array as the SPS moves overhead. Since the orbital orientation of the SPS can vary, the array's rectennas must be CP in order to keep a constant collected dc power. The harmful second harmonic frequency (11.6 GHz) generated by the rectenna's diode is prohibited from re-radiation with the use of a filter located behind the antenna. Astronomers use the band containing 11.6 GHz to listen for signals coming from space. Therefore, the radiated noise at 11.6 GHz could be detrimental to their purpose.

Traditionally, rectennas have used dipoles or patch antennas with low gains. Here, a dual rhombic loop antenna (DRLA) is used with a gain of 10.7 dBi. The use of a high-gain antenna

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The authors are with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: strassner@ee.tamu.edu; chang@ee.tamu.edu).

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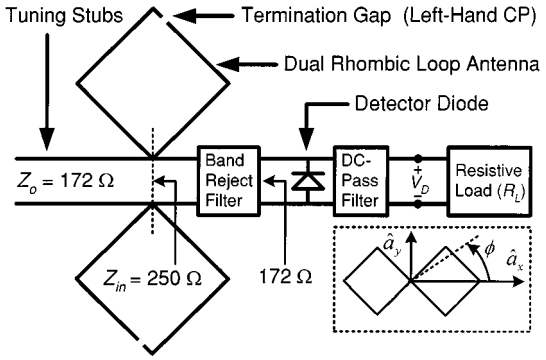


Fig. 1. Rectenna block diagram and spatial orientation.

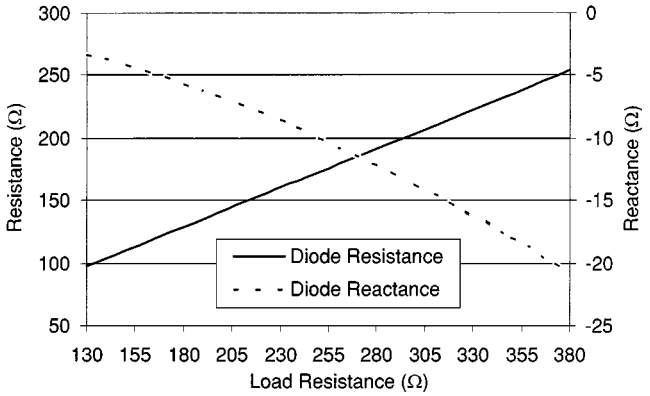


Fig. 2. Calculated diode impedance versus load resistance for $V_D = 3.5$ V.

has the advantage of reducing the number of rectenna elements necessary to cover the same receiving area. The effective area of an antenna is proportional to its gain. The higher antenna gain corresponds to a larger effective area.

II. Rectenna Operation Theory

Fig. 1 diagrams the main components necessary for efficient rectenna operation. The high-gain antenna couples power into the CPS circuit. A band-reject filter located behind the antenna allows the incoming power at 5.8 GHz to pass to the detector diode where a large portion of the RF power is converted to dc power. The remaining RF portion is bounced between the band-reject filter and the dc-pass filter where it remixes at the diode and forms more dc. The resistive load (R_L) is isolated from any RF signals because of the dc pass filter. R_L must be chosen such that the dc-converted portion of the RF power is maximized. Proper placement of the diode and filters is also crucial to maximizing the dc power.

The diode conversion efficiency (η_D) is key in determining the rectenna's performance. The diode efficiency is defined as the following ratio:

$$\eta_D = \frac{\text{dc output power}}{\text{RF power incident on diode}}. \tag{1}$$

A diode model described by Yoo and Chang [12] is used to predict the rectenna diode's behavior. The model depends only on the diode electrical parameters and microwave circuit losses at the fundamental frequency of operation. Harmonic effects are not included. The RF-to-dc conversion efficiency is described by

$$\eta_D = \frac{1}{A+B} \tag{2}$$

where the low-frequency denominator asymptote is

$$A = 1+\frac{R_L}{\pi R_S}\left(1+\frac{V_{bi}}{V_D}\right)^2\left[\theta_{\text{on}}\left(1+\frac{1}{2\cos^2\theta_{\text{on}}}\right)-\frac{3}{2}\tan\theta_{\text{on}}\right] + \frac{R_L}{\pi R_S}\left(1+\frac{V_{bi}}{V_D}\right)\frac{V_{bi}}{V_D}(\tan\theta_{\text{on}}-\theta_{\text{on}}) \tag{3}$$

and the high-frequency term is

$$B = \frac{R_S R_L C_j^2 \omega^2}{2\pi}\left(1+\frac{V_{bi}}{V_D}\right)\left(\frac{\pi-\theta_{\text{on}}}{\cos^2\theta_{\text{on}}}+\tan\theta_{\text{on}}\right) \tag{4}$$

and ω is the angular frequency ($2\pi f$). R_S is the diode's series resistance. V_{bi} is the forward-bias turn-on voltage of the diode and V_D is the self-bias voltage due to rectification across the terminals of the diode. The variable θ_{on} refers to the forward-bias turn-on angle of the diode [9]. It is represented by

$$\tan\theta_{\text{on}} - \theta_{\text{on}} = \frac{\pi R_S}{R_L\left(1+\dfrac{V_{bi}}{V_D}\right)}. \tag{5}$$

Equation (5) is a transcendental equation and can be solved iteratively. The diode's junction capacitance C_j is

$$C_j = C_{jo}\sqrt{\frac{V_{bi}}{V_{bi}+|V_D|}} \tag{6}$$

where C_{jo} is the diode's zero-bias junction capacitance.

The diode's input impedance is defined as

$$Z_D = \frac{\pi R_S}{D+jE} \tag{7}$$

where

$$D = \cos\theta_{\text{on}}\left(\frac{\theta_{\text{on}}}{\cos\theta_{\text{on}}} - \sin\theta_{\text{on}}\right) \tag{8}$$

and

$$E = \omega R_S C_j\left(\frac{\pi-\theta_{\text{on}}}{\cos\theta_{\text{on}}}+\sin\theta_{\text{on}}\right). \tag{9}$$

The diode used in the rectenna circuit is the M/A COM detector diode MA4E1317. It has series resistance $R_S = 4\ \Omega$, zero-bias junction capacitance $C_{j0} = 0.02$ pF, built-in turn-on voltage $V_{bi} = 0.7$ V, and breakdown voltage $V_B = 7$ V. The load resistance (R_L) has been chosen to be 250 Ω. For this load resistance, $Z_D = 172.1 - j9.1\ \Omega$ at 5.8 GHz and $V_B/2 = 3.5$ V, as shown in Fig. 2. The dc-pass filter (capacitor) acts as a shorted stub matching network to not only tune out this diode reactance, but also to optimize the remixing of the power at the harmonic frequencies. The detector should not be designed to operate at more than 3.5 V since this would exceed $V_B/2$ and could force the diode into avalanche breakdown. However, this diode has been shown to produce output voltages up to 5 V. Fig. 3 shows the effects the diode voltage has on the diode impedance. The diode resistance at 3.5 V is 172 Ω. The CPS transmission line that allows power to flow between the various rectenna components is designed to have a characteristic impedance $Z_o = 172\ \Omega$. This minimizes the reflection of the 5.8-GHz RF power at the diode terminals, thus increasing the rectenna's efficiency.

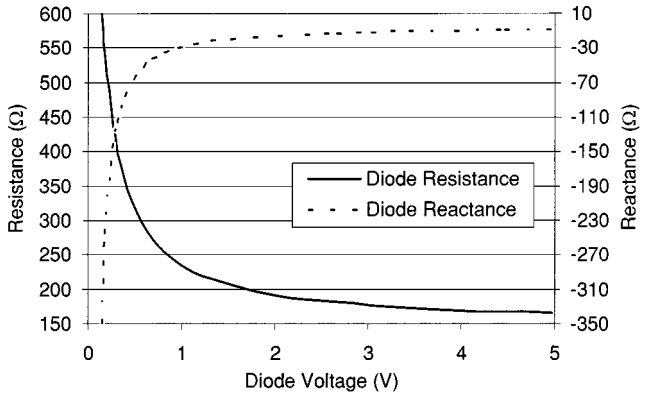


Fig. 3. Calculated diode impedance versus diode voltage for $R_L = 250\ \Omega$.

III. Simulated and Measured Data for Rectenna Components

The rectenna outlined in Fig. 1 consists of an antenna, band-reject filter, Schottky detector diode, dc-pass filter, and a resistive load. The antenna and band-reject filter are designed using the full-wave electromagnetic simulator IE3D. IE3D allows for all of the sections to be analyzed together and can deembed certain sections in order to isolate and identify the microwave characteristics of other components in the microwave circuit.

A. CPS Characteristic Impedance

The CPS width and gap are 0.824 and 0.4 mm, respectively. These dimensions provide the proper size for diode and capacitor bonding and the desired CPS characteristic impedance (172 Ω). The impedance of CPS is higher than that of microstrip and matches better to the real input impedance of the diode.

B. CP DRLA

The rectenna uses a DRLA configuration [13], as seen in Fig. 1. The DRLA is terminated with two gaps. The positioning of the gaps, as shown in Fig. 1, yields left-hand circular polarization. If the gaps are mirrored to the opposing sides of the antenna, the DRLA will become a right-hand CP. Circular polarization is very sensitive to the gap position. The advantages for using the DRLA are high CP gain, wide-band performance, and fabrication simplicity. The CPS tuning stubs yield a real impedance at the antenna's input terminals and allow for the individual rectenna to be connected to other rectennas in an array. The reflecting plane located 11 mm (0.21 λ_o) behind the antenna increases the gain by directing the beam broadside in one direction. IE3D simulated antenna input impedance data is shown in Fig. 4. The input impedance (Z_{in}) at the antenna's input terminals for the resonant frequency 5.8 GHz is shown to be 250 Ω. A slight saddle region exists around 5.8 GHz improving the antenna's bandwidth. To find the antenna's simulated input impedances, radiation patterns and circular polarization, the antenna must be simulated in IE3D with the band-reject filter in place since the filter will couple to the antenna and affect the radiation. The filter is then deembedded in IE3D to find the input impedances.

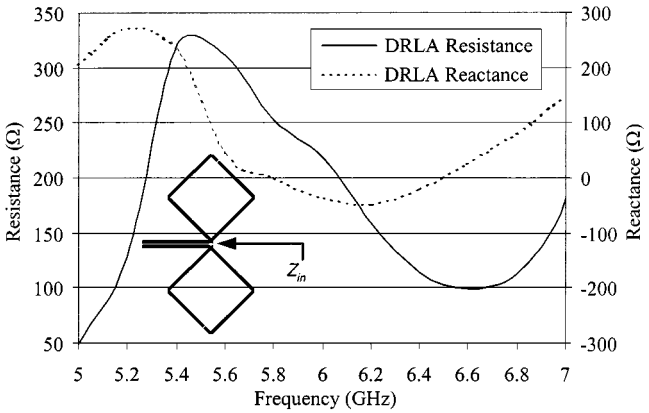


Fig. 4. IE3D simulated input impedance of the DRLA located 11 mm above a reflecting plane.

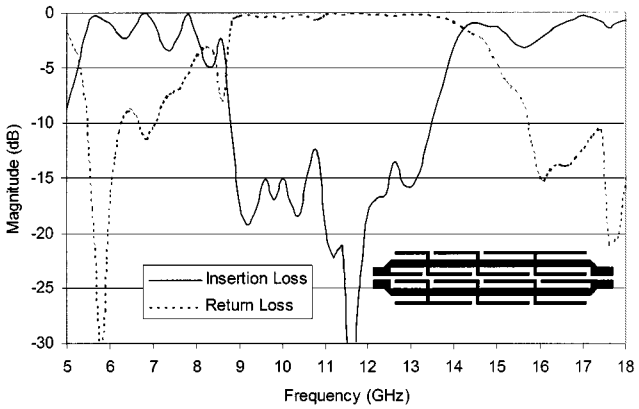


Fig. 5. IE3D simulated CPS BRF S-parameters.

C. Coplanar Stripline Band-Reject Filter (CPS BRF)

The CPS BRF is used to pass 5.8 GHz from the antenna to the diode and block the second harmonic 11.6 GHz from flowing from the diode to the antenna. The filter's geometry improves upon existing band-reject designs [14] by adding additional stubs on the outside of the main CPS lines for better rejection. The CPS BRF uses $\lambda/4$ stubs to block 11.6 GHz. This filter has high harmonic rejection in comparison with other planar CPS geometries of comparable size. The filter's simulated S-parameters from IE3D are shown in Fig. 5. IE3D predicts an insertion loss of 0.3 dB at 5.8 GHz from the antenna to the diode. The filter blocks 11.6 GHz flowing from the diode to the antenna by more than 20 dB. The diode-side port of the CPS BRF is terminated to the characteristic impedance of the CPS or 172 Ω. The antenna-side port of the filter has a different port impedance (Z_{in}) for every different frequency. At 5.8 GHz, the CPS BRF's antenna-side port impedance is 250 Ω, and the diode-side port impedance is 172 Ω. IE3D determines the impedances at other frequencies by first simulating the DRLA and CPS BRF together. The CPS BRF is then deembedded in order to determine the impedance looking into the DRLA's input terminals. These input impedances are used as the antenna-side port impedances for determining the CPS BRF's S-parameters. At 5.8 GHz, the filter matches the DRLA to the resistance of the detector diode.

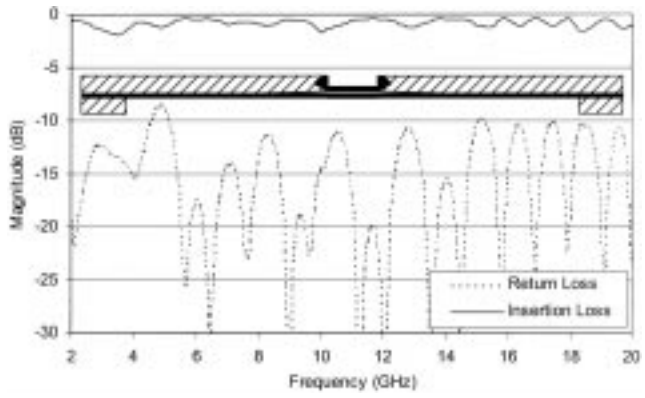


Fig. 6. Measured back-to-back 50-Ω microstrip to 172-Ω CPS balun S-parameters. The inset drawing is a top view of the balun circuit with the hatched area representing the bottom-side metallization (balun ground) and the black areas representing the top-side metallization. Both sides are separated by 10-mil Duroid 5870.

TABLE I
50–172-Ω BALUN PERFORMANCE

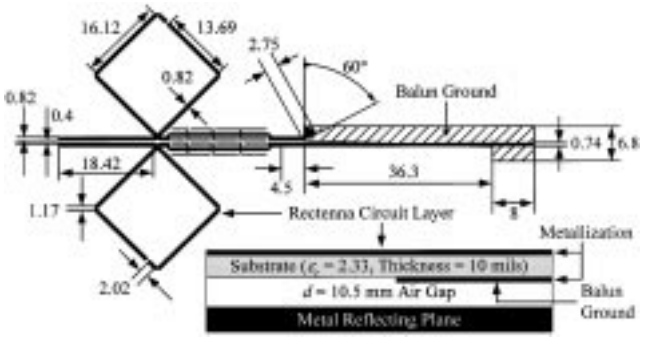
	5.8 GHz	11.6 GHz	17.4 GHz
Return loss (dB)	20	20	10.2
Insertion loss (dB)	0.42	0.44	1.1
½ Insertion loss (dB)	0.21	0.22	0.55

D. Microstrip to CPS Baluns

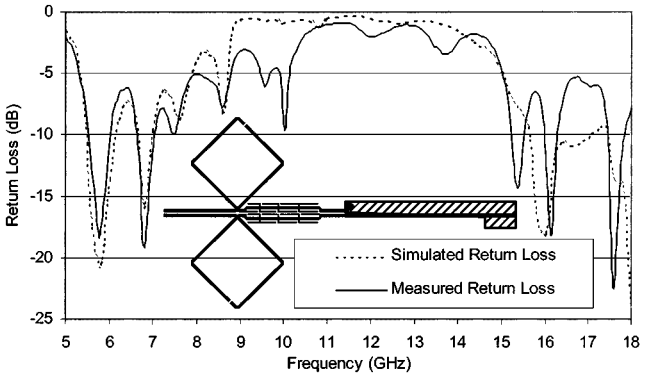
In order to measure various patterns and S-parameters of the antenna and band-reject filter, a balun must be designed that matches the 172-Ω CPS BRF diode-side impedance to a 50-Ω microstrip line. For measurement purposes, two of the baluns must be placed back-to-back. The return and insertion losses are shown in Fig. 6. The losses at 5.8, 11.6, and 17.4 GHz are listed in Table I. Half of the total loss represents one side of the back-to-back balun circuit or one microstrip to CPS transition. The balun is impedance-matched at both 5.8 and 11.6 GHz. The back-to-back balun shows a broad-band operation with an insertion loss of less than 2 dB and a return loss better than 10 dB for 5–20 GHz.

E. Antenna + CPS BRF + Balun Linear Polarized (LP) Measured Results

To obtain an accurate measurement for the rectenna, the antenna and band-reject filter must be both simulated and measured together due to coupling between the two sections. The circuit used to obtain the rectenna's return loss, patterns, and gain measurements is shown in Fig. 7(a). The circuit includes the DRLA, CPS BRF, and CPS to microstrip balun. Using the HP 8510B network analyzer measurement system, the return loss or S_{11} was obtained, as shown in Fig. 7(b). Slight differences between the simulated and measured return losses are attributed to difficulties in precisely aligning the balun's top layer with the balun's ground layer. The differences seen between 9–10 GHz are due to radiation losses attributed to the balun's radial fan. The simulator does not fully recognize this radiation loss. At the fundamental frequency 5.8 GHz, $S_{11} = -18.3$ dB, and, at the second harmonic frequency 11.6 GHz, $S_{11} = -1.1$ dB. Therefore, 5.8 GHz will pass through with low loss, and the second harmonic 11.6 GHz will have high loss.



(a)



(b)

Fig. 7. (a) Rectenna pattern and gain measurement circuit layout. (All dimensions in millimeters.) Both a top view of the rectenna and its layered profile is shown. (b) Measured and IE3D simulated return loss of the pattern and gain measurement circuit.

The 2 : 1 voltage standing wave ratio (VSWR) bandwidth centered about 5.8 GHz is 10%.

To determine the axial ratio (AR), linear gain pattern measurements are taken using a Narda 642 standard gain horn located a distance away along the normal or z-axis of the rectenna (see Fig. 1 for coordinates). These measurements are shown in Fig. 8(a). The rhombic loop antenna is measured for three rotated orientations at $\phi = 0\,°, 45°$, and $90°$ (ϕ is shown in Fig. 1). The broadside ($\theta = 0°$) LP gains ($G_{\rm LP}$) and 3-dB beamwidths are listed in Table II.

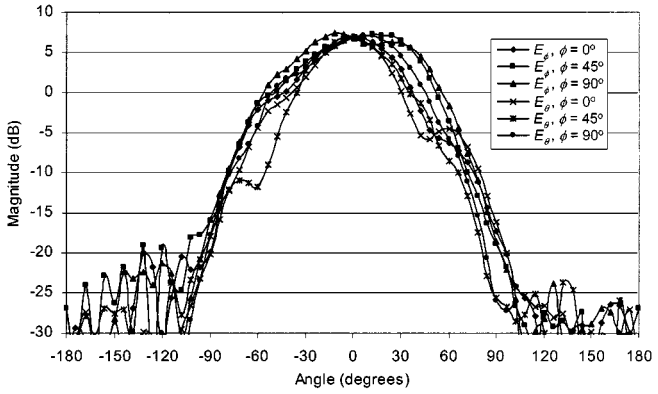
The AR is determined by subtracting the smallest broadside gain from the largest. From the AR, the gain correction factor (GCF) for scaling LP gains into CP [15] gains is determined. The GCF in decibels is defined as follows:

$$\mathrm{GCF} = 20 \cdot \log\left(\frac{10^{AR/20}+1}{\sqrt{2}\cdot 10^{AR/20}}\right). \tag{10}$$

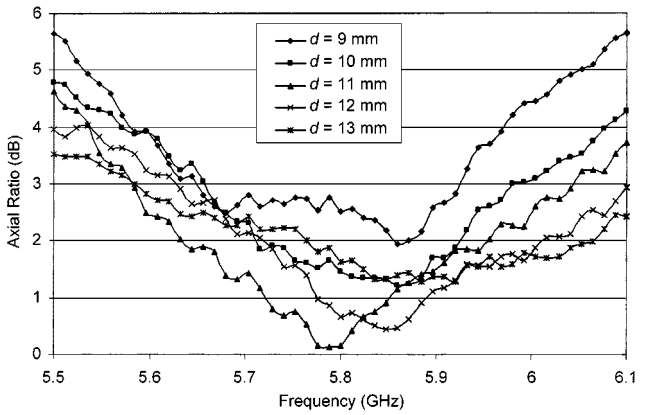
Since $AR = 0.2$ dB, GCF $= 2.91$ dB. If the rhombic loop antenna was exactly CP at 5.8 GHz, i.e., $AR = 0$ dB, the GCF would equal 3 dB. Using the GCF, the adjusted CP gain is

$$G_{\rm CP} = G_{\rm LP} + \mathrm{GCF}. \tag{11}$$

By taking the broadside ($\theta = 0°$) LP gain average and adding the GCF, the adjusted CP gain of the rectenna + the balun is 9.8 dB. If the CPS BRF, balun, and connector losses are deembedded, the DRLA can be shown to have a CP gain of 10.5 dB. This scaling acts as an approximation for CP gain and should be supported by CP-to-CP measurements.



(a)



(b)

Fig. 8. (a) Measured LP gains at 5.8 GHz for $\phi = 0°, 45°$, and $90°$ rhombic loop orientations. (b) Measured rectenna AR for different reflecting plane spacing (d).

TABLE II
LINEAR POLARIZED GAINS FOR ANTENNA + CPS LPF + BALUN

$\theta = 0°$ (Broadside)	E_ϕ $\phi = 0°$	E_ϕ $\phi = 45°$	E_ϕ $\phi = 90°$	E_θ $\phi = 0°$	E_θ $\phi = 45°$	E_θ $\phi = 90°$
LP Gain (dB)	6.9	6.8	6.7	6.8	6.9	6.9
LP Beamwidth (°)	55	70	86	41	39	50

Antenna patterns are also measured at 11.6 GHz for the three rotated rectenna orientations at $\phi = 0°, 45°$, and $90°$. These patterns show the main beam to be at $\theta = 36°$ for the second harmonic. The filter suppresses the maximum gain down to around -5 dB, which is approximately 12 dB below the gain of the fundamental frequency.

The air gap thickness (d) separating the rectenna from the reflecting plane greatly affects the AR, as revealed by the measurement data shown in Fig. 8(b). The best AR of 0.2 dB at 5.8 GHz is obtained when $d = 11$ mm. When $d < 11$ mm for the 0° rectenna orientation, the E_ϕ LP gain is greater than the E_θ LP gain. Similarly, when $d > 11$ mm, the E_θ gain is greater.

F. Antenna + CPS BRF + Balun CP Measured Results

In order to confirm the scaling of LP gain to CP gain in the previous section, a cavity-backed CP spiral antenna (AR $\cong$ 0.2 dB) is used to obtain the actual CP measured gain of the circuit shown in Fig. 7(a). The rhombic loop antenna is measured for three rotated orientations at $\phi = 0°, 45°$, and $90°$.

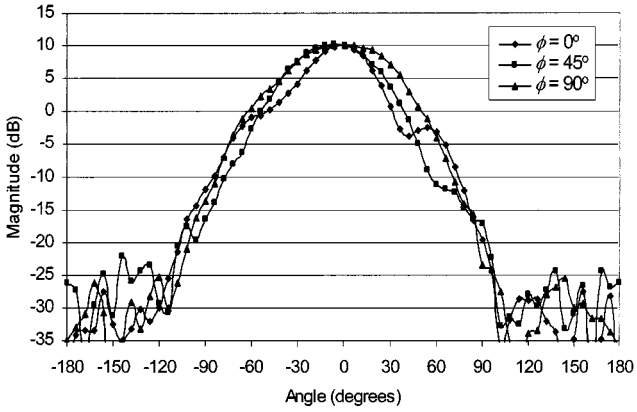


Fig. 9. Measured CP gains at 5.8 GHz for $\phi = 0°, 45°$, and $90°$ rhombic loop orientations.

Fig. 9 shows the three patterns. The broadside ($\theta = 0°$) CP gain is close to 10 dB, which is close to 3 dB higher than the measured linear gains. If the CPS BRF, balun, and connector losses are deembedded, the DRLA can be shown to have a CP gain of approximately 10.7 dB. This CP measured gain is close to the scaled CP gain of 10.5 dB. The beamwidth of the DRLA is 40° in the y–z-plane and 60° in the x–z-plane for the $\phi = 0°$ rectenna orientation. The DRLA beamwidths describe a pattern with an elliptical cross section with the maximum dimension in the x–z-plane and minimum dimension in the y–z-plane for $\phi = 0°$.

G. DC-Pass Filter

The dc-pass filter consists of a 2.4-nF 50 VDC C08BLBB1X5UX dc-blocking capacitor manufactured by Dielectric Laboratories, Cazenovia, NY. The capacitor is used to reflect all of the microwave energy arising from the diode from reaching the load resistor, thus returning the RF energy back to the diode. The capacitor's characteristics across the CPS line are shown in Fig. 10. The capacitor blocks 5.8, 11.6, and 17.4 GHz greater than 16.8 dB. This translates to less than 2% of the total RF power leaking to the load.

H. Diode Efficiency Direct Measurement

The diode used in the rectenna circuit is the M/A COM flip-chip detector diode MA4E1317 with negligible parasitics. The diode converts the incoming 5.8-GHz microwave energy coming from the CPS BRF into a large dc component and smaller power levels at each of the harmonic frequencies. The diode efficiency direct measurement circuit and curves for V_D and η_D versus power delivered to the diode (P_D) for various R_L are shown in Fig. 11. After varying the load resistance R_L and capacitor to diode spacing at various incident powers to the diode, the optimum distance was found to be 9.5 mm. The diode voltage increases according to the relationship V_D^2/R_L as R_L increases. The detector should not be designed to operate at more than 3.5 V since this would exceed $V_B/2$. R_L between 150 and 250 Ω produces the optimum diode efficiency performance. Over 80% conversion efficiency was achieved with an R_L of 250 Ω.

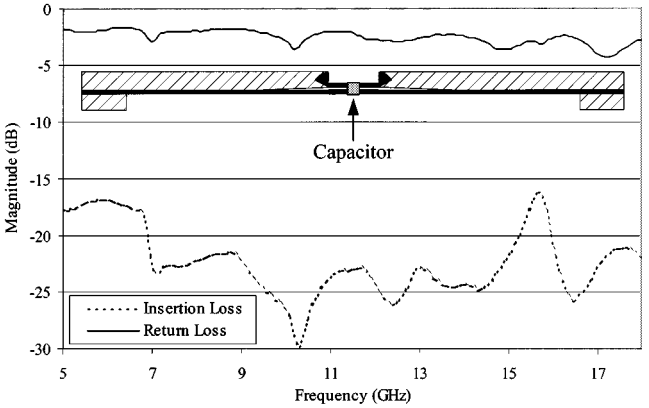


Fig. 10. Measured balun–capacitor–balun return and insertion losses.

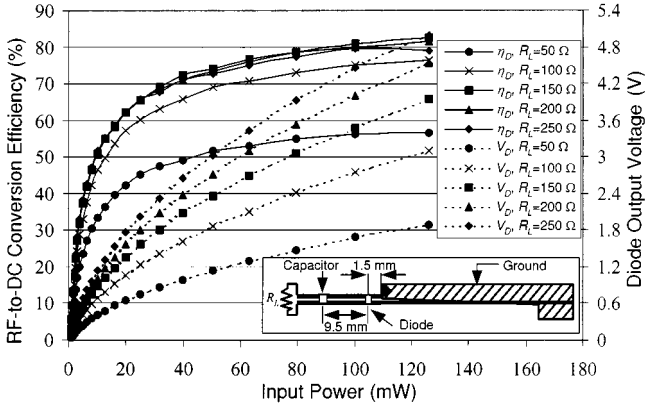


Fig. 11. Directly measured diode conversion efficiency and output voltage versus power delivered to the diode for various load resistances.

I. Free-Space Rectenna Measurement Results

The diode used in the rectenna circuit is the M/A COM detector diode MA4E1317. It is in a flip-chip package with negligible parasitics. The diode converts the incoming 5.8-GHz microwave energy coming from the CPS BRF into a dc output. Far-field H- and E-plane free-space voltage measurements for the $\phi = 0°$ rectenna orientation and $R_L = 250\ \Omega$ are taken in order to determine the rectenna's RF-to-dc conversion efficiency. Equation (1) or the diode efficiency is rewritten incorporating the Friis transmission equation as

$$\eta_D = \frac{\left(\frac{V_D^2}{R_L}\right)}{P_t \cdot G_t \cdot G_r \cdot \left(\frac{\lambda_o}{4\pi r}\right)^2} \tag{12}$$

where P_t and G_t are the transmitted power and transmitter gain, respectively. G_r is the gain of the rectenna, and r is the distance between the transmitter and rectenna in meters. λ_o is the free-space wavelength at 5.8 GHz in meters. The calculated free-space efficiency curves using (2)–(6), as well as the directly measured diode efficiency and E-plane ($\phi = 0$) and H-plane ($\phi = 0$) measured efficiency curves are shown in Fig. 12 for $R_L = 250\ \Omega$. The E- and H-plane refer to the horn's orientation. All of the curves saturate at around 80%. The calculated diode efficiency closely models the measured RF-to-dc conversion efficiency.

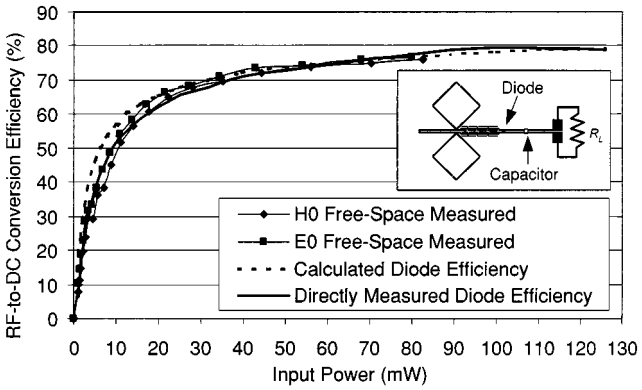


Fig. 12. Free-space measured, direct measured, and calculated efficiency for $R_L = 250\ \Omega$.

IV. Conclusions

This rectenna achieves efficiencies very close to the highest ever recorded at 5.8 GHz (82%) with the added improvement of circular polarization and high antenna gain. The DRLA wide bandwidth allows the rectenna to operate from 5.6 to around 6 GHz with a better than 3-dB AR. The flip-chip Schottky diode used provides excellent efficiency near 80% with very small size. The capacitor blocks the RF energy by more than 16.8 dB, and the CPS BRF suppresses the second harmonic signal to around 20 dB below the peak fundamental gain. This results in minimal radiation at the second harmonic frequency. The diode model presented predicts the RF-to-dc conversion extremely well and allows the proper diode to be chosen based upon its parameters R_S, C_{j0}, V_{bi}, and V_B. The electromagnetic simulator IE3D models each microwave circuit section of the rectenna with reasonable accuracy providing the insight necessary to facilitate the design.

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Berndie Strassner (S'96) received the B.S. degree in electrical engineering from the Rose-Hulman Institute of Technology, Terre Haute, IN, in 1995, and the M.S. degree in electrical engineering from Texas A&M University, College Station, TX, in 1997.

During the summer of 1992, 1993, and 1995, he was with the Johnson Space Center, Lockheed-Martin, where he was involved in the areas of space-shuttle navigational controls, power systems, and communication systems, respectively. In 1994, he was involved with microwave deembedding processes at the Technische Universität Hamburg-Harburg, Harburg, Germany. From 1996 to 1997, he was with Sandia National Laboratories, where he was involved with the study of the effects of harmonic termination on power-amplifier performance. He is currently a Research Assistant with the Electromagnetics Laboratory, Texas A&M University. His current research is RF identification tags, rectifying antenna arrays, and reflecting antenna arrays.

Kai Chang (S'75–M'76–SM'85–F'91) received the B.S.E.E. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1970, the M.S. degree from the State University of New York at Stony Brook, in 1972, and the Ph.D. degree from The University of Michigan at Ann Arbor, in 1976.

From 1972 to 1976, he was with the Microwave Solid-State Circuits Group, Cooley Electronics Laboratory, The University of Michigan at Ann Arbor, where he was a Research Assistant. From 1976 to 1978, he was with Shared Applications Inc., Ann Arbor, MI, where he was involved with computer simulation of microwave circuits and microwave tubes. From 1978 to 1981, he was with the Electron Dynamics Division, Hughes Aircraft Company, Torrance, CA, where he was involved in the research and development of millimeter-wave solid-state devices and circuits, power combiners, oscillators, and transmitters. From 1981 to 1985, he was with TRW Electronics and Defense, Redondo Beach, CA, where he was a Section Head involved with the development of state-of-the-art millimeter-wave integrated circuits and subsystems, including mixers, voltage-controlled oscillators (VCOs), transmitters, amplifiers, modulators, upconverters, switches, multipliers, receivers, and transceivers. In August 1985, he joined the Electrical Engineering Department, Texas A&M University, College Station, as an Associate Professor, and became a Professor in 1988. In January 1990, he became an E-Systems Endowed Professor of Electrical Engineering. He has authored and co-authored several books, including *Microwave Solid-State Circuits and Applications* (New York: Wiley, 1994), *Microwave Ring Circuits and Antennas* (New York: Wiley, 1996), *Integrated Active Antennas and Spatial Power Combining* (New York: Wiley, 1996), and *RF and Microwave Wireless Systems* (New York: Wiley, 2000). He has served as the Editor of the four-volume *Handbook of Microwave and Optical Components* (New York: Wiley, 1989 and 1990). He is the Editor of *Microwave and Optical Technology Letters* and the Wiley Book Series on "Microwave and Optical Engineering." He has also authored or co-authored over 350 technical papers and several book chapters in the areas of microwave and millimeter-wave devices, circuits, and antennas. His current interests are in microwave and millimeter-wave devices and circuits, microwave integrated circuits, integrated antennas, wide-band and active antennas, phased arrays, microwave power transmission, and microwave optical interactions.

Dr. Chang was the recipient of the 1984 Special Achievement Award presented by TRW, the 1988 Halliburton Professor Award, the 1989 Distinguished Teaching Award, the 1992 Distinguished Research Award, and the 1996 Texas Engineering Experiment Station (TEES) Fellow Award presented by Texas A&M University.