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Lab 3
COMPUTER TECHNOLOGY 4.2

(E1) Identify hazard:

(a) LD R1, 0(R2)
DADD R3, R1, R2
Data Hazard (RAW)
DADD instruction depends on the result of the LD instruction. The LD loads a value into R1, and the DADD uses that value

(b) MULT R1, R2, R3
DADD R1, R2, R3
Data Hazard (WAW)
Both MULT and DADD write to R1. If the DADD completes before the MULT, the value written by MULT will be overwritten.

(c) MULT R1, R2, R3
MULT R4, R5, R6
No Hazard
The two MULT instructions operate on different registers and do not have any dependencies.

(d) DADD R1, R2, R3
SD 2000(R0), R1
Data Hazard (RAW)
The SD instruction depends on the result of the DADD instruction. The DADD calculates a value and stores it in R1 which is used by SD.

(e) DADD R1, R2, R3
SD 2000(R1), R4
No Hazard. The DADD and SD instructions operate on different registers and do not have any dependencies.

E3 (a) Behaviour of a 2-bit saturating counter branch predictor:

It has 4 states: 00 (Strongly not taken), 01 (Weakly Not taken), 10 (Weakly taken) and 11 (Strongly taken).

00: Predict Not Taken, Transition to 01 on Taken.

01: Predict Not Taken, Transition to 10 on Taken, Transition to 00 on Not Taken

10: Predict Taken, Transition to 11 on Taken, Transition to 01 on Not Taken

11: Predict Taken, Transition to 10 on Not Taken.

(b) Branch Predictor:

Initial State: 00 (Strongly Not Taken)

Iteration 1 (x[0] is not 0):

Branch Taken (since x[0] < 0 is false)

Predictor State: 01 (Transition from 00 on Taken)

Iteration 2 (x[1] is 0):

Branch Not Taken (since x[1] < 0 is true)

Predictor State: 00 (Transition from 01 on Not Taken)

Iteration 3 (x[2] is not 0):

Branch Taken

Predictor State: 01 (Transition from 00 on Taken)

Iteration 4 (x[3] is 0):

Branch Not Taken

Predictor State: 00 (Transition from 01 on Not Taken)