BRYSON FIBANDA OMULUBI
SCT212-0025/2020
Lab 4
COMPUTER TECHNOLOGY 4-2

E1 (a) Tag size for the cache:

Cache size: 256x1024 bytes = 262144 bytes
Block size: 64 bytes
Number of Blocks: 262144 bytes / 64 bytes = 4096 blocks
Index Bits: $\log_2(4096) = 12$ bits
Block Offset Bits: $\log_2(64) = 6$ bits
Address size: 32 bits
Tag size = 32 - 12 - 6
= 14 bits.

(b) Speedup Calculation.

With Misses:

CPI = CPI base + (Memory access x Miss rate x Miss Penalty)
= 1.0 + (0.5 x 0.02 x 25)
= 1.25

With All Hits:

= 1.0

Speedup:

$$\frac{\text{CPI with misses}}{\text{CPI with all hits}}$$

$$= \frac{1.25}{1.0}$$

= 1.25

E2 Calculations:

Miss Rate: 5% of 10^7 accesses = 5×10^7 misses per second

Write misses: 20% are writes = $0.20 \times 5 \times 10^7$

Read misses: 80% are reads = $0.80 \times 5 \times 10^7 = 4 \times 10^7$

Memory Traffic from Reads: $4 \times 10^7 \times 2 = 8 \times 10^7$

Write backs will be proportional to the number of misses and the percentage of modified blocks.

Total Memory traffic = Read traffic + Write Traffic (Including write-backs)

E3 Write-Through Cache:

Writes: 20% of instructions

Miss Rate: 1%

Miss Penalty: 50 clock cycles

Block Write Penalty: 100 clock cycles

Average Memory Access Time: Hit Time + Miss Rate × Miss Penalty

= 1 + 0.01 × 50

= 1.5 clock cycles

Write time: 2 clock cycles

Write Back Cache:

Writes: 1% of instructions

Miss rate: 1%

Miss penalty: 50 clock cycles

Block Write Penalty: 100 clock cycles

AMAT = 1 + 0.01 × 50

= 1.5 clock cycles

Write time = 2 clock cycles

Write back cache is better due to lower memory traffic.