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SCT212-0075/2020

Lab 5

COMPUTER TECHNOLOGY 4-2

① (a) Miss Analysis:

$$\begin{aligned} X &= 1000 \times 4 = 4000 \\ &= 4000 / 32 \text{ bytes} \\ &= 125 \text{ blocks} \end{aligned}$$

$$\begin{aligned} Y &= 1000 \times 4 = 4000 \\ &= 4000 / 32 \\ &= 125 \text{ blocks} \end{aligned}$$

$$\begin{aligned} \text{Compulsory misses} &= 125 + 125 \\ &= 250 \text{ misses} \end{aligned}$$

Capacity Misses:

$$16 \times 32 = 512 \text{ blocks}$$

No capacity miss

Conflict Misses:

$$= 0 \times 4000 / 32 = 0 \times 200$$

$$0 \times 8000 / 32 = 0 \times 400$$

Cache: 512 blocks

Mapping:  $0 \times 200$  to 0 ( $0 \times 200 \times 512 = 0$ )

$0 \times 400$  to 0 ( $0 \times 400 \times 512 = 0$ )

$$\text{Conflict Misses} = 1000 / 8$$

$$= 125 \text{ conflict misses}$$

Total Misses:

$$= 250 + 125$$

$$= 375 \text{ misses}$$



(b) Software solution to reduce number of data cache misses:

~~Cache Organization~~ Solution: Set-Associative Cache

• Cache Organization:

16 cache size

32 bytes block size

2-way set associativity

Number of sets:  $16 \text{ kb} / (32 \times 2)$

$= 256 \text{ sets}$

• Miss Analysis

$= 250$

• Misses with 2-way set associativity:

$= 250$

(c) Data cache miss rate:

Memory access  $= 1000 \times 2 + 1$

$= 3000$

Miss Rate (Direct mapped)

$= 375 / 3000$

$= 0.125$

$= 12.5\%$

Miss Rate (2-way set associative)

$= 250 / 3000$

$= 0.0833$

$= 8.33\%$