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Lab 2

COMPUTER TECHNOLOGY 4-2

(a) Timing of the instruction sequence:

Cycle	LD R1,0(R2)	ADDI R1,R1,1	SD 0(R2),R1	ADDI R2,R2,4	BNEZ R4,Loop
1	IF				
2	ID				
3	EX				
4	MEM				
5	WB				
6		IF			
7		ID			
8		EX			
9		MEM			
10		WB			
11			IF		
12			ID		
13			EX		
14			MEM		
15			WB		
16				IF	
17				ID	
18				EX	
19				MEM	
20				WB	
21					IF
22					ID
33					EX
24					MEM
25					WB

Loop repeats 42 times.

(a) How many cycles the loop takes to execute.

25 iterations × 42 iterations

= 1050 cycles.

(b) Timing for the RISC pipeline:

Cycle	LD R1,0(R2)	ADDI R1,R1,1	SD 0(R2),R1	ADDI R2,R2,4	BNEZ R4,loop
1	IF				
2	ID				
3	EX	IF			
4	MEM	ID	IF		
5	WB	EX	ID	IF	
6		MEM	EX	ID	IF
7		WB	MEM	EX	ID
8			WB	MEM	EX
9				WB	MEM
10					WB

(c) RISC pipeline with delayed branch.

Cycle	LD R1,0(R2)	ADDI R1,R1,1	SD 0(R2),R1	ADDI R2,R2,4	BNEZ R4,loop
1	IF				
2	ID				
3	EX	IF			
4	MEM	ID	IF		
5	WB	EX	ID	IF	
6		MEM	EX	ID	Bne (Delay slot)
7		WB	MEM	EX	IF
8			WB	MEM	ID
9				WB	EX
10					MEM
11					WB