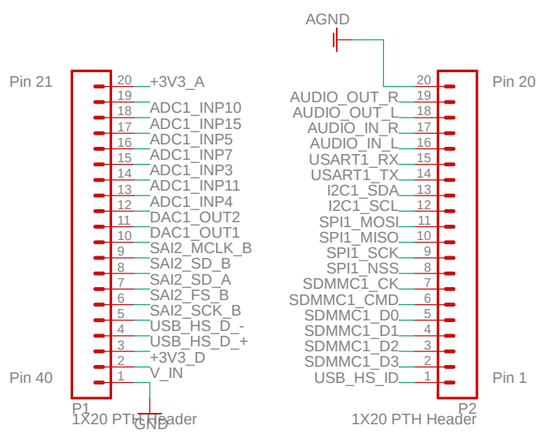
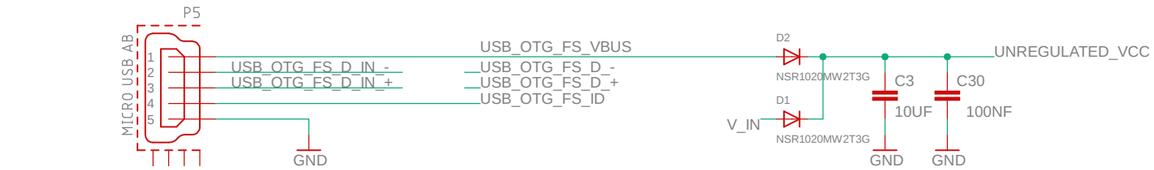


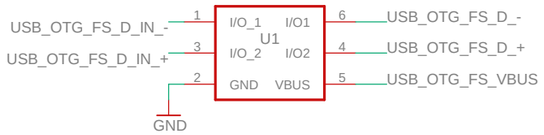
V_IN acceptable range:
4V-17V

Leaving USB shield ungrounded

Diodes D1 & D2 are for isolation between VBUS and 5V reg.

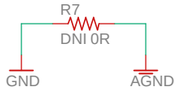


Type A or Type B is determined by state of ID pin.
For A, Tie ID to GND
For B, Leave ID Floating



Unpopulated resitor for connecting grounds internally.

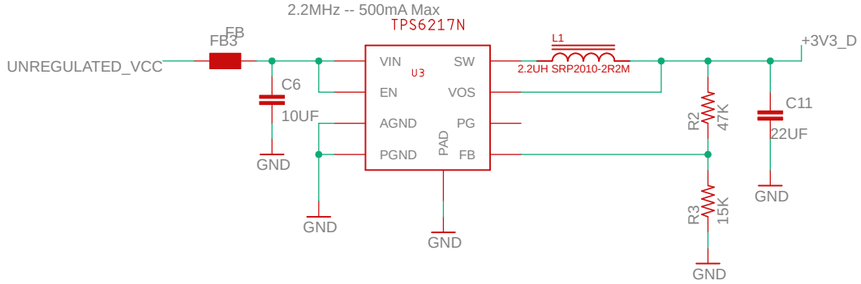
Grounds should be connected outside of Daisy Seed Device.



Power Indicator

+3V3 DIGITAL

2.2MHz -- 500mA Max



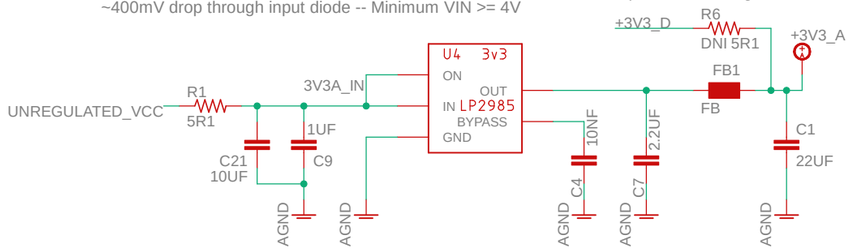
+3V3 ANALOG

Dropout Voltage:
~7mV at 1mA
~280mV at full 150mA

Worst-case Minimum UNREGULATED VCC needs to be 3.58V

~400mV drop through input diode -- Minimum VIN >= 4V

Jumper for connecting 3vd to 3va via RC if 3va circuit wasn't populated.



Power, USB, Pinout

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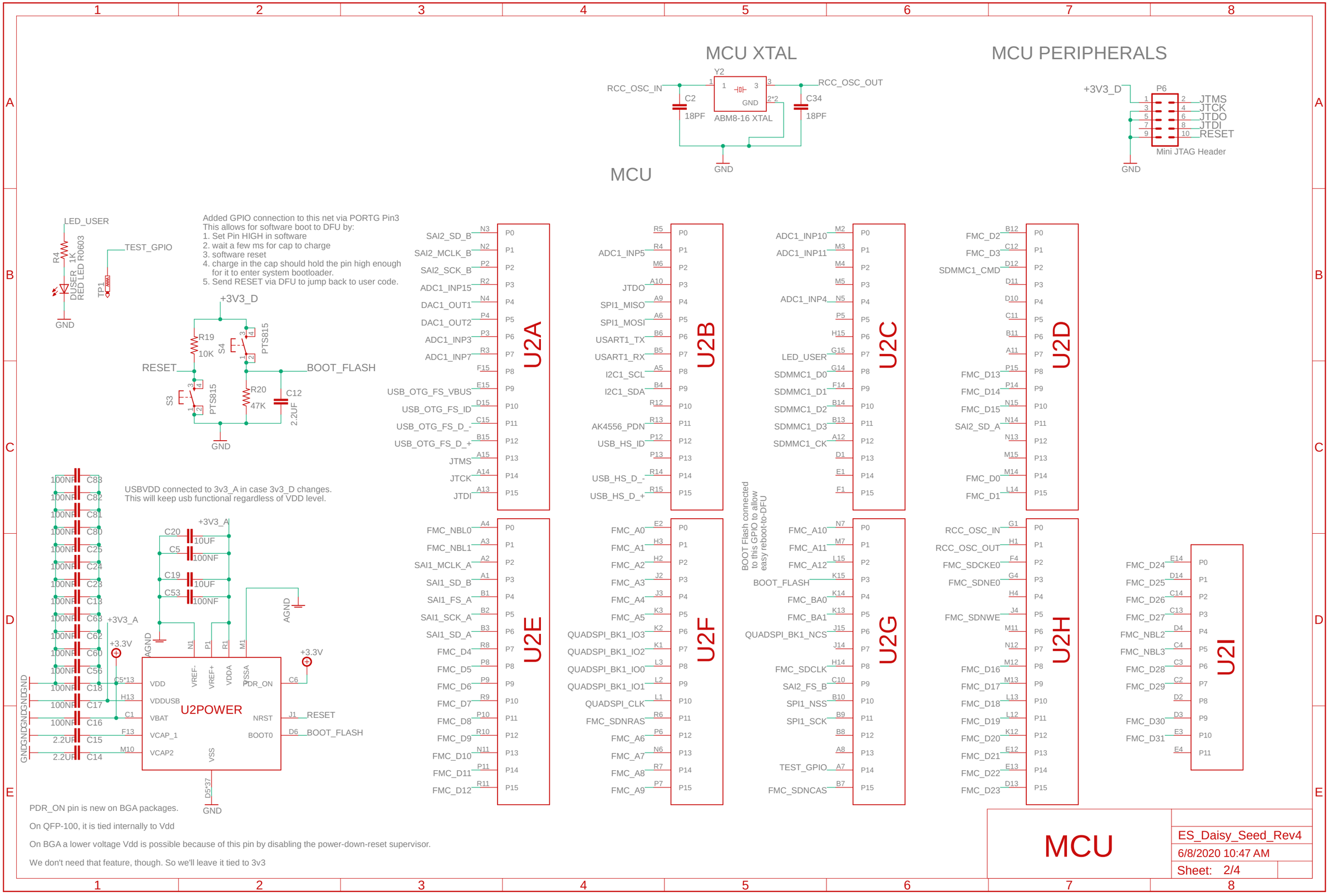
MCU XTAL
Y2
RCC_OSC_IN
RCC_OSC_OUT
C2
18PF
C34
18PF
ABM8-16 XTAL
GND
MCU PERIPHERALS
+3V3_D
P6
JTMS
JTCK
JTDO
JTDI
RESET
Mini JTAG Header
GND
MCU
LED_USER
R4
1K
DUSER
RED LED R0603
TEST_GPIO
TP1
GND
Added GPIO connection to this net via PORTG Pin3
This allows for software boot to DFU by:
1. Set Pin HIGH in software
2. wait a few ms for cap to charge
3. software reset
4. charge in the cap should hold the pin high enough for it to enter system bootloader.
5. Send RESET via DFU to jump back to user code.
+3V3_D
R19
10K
S4
PTS815
RESET
BOOT_FLASH
S3
PTS815
R20
47K
C12
2.2UF
GND
U2A
SAI2_SD_B
SAI2_MCLK_B
SAI2_SCK_B
ADC1_INP15
DAC1_OUT1
DAC1_OUT2
ADC1_INP3
ADC1_INP7
USB_OTG_FS_VBUS
USB_OTG_FS_ID
USB_OTG_FS_D_-
USB_OTG_FS_D_+
JTMS
JTCK
JTDI
U2B
ADC1_INP5
JTDO
SPI1_MISO
SPI1_MOSI
USART1_TX
USART1_RX
I2C1_SCL
I2C1_SDA
AK4556_PDN
USB_HS_ID
USB_HS_D_-
USB_HS_D_+
U2C
ADC1_INP10
ADC1_INP11
ADC1_INP4
LED_USER
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3
SDMMC1_CK
U2D
FMC_D2
FMC_D3
SDMMC1_CMD
FMC_D13
FMC_D14
FMC_D15
SAI2_SD_A
FMC_D0
FMC_D1
100NF C83
100NF C82
100NF C81
100NF C80
100NF C25
100NF C24
100NF C23
100NF C13
100NF C63
100NF C62
100NF C60
100NF C56
100NF C18
100NF C17
100NF C16
2.2UF C15
2.2UF C14
USBVDD connected to 3v3_A in case 3v3_D changes.
This will keep usb functional regardless of VDD level.
+3V3_A
C20
10UF
C5
100NF
C19
10UF
C53
100NF
AGND
+3V3_A
+3.3V
+3.3V
VDD
VDDUSB
VBAT
VCAP_1
VCAP2
VREF-
VREF+
VDDA
VSSA
PDR_ON
NRST
BOOT0
VSS
U2POWER
RESET
BOOT_FLASH
GND
U2E
FMC_NBL0
FMC_NBL1
SAI1_MCLK_A
SAI1_SD_B
SAI1_FS_A
SAI1_SCK_A
SAI1_SD_A
FMC_D4
FMC_D5
FMC_D6
FMC_D7
FMC_D8
FMC_D9
FMC_D10
FMC_D11
FMC_D12
U2F
FMC_A0
FMC_A1
FMC_A2
FMC_A3
FMC_A4
FMC_A5
QUADSPI_BK1_IO3
QUADSPI_BK1_IO2
QUADSPI_BK1_IO0
QUADSPI_BK1_IO1
QUADSPI_CLK
FMC_SDNRAS
FMC_A6
FMC_A7
FMC_A8
FMC_A9
BOOT Flash connected to this GPIO to allow easy reboot-to-DFU
U2G
FMC_A10
FMC_A11
FMC_A12
BOOT_FLASH
FMC_BA0
FMC_BA1
QUADSPI_BK1_NCS
FMC_SDCLK
SAI2_FS_B
SPI1_NSS
SPI1_SCK
TEST_GPIO
FMC_SDNCAS
U2H
RCC_OSC_IN
RCC_OSC_OUT
FMC_SDCKE0
FMC_SDNE0
FMC_SDNWE
FMC_D16
FMC_D17
FMC_D18
FMC_D19
FMC_D20
FMC_D21
FMC_D22
FMC_D23
U2I
FMC_D24
FMC_D25
FMC_D26
FMC_D27
FMC_NBL2
FMC_NBL3
FMC_D28
FMC_D29
FMC_D30
FMC_D31
PDR_ON pin is new on BGA packages.
On QFP-100, it is tied internally to Vdd
On BGA a lower voltage Vdd is possible because of this pin by disabling the power-down-reset supervisor.
We don't need that feature, though. So we'll leave it tied to 3v3
MCU
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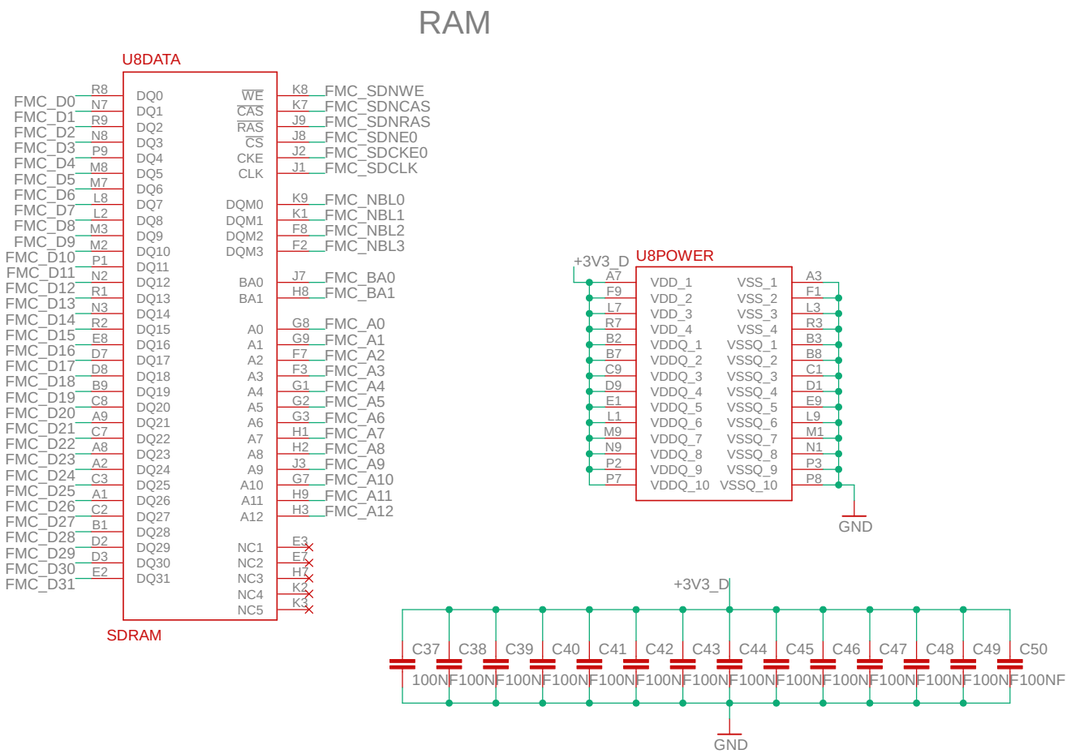

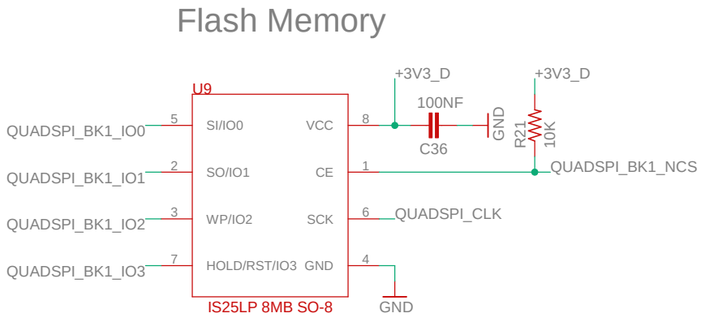

EXT. MEMORIES

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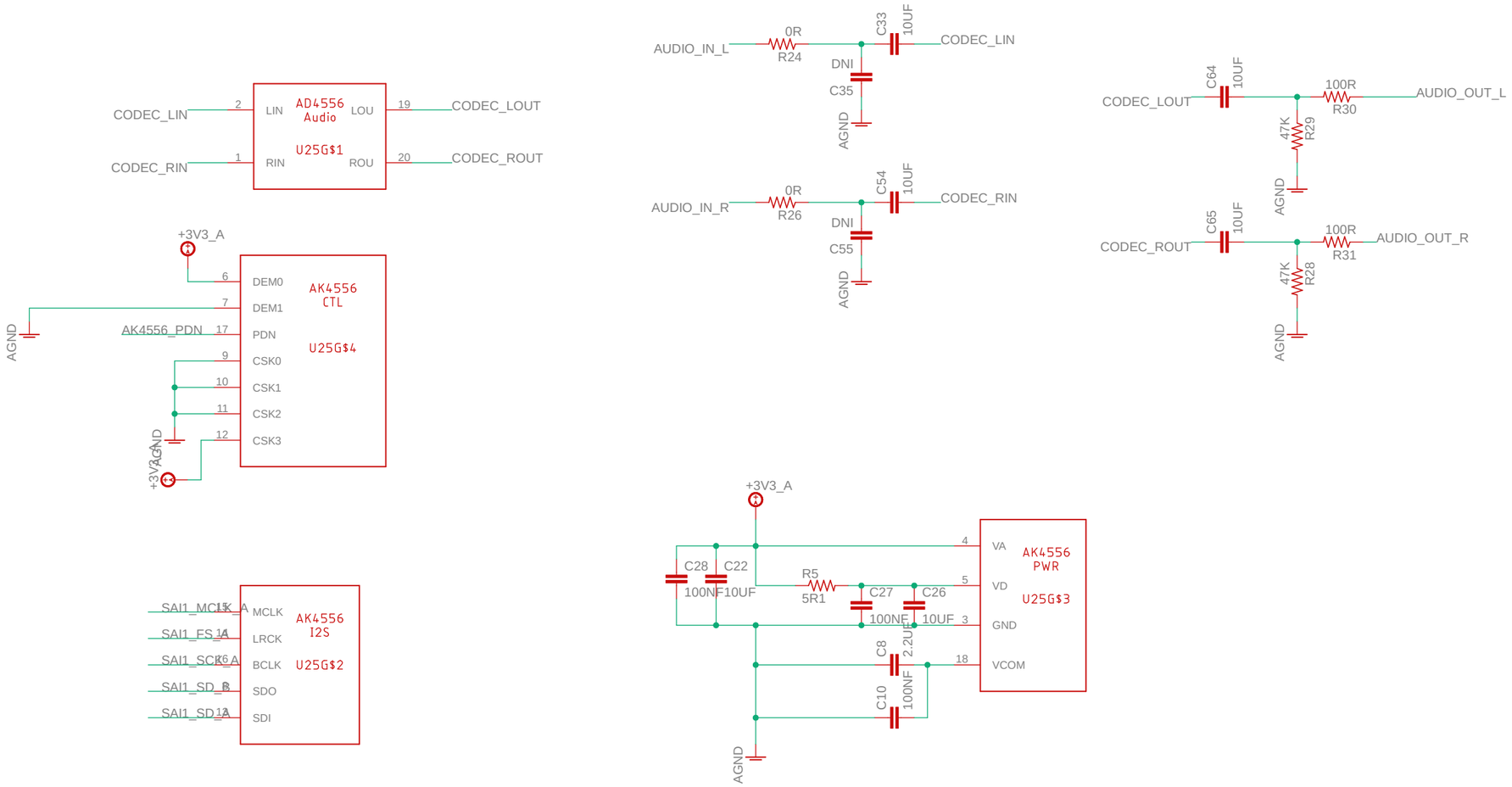

Audio

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