```verilog
always @ (posedge clk or posedge rst)
begin
   if (rst == 1'b1) begin
      cnt = 1'b0 ;
   end else begin
      if (cnt == 1'b1) begin
         cnt = 1'b0 ;
      end else begin
         cnt = cnt + 1'b1 ;
      end
   end
end

always @ (posedge clk or posedge rst)
begin
   if (rst == 1'b1) begin
      r_state <= 128'h55555555_55555555_55555555_55555555 ;
   end
   else begin
         case (cnt)
            1'b0: r_state = 128'h55555555_55555555_55555555_55555555 ;
            1'b1: r_state = 128'hAAAAAAAA_AAAAAAAA_AAAAAAAA_AAAAAAAA ;
         endcase
   end
end
```