

SoC-FPGA Design Guide

Real Time Embedded Systems

LAP – IC – EPFL

Version 0.23 (Preliminary)

Sahand Kashani-Akhavan

René Beuchat

1 TABLE OF CONTENTS

2	List of Figures	2
3	Table of Tables	3
4	Introduction	4
5	Terasic DE1-SoC Board	5
5.1	Specifications	5
5.1.1	FPGA Device	5
5.1.2	Configuration and Debug	5
5.1.3	Memory Device	5
5.1.4	Communication	5
5.1.5	Connectors	6
5.1.6	Display	6
5.1.7	Audio	6
5.1.8	Video Input.....	6
5.1.9	ADC.....	6
5.1.10	Switches, Buttons and Indicators	6
5.1.11	Sensors	6
5.1.12	Power	6
5.1.13	Block Diagram	7
5.2	Layout.....	7
6	Cyclone V Overview	9
6.1	Introduction to the Cyclone V Hard Processor System	9
6.2	Features of the HPS.....	10
6.3	System Integration Overview	11
6.3.1	MPU Subsystem	11
6.3.2	SDRAM Controller Subsystem	11
6.3.3	Support Peripherals.....	11
6.3.4	Interface Peripherals	12
6.3.5	On-Chip Memory.....	12
6.4	HPS-FPGA Interfaces	12
6.5	HPS Address Map	13
6.5.1	HPS Address Spaces	13

6.5.2	HPS Peripheral Region Address Map.....	14
6.6	HPS Booting and FPGA Configuration	15
6.6.1	HPS Boot and FPGA Configuration Ordering.....	16
6.6.2	Zooming In On the HPS Boot Process.....	18
7	Using the Cyclone V.....	19
7.1	Hardware.....	19
7.1.1	FPGA-only.....	19
7.1.2	HPS-only	19
7.2	Software	19
8	todo.....	19
9	Appendix	20
9.1	DE1-SoC Top-level VHDL Entity	20
9.2	DE1-SoC Pin Assignment TCL script.....	23
10	References.....	34
11	SoC part test.....	36
11.1	HPS Architecture	36
11.2	Hardware development	36
11.2.1	Qsys integration.....	36
11.3	Software development.....	38
11.3.1	ARM DS-5 tools	38
11.3.2	Hello World on ARM HPS part.....	38
11.3.3	[3]GPIO access.....	39

2 LIST OF FIGURES

Figure 5-1. Terasic DE1-SoC Board [1]	5
Figure 5-2. Block Diagram of the DE1-SoC Board [1]	7
Figure 5-3. Back [1]	7
Figure 5-4. Front [1]	8
Figure 6-1. Altera SoC FPGA Device Block Diagram [2, pp. 1-1]	9
Figure 6-2. HPS Block Diagram [2, pp. 1-3]	10
Figure 6-3. HPS Address Space Relations [2, pp. 1-14]	13
Figure 6-4. Simplified HPS Boot Flow [2, pp. A-3]	16

Figure 6-5. Independent FPGA Configuration and HPS Booting [2, pp. A-2]	16
Figure 6-6. FPGA Configuration before HPS Booting (HPS boots from FPGA) [2, pp. A-2].....	17
Figure 6-7. HPS Boots and Performs FPGA Configuration [2, pp. A-3]	17
Figure 6-8. HPS Boot Flows [2, pp. A-3]	18
Figure 9-1. DE1-SoC Top-level VHDL Entity	22
Figure 9-2. DE1-SoC Pin Assignment TCL Script	33

3 TABLE OF TABLES

Table 6-1. HPS Address Spaces [2, pp. 1-13]	13
Table 6-2. Common Address Space Regions [2, pp. 1-15].....	13
Table 6-3. HPS Peripheral Region Address Map [2, pp. 1-16]	15

4 INTRODUCTION

The development of embedded systems based on chips containing one or more microprocessors and hardcore peripherals, as well as an FPGA part is becoming more and more important. This technology gives the designer a lot of freedom and powerful abilities. Classical design flows with microcontrollers are emphasized with the full power of FPGAs.

Mixed designs are becoming a reality. One can now design specific accelerators to greatly improve algorithms, or create specific programmable interfaces with the external world.

Two main HDL (**H**ardware **D**esign **L**anguage) languages are available for the design of the FPGA part: **VHDL** and Verilog. There also exist other tools that perform automatic translations from C to HDL. New emerging technologies like OpenCL allow compatibility between high-level software design, and low-level hardware implementations such as:

- Compilation for single or multicore processors
- Compilation for GPUs (Graphical Processing Unit)
- Translation and compilation for FPGAs. The latest models use a PCIe interface or some other way of parameters passing between the main processor and the FPGA

*This guide assumes users know how to use **QUARTUS II**, **NIOS II**, **QSYS** and **MODELSIM-ALTERA**.*

*All hardware and software examples in this guide were made with Quartus II, SoC EDS and Nios II Software Build Tools version **14.0**.*

We will be using the Terasic DE1-SoC board: <http://de1-soc.terasic.com>

5 Terasic DE1-SoC BOARD

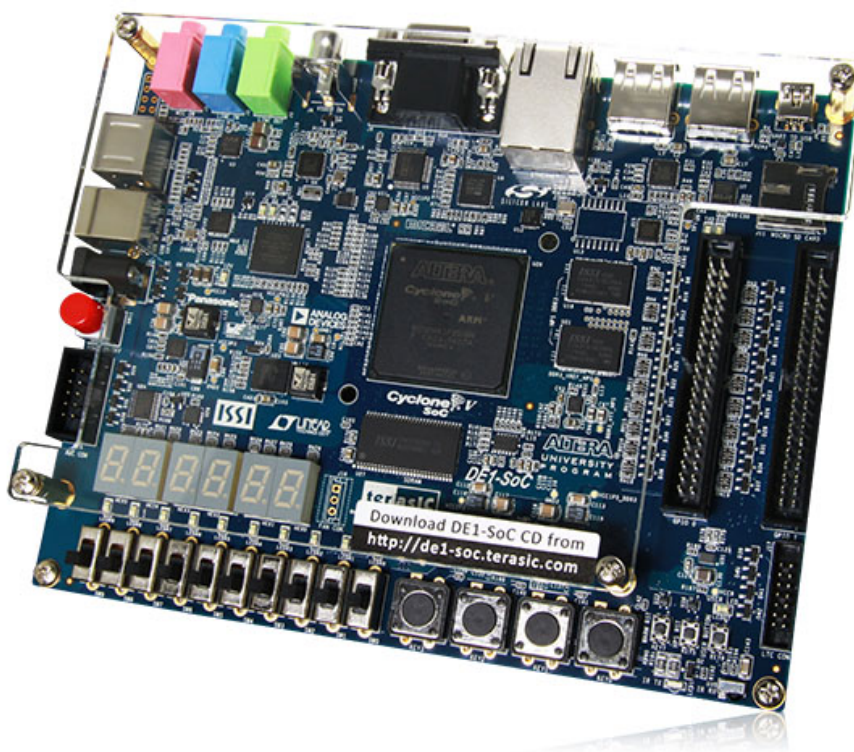


Figure 5-1. Terasic DE1-SoC Board [1]

The DE1-SoC board has many features that allow users to implement a wide range of designed circuits. We will discuss some noteworthy features in this guide.

5.1 SPECIFICATIONS

5.1.1 FPGA Device

- Cyclone V SoC **5CSEMA5F31C6** Device
- Dual-core **ARM CORTEX-A9** (HPS)
- **85K** Programmable Logic Elements
- 4'450 Kbits embedded memory
- 6 Fractional PLLs
- 2 Hard Memory Controllers (only seems to be used for the HPS DDR3 SDRAM, not the FPGA SDRAM)

5.1.2 Configuration and Debug

- Quad Serial Configuration device – **EPCQ256** on FPGA
- On-Board **USB BLASTER II** (Normal type B USB connector)

5.1.3 Memory Device

- **64 MB** (32Mx16) SDRAM on FPGA
- **1 GB** (2x256Mx16) DDR3 SDRAM on HPS
- **MICRO SD** Card Socket on HPS

5.1.4 Communication

- Two Port USB 2.0 Host (ULPI interface with USB type A connector)
- USB to UART (micro USB type B connector)
- 10/100/1000 Ethernet
- PS/2 mouse/keyboard
- IR Emitter/Receiver

5.1.5 Connectors

- Two 40-pin Expansion Headers
- One 10-pin ADC Input Header
- One LTC connector (One Serial Peripheral Interface (SPI) Master, one I2C and one GPIO interface)

5.1.6 Display

- 24-bit VGA DAC

5.1.7 Audio

- 24-bit CODEC, line-in, line-out, and microphone-in jacks

5.1.8 Video Input

- TV Decoder (NTSC/PAL/SECAM) and TV-in connector

5.1.9 ADC

- Fast throughput rate: 1 MSPS
- Channel number: 8
- Resolution: 12 bits
- Analog input range : 0 ~ 2.5 V or 0 ~ 5V as selected via the RANGE bit in the control register

5.1.10 Switches, Buttons and Indicators

- 4 User Keys (FPGA x4)
- 10 User switches (FPGA x10)
- 11 User LEDs (FPGA x10; HPS x 1)
- 2 HPS Reset Buttons (HPS_RST_n and HPS_WARM_RST_n)
- Six 7-segment displays

5.1.11 Sensors

- G-Sensor on HPS

5.1.12 Power

- 12V DC input

5.1.13 Block Diagram

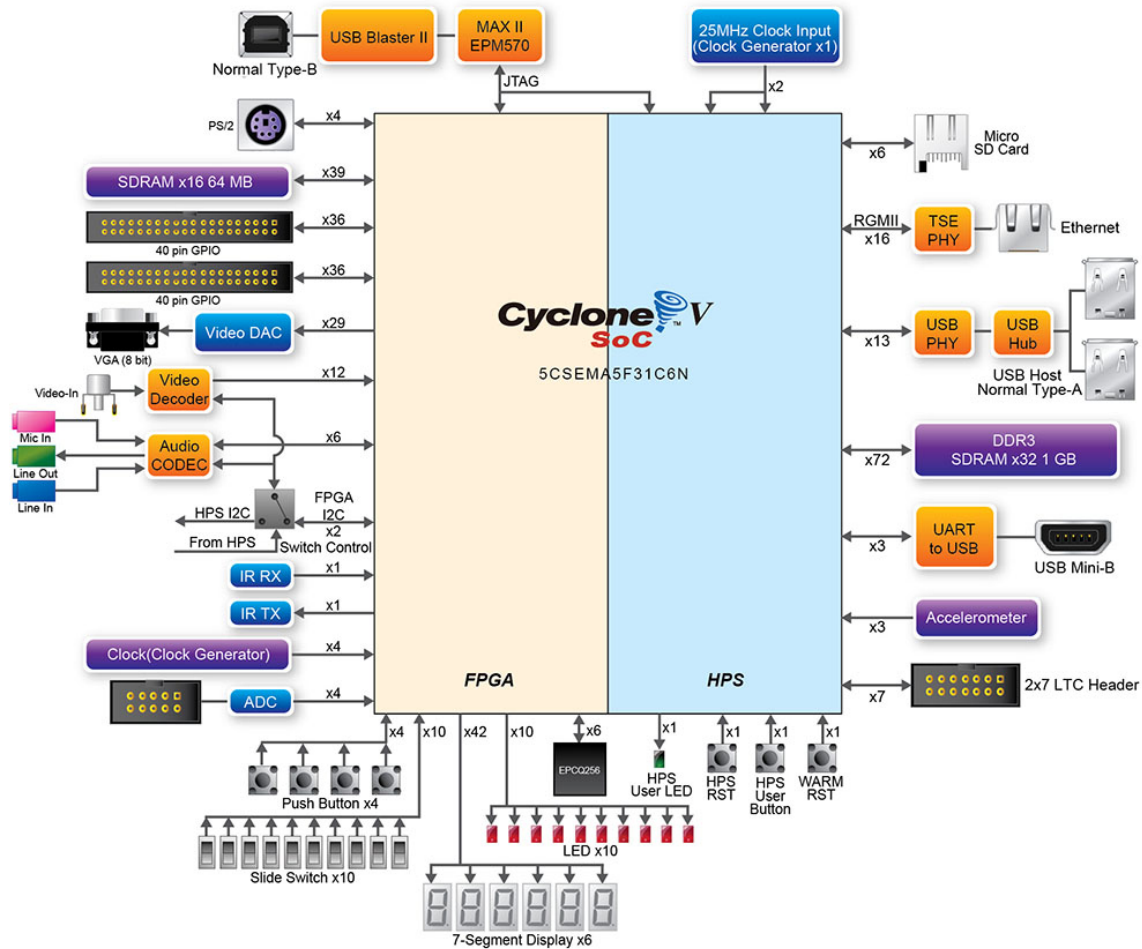


Figure 5-2. Block Diagram of the DE1-SoC Board [1]

5.2 LAYOUT

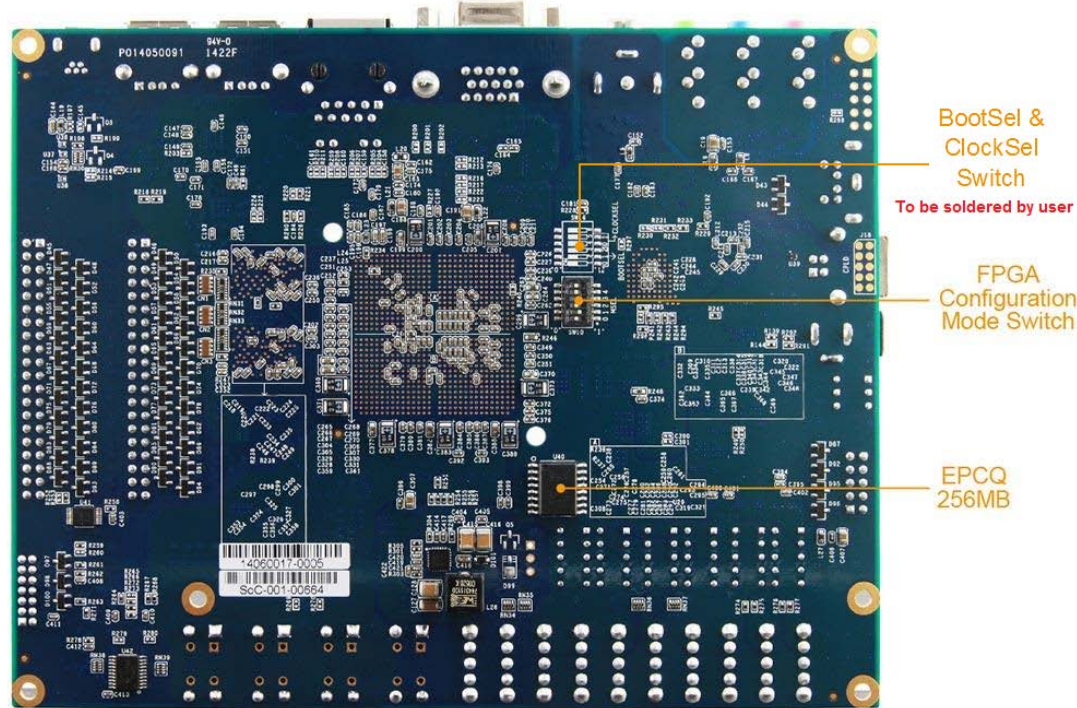


Figure 5-3. Back [1]



Figure 5-4. Front [1]

- Green for peripherals directly connected to the FPGA
- Orange for peripherals directly connected to the HPS
- Blue for board control

Manuals and resources are available on the DE1-SoC [resources](#) page.

6 CYCLONE V OVERVIEW

This section describes some features of the Cyclone V family of devices. We do not list all features, but only the ones most important to us. All information below, along with the most complete documentation regarding this family can be found in the Cyclone V Device Handbook [2].

6.1 INTRODUCTION TO THE CYCLONE V HARD PROCESSOR SYSTEM

The Cyclone V device is a single-die system on a chip (SoC) that consists of two distinct parts – a hard processor system (HPS) portion and an FPGA portion.

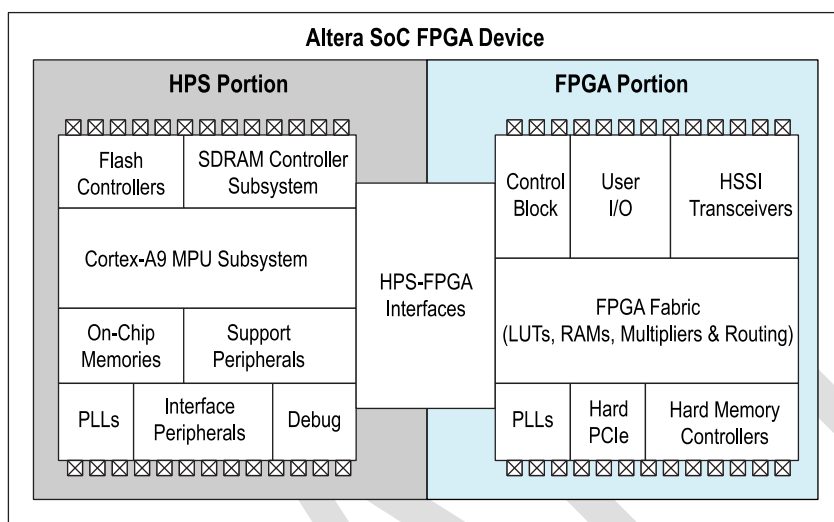


Figure 6-1. Altera SoC FPGA Device Block Diagram [2, pp. 1-1]

The HPS contains a microprocessor unit (MPU) subsystem with single or dual ARM Cortex-A9 MPCore processors, flash memory controllers, SDRAM L3 Interconnect, on-chip memories, support peripherals, interface peripherals, debug capabilities, and phase-locked loops (PLLs). The dual-processor HPS supports symmetric (SMP) and asymmetric (AMP) multiprocessing.

*The DE1-SoC has a **DUAL**-processor HPS.*

The FPGA portion of the device contains the FPGA fabric, a control block (CB), phase-locked loops (PLLs), and depending on the device variant, high-speed serial interface (HSSI) transceivers, hard PCI Express (PCIe) controllers, and hard memory controllers.

The DE1-SoC does not contain any HSSI transceivers, or hard PCIe controllers.

The HPS and FPGA portions of the device are distinctly different. The HPS can boot from multiple sources, including the FPGA fabric and external flash. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

The MPU subsystem can boot from flash devices connected to the HPS pins. Or, when the FPGA portion is configured by an external source, the MPU subsystem can boot from memory available on the FPGA portion of the device.

The HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. The **FPGA I/O PINS** are configured by an **FPGA CONFIGURATION IMAGE** through the HPS or any external source supported by the device. The **HPS I/O PINS** are configured by **SOFTWARE** executing in the HPS. Software executing on the HPS accesses control registers in the Cyclone V system manager to assign HPS I/O pins to the available HPS modules.

The **SOFTWARE** that configures the **HPS I/O PINS** is called the **PRELOADER**.

The HPS and FPGA portions of the device have separate external power supplies and independently power on. You can power on the HPS without powering on the FPGA portion of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion. You can also turn off the FPGA portion of the device while leaving the HPS power on.

6.2 FEATURES OF THE HPS

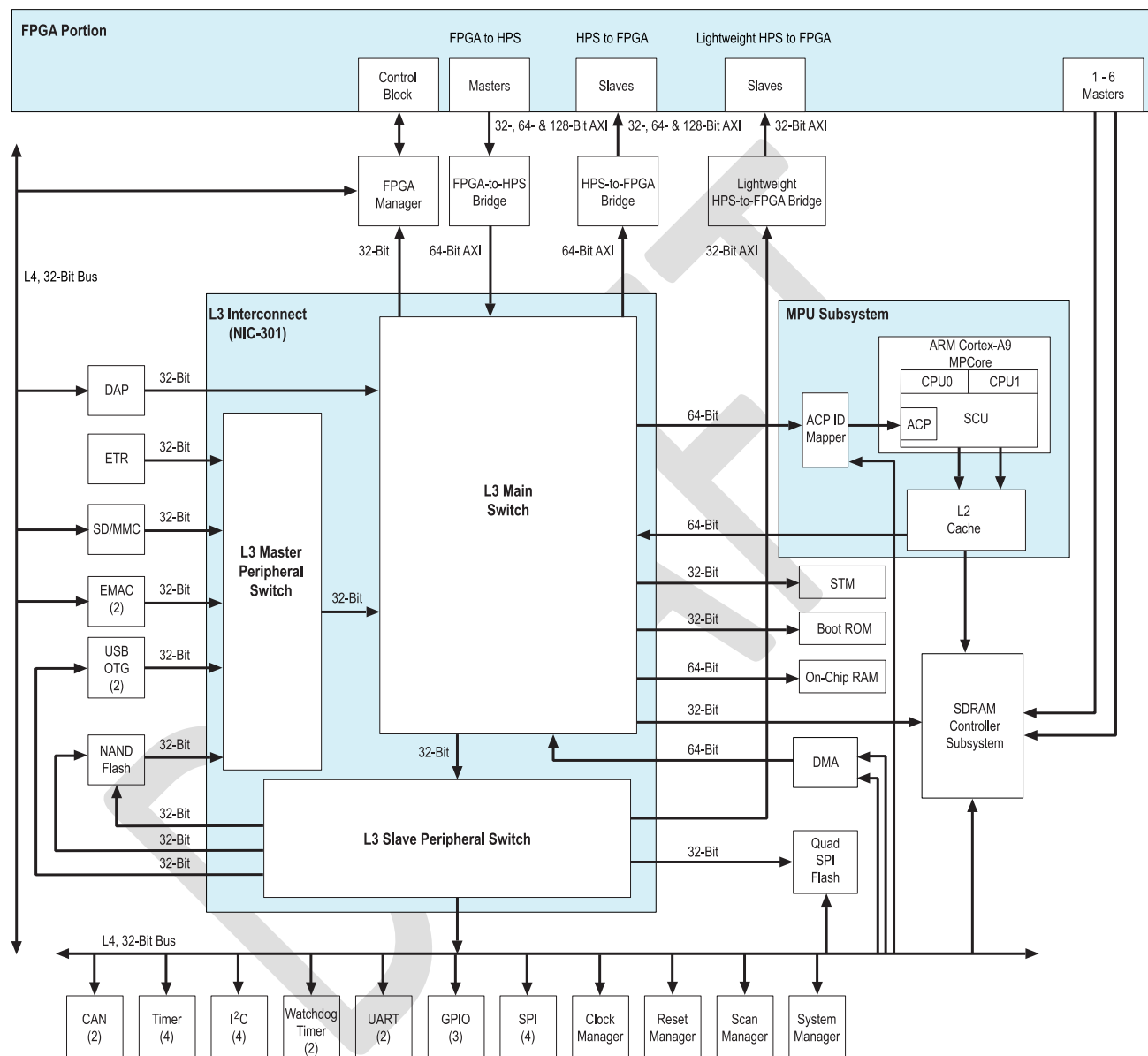


Figure 6-2. HPS Block Diagram [2, pp. 1-3]

The following list contains the main modules of the HPS:

- MPU subsystem featuring dual ARM Cortex-A9 MPCore processors
- General-purpose Direct Memory Access (DMA) controller
- Two Ethernet media access controllers (EMACs)
- Two USB 2.0 On-The-Go (OTG) controllers
- NAND flash controller
- Quad SPI flash controller
- Secure Digital (SD) / MultiMediaCard (MMC) controller

- Two serial peripheral interface (SPI) master controllers
- Two SPI slave controllers
- Four inter-integrated circuit (I²C) controllers
- 64 KB on-chip RAM
- 64 KB on-chip boot ROM
- Two UARTs
- Four timers
- Two watchdog timers
- Three general-purpose I/O (GPIO) interfaces
- Two controller area network (CAN) controllers
- ARM CoreSight debug components
- System manager
- Clock manager
- Reset manager
- Scan manager
- FPGA manager

6.3 SYSTEM INTEGRATION OVERVIEW

In this part, we briefly go through *some* features provided by the most important HPS components.

6.3.1 MPU Subsystem

Here are a few important features of the MPU subsystem:

- Interrupt controller
- One general-purpose timer and one watchdog timer per processor
- One Memory management unit (MMU) per processor

The HPS masters the L3 interconnect and the SDRAM controller subsystem.

6.3.2 SDRAM Controller Subsystem

The SDRAM controller subsystem is **MASTERED** by **HPS MASTERS** and **FPGA FABRIC MASTERS**. It supports DDR2, DDR3, and LPDDR2 devices. It is composed of 2 parts:

- SDRAM controller
- DDR PHY (interfaces the single port memory controller to the HPS I/O)

The DE1-SoC contains DDR3 SDRAM on the HPS

6.3.3 Support Peripherals

6.3.3.1 System Manager

This is one of the most *essential* HPS components. It offers a few important features:

- **PIN MULTIPLEXING** (term used for the **SOFTWARE** configuration of the **HPS I/O PINS** by the **PRE-LOADER**)
- Freeze controller that places I/O elements into a safe state for configuration
- Low-level control of peripheral features not accessible through the control and status registers (CSRs)

*The low-level control of some peripheral features that are not accessible through the CSRs is **NOT** externally documented. You will see this type of code when you generate your custom preloader, but must **NOT** use the constructs in your own code.*

6.3.3.2 *FPGA Manager*

The FPGA manager offers the following features:

- Manages the configuration of the FPGA portion of the device
- Monitors configuration-related signals in the FPGA
- Provides 32 general-purpose inputs and 32 general-purpose outputs to the FPGA fabric

6.3.4 *Interface Peripherals*

6.3.4.1 *GPIO Interfaces*

The HPS provides three GPIO interfaces and offer the following features:

- Supports digital de-bounce
- Configurable interrupt mode
- Supports up to 71 I/O pins and 14 input-only pins, based on device variant
- Supports up to 67 I/O pins and 14 input-only pins

The DE1-SoC has 67 I/O pins and 14 input-only pins

6.3.5 *On-Chip Memory*

*The following on-chip memories are **DIFFERENT** from any on-chip memories located in the FPGA fabric.*

6.3.5.1 *On-Chip RAM*

The on-chip RAM offers the following features:

- 64 KB size
- High performance for all burst lengths

6.3.5.2 *Boot ROM*

The boot ROM offers the following features:

- 64 KB size
- Contains the code required to support HPS boot from cold or warm reset
- Used **EXCLUSIVELY** for booting the HPS

*The code in the boot ROM **CANNOT** be changed.*

6.4 *HPS-FPGA INTERFACES*

The HPS-FPGA interfaces provide a variety of communication channels between the HPS and the FPGA fabric.

The HPS-FPGA interfaces include:

- FPGA-to-HPS bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the FPGA fabric to master transactions to slaves in the HPS. This interface allows the FPGA fabric to have full visibility into the HPS address space.
- HPS-to-FPGA bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the HPS to master transactions to slaves in the FPGA fabric. I will sometimes call this the “*heavyweight*” HPS-to-FPGA bridge to distinguish its “*lightweight*” counterpart (see below).
- Lightweight HPS-to-FPGA bridge – a bus with a 32-bit fixed data width. It allows the HPS to master transactions to slaves in the FPGA fabric.
- FPGA manager interface – signals that communicate with FPGA fabric for boot and configuration.
- Interrupts – allow soft IP to supply interrupts directly to the MPU interrupt controller.
- HPS debug interface – an interface that allows the HPS debug control domain to extend into the FPGA.

6.5 HPS ADDRESS MAP

6.5.1 HPS Address Spaces

The HPS address map specifies the address of slaves, such as memory and peripherals, as viewed by the HPS masters. The HPS has 3 address spaces:

Name	Description	Size
MPU	MPU subsystem	4 GB
L3	L3 interconnect	4 GB
SDRAM	SDRAM controller subsystem	4 GB

Table 6-1. HPS Address Spaces [2, pp. 1-13]

The following figure shows the relationships between the different HPS address spaces. The figure is **NOT** to scale.



Figure 6-3. HPS Address Space Relations [2, pp. 1-14]

The window regions provide access to other address spaces. The thin black arrows indicate which address space is accessed by a window region (arrows point to accessed address space).

The SDRAM window in the MPU can grow and shrink at the top and bottom (short blue vertical arrows) at the expense of the FPGA slaves and boot regions. The ACP window can be mapped to any 1 GB region in the MPU address space (blue vertical bidirectional arrow), on gigabyte-aligned boundaries.

The following table shows the base address and size of each region that is common to the L3 and MPU address spaces.

Region Name	Description	Base Address	Size
FPGA slaves	FPGA slaves connected to the HPS-to-FPGA bridge	0xC0000000	960 MB
HPS peripherals	Slaves directly connected to the HPS (corresponds to all orange colored elements on Figure 5-4 and Figure 5-3)	0xFC000000	64 MB
Lightweight FPGA slaves	FPGA slaves connected to the lightweight HPS-to-FPGA bridge	0xFF200000	2 MB

Table 6-2. Common Address Space Regions [2, pp. 1-15]

6.5.2 HPS Peripheral Region Address Map

The following table lists the slave identifier, slave title, base address, and size of each slave in the HPS peripheral region. The *Slave Identifier* column lists the names used in the HPS register map file provided by Altera (more on this later).

Slave Identifier	Slave Title	Base Address	Size
STM	STM	0xFC000000	48 MB
DAP	DAP	0xFF000000	2 MB
LWFPGASLAVES	FPGA slaves accessed with lightweight HPS-to-FPGA bridge	0xFF200000	2 MB
LWHP2FPGAREGS	Lightweight HPS-to-FPGA bridge GPV	0xFF400000	1 MB
HPS2FPGAREGS	HPS-to-FPGA bridge GPV	0xFF500000	1 MB
FPGA2HPSREGS	FPGA-to-HPS bridge GPV	0xFF600000	1 MB
EMAC0	EMAC0	0xFF700000	8 KB
EMAC1	EMAC1	0xFF702000	8 KB
SDMMC	SD/MMC	0xFF704000	4 KB
QSPIREGS	Quad SPI flash controller registers	0xFF705000	4 KB
FPGAMGRREGS	FPGA manager registers	0xFF706000	4 KB
ACPIDMAP	ACP ID mapper registers	0xFF707000	4 KB
GPIO0	GPIO0	0xFF708000	4 KB
GPIO1	GPIO1	0xFF709000	4 KB
GPIO2	GPIO2	0xFF70A000	4 KB
L3REGS	L3 interconnect GPV	0xFF800000	1 MB
NANDDATA	NAND controller data	0xFF900000	1 MB
QSPIDATA	Quad SPI flash data	0xFFA00000	1 MB
USB0	USB0 OTG controller registers	0xFFB00000	256 KB
USB1	USB1 OTG controller registers	0xFFB40000	256 KB
NANDREGS	NAND controller registers	0xFFB80000	64 KB
FPGAMGRDATA	FPGA manager configuration data	0xFFB90000	4 KB
CAN0	CAN0 controller registers	0xFFC00000	4 KB
CAN1	CAN1 controller registers	0xFFC01000	4 KB
UART0	UART0	0xFFC02000	4 KB
UART1	UART1	0xFFC03000	4 KB
I2C0	I2C0	0xFFC04000	4 KB
I2C1	I2C1	0xFFC05000	4 KB
I2C2	I2C2	0xFFC06000	4 KB
I2C3	I2C3	0xFFC07000	4 KB
SPTIMER0	SP Timer0	0xFFC08000	4 KB
SPTIMER1	SP Timer1	0xFFC09000	4 KB
SDRREGS	SDRAM controller subsystem registers	0xFFC20000	128 KB
OSC1TIMER0	OSC1 Timer0	0xFFD00000	4 KB
OSC1TIMER1	OSC1 Timer1	0xFFD01000	4 KB
L4WD0	Watchdog0	0xFFD02000	4 KB
L4WD1	Watchdog1	0xFFD03000	4 KB
CLKMGR	Clock manager	0xFFD04000	4 KB
RSTMGR	Reset manager	0xFFD05000	4 KB
SYSMGR	System manager	0xFFD08000	16 KB
DMANONSECURE	DMA nonsecure registers	0xFFE00000	4 KB
DMASECURE	DMA secure registers	0xFFE01000	4 KB
SPIS0	SPI slave0	0xFFE02000	4 KB
SPIS1	SPI slave1	0xFFE03000	4 KB
SPIM0	SPI master0	0xFFFF0000	4 KB
SPIM1	SPI master1	0xFFFF01000	4 KB

SCANMGR	Scan manager registers	0xFFFF02000	4 KB
ROM	Boot ROM	0xFFFFD0000	64 KB
MPUSCU	MPU SCU registers	0xFFFFEC000	8 KB
MPUL2	MPU L2 cache controller registers	0xFFFFEF000	4 KB
OCRAM	On-chip RAM	0xFFFFF0000	64 KB

Table 6-3. HPS Peripheral Region Address Map [2, pp. 1-16]

The programming model for accessing the HPS peripherals in Table 6-3 is the same as for peripherals created on the FPGA fabric. That is, every peripheral has a base address at which a certain number of registers can be found. You can then read and write to a certain set of these registers in order to modify the peripheral's behavior.

When using a HPS peripheral in Table 6-3, you do not need to hard-code any base address or peripheral register map in your programs, as Altera provides a header file for each one.

Two directories contain all **HPS**-related **HEADER FILES**:

1. “<altera_install_directory>\embedded\ip\altera\hps\altera_hps\hwlib\include”
Contains **HIGH-LEVEL** header files that typically contain a few **FUNCTIONS** which facilitate control over the HPS components.
2. “<altera_install_directory>\embedded\ip\altera\hps\altera_hps\hwlib\include\socal”
Contains **LOW-LEVEL** header files that provide a peripheral's **BIT-LEVEL REGISTER DETAILS**. For example, any bits in a peripheral's register that correspond to undefined behavior will be specified in these header files.

To illustrate the differences among the high and low-level header files, we can compare the ones related to the FPGA manager peripheral:

1. “...\hwlib\include\alt_fpga_manager.h”

```
ALT_STATUS_CODE alt_fpga_reset_assert(void);
ALT_STATUS_CODE alt_fpga_configure(const void* cfg_buf, size_t cfg_buf_len);
```

2. “...\hwlib\include\socal\alt_fpgamgr.h”

```
/* The width in bits of the ALT_FPGAMGR_CTL_EN register field. */
#define ALT_FPGAMGR_CTL_EN_WIDTH 1
/* The mask used to set the ALT_FPGAMGR_CTL_EN register field value. */
#define ALT_FPGAMGR_CTL_EN_SET_MSK 0x00000001
/* The mask used to clear the ALT_FPGAMGR_CTL_EN register field value. */
#define ALT_FPGAMGR_CTL_EN_CLR_MSK 0xffffffff
```

An **important** header file is “...\hwlib\include\socal\hps.h”. It contains the HPS component's full **REGISTER MAP**, as provided in Table 6-3.

Note however, that there exists **NO HEADER FILE** for the “*heavyweight*” HPS-to-FPGA bridge, as it is not located in the “HPS peripherals” region in Figure 6-3. Indeed, the “*heavyweight*” HPS-to-FPGA bridge is not considered a HPS peripheral, whereas the *lightweight* HPS-to-FPGA bridge is. Therefore, in order to use the “*heavyweight*” HPS-to-FPGA bridge, you will have to define a macro in your code, as follows:

```
#define ALT_HWFGASLVS_OFST 0xc0000000
```

The reason why the “*lightweight*” HPS-to-FPGA bridge is considered a HPS peripheral may be related to the fact that it has a fixed 32-bit bus width (coincidence that this corresponds to the HPS' native data size?)

6.6 HPS BOOTING AND FPGA CONFIGURATION

Before being able to use the Cyclone V SoC, one needs to understand how the HPS boots and how the FPGA is configured. We'll first take a look at the ordering between the HPS and FPGA.

6.6.1 HPS Boot and FPGA Configuration Ordering

The **HPS BOOT** starts when the processor is released from reset (for example, on power up) and executes code in the internal *boot ROM* at the reset exception address. The boot process ends when the code in the boot ROM jumps to the next stage of the boot software. This next stage of the boot software is referred to as the *preloader*. Figure 6-4 illustrates this *initial* incomplete HPS boot flow.



Figure 6-4. Simplified HPS Boot Flow [2, pp. A-3]

The processor can boot from the following sources:

- NAND flash memory through the NAND flash controller
- SD/MMC flash memory through the SD/MMC flash controller
- SPI and QSPI flash memory through the QSPI flash controller using *Slave Select 0*
- FPGA fabric on-chip memory

The choice of the boot source is done by modifying the *BOOTSEL* and *CLKSEL* values **BEFORE THE DEVICE IS POWERED UP**. Therefore, the Cyclone V device normally uses a **PHYSICAL DIP SWITCH** to configure the *BOOTSEL* and *CLKSEL*.

*The DE1-SoC can **ONLY BOOT** from **SD/MMC** flash memory, as its *BOOTSEL* and *CLKSEL* values are hard-wired on the board. Although its HPS contains all necessary controllers, the board doesn't have a physical DIP switch to modify the *BOOTSEL* and *CLKSEL* values. The actual location of the DIP switch is present underneath the board, as can be seen in Figure 5-3, but a switch isn't soldered.*

CONFIGURATION OF THE FPGA portion of the device starts when the FPGA portion is released from reset state (for example, on power up). The control block (CB) in the FPGA portion of the device is responsible for obtaining an FPGA configuration image and configuring the FPGA. The FPGA configuration ends when the configuration image has been fully loaded and the FPGA enters user mode. The FPGA configuration image is provided by users and is typically stored in non-volatile flash-based memory. The FPGA CB can obtain a configuration image from the HPS through the FPGA manager, or from another external source, such as the *Quartus II Programmer*.

The following three figures illustrate the possible HPS boot and FPGA configuration schemes.



Figure 6-5. Independent FPGA Configuration and HPS Booting [2, pp. A-2]

Figure 6-5 shows the scheme where the FPGA configuration and the HPS boot occur independently. The FPGA configuration obtains its image from a non-HPS source (*Quartus II Programmer*), while the HPS boot obtains its configuration image from a non-FPGA fabric source.



Figure 6-6. FPGA Configuration before HPS Booting (HPS boots from FPGA) [2, pp. A-2]

Figure 6-6 shows the scheme where the FPGA is first configured through the *Quartus II Programmer*, then the HPS boots from the FPGA fabric. The HPS boot waits for the FPGA fabric to be powered on and in user mode before executing. The HPS boot ROM code executes the preloader from the FPGA fabric over the HPS-to-FPGA bridge. The preloader can be obtained from the FPGA on-chip memory, or by accessing an external interface (such as a larger external SDRAM).



Figure 6-7. HPS Boots and Performs FPGA Configuration [2, pp. A-3]

Figure 6-7 shows the scheme under which the HPS first boots from one of its non-FPGA fabric boot sources, then software running on the HPS configures the FPGA fabric through the FPGA manager. The software on the HPS obtains the FPGA configuration image from any of its flash memory devices or communication interfaces, such as the SD/MMC memory, or the Ethernet port. The software is provided by users and the boot ROM is not involved in configuring the FPGA fabric.

6.6.2 Zooming In On the HPS Boot Process

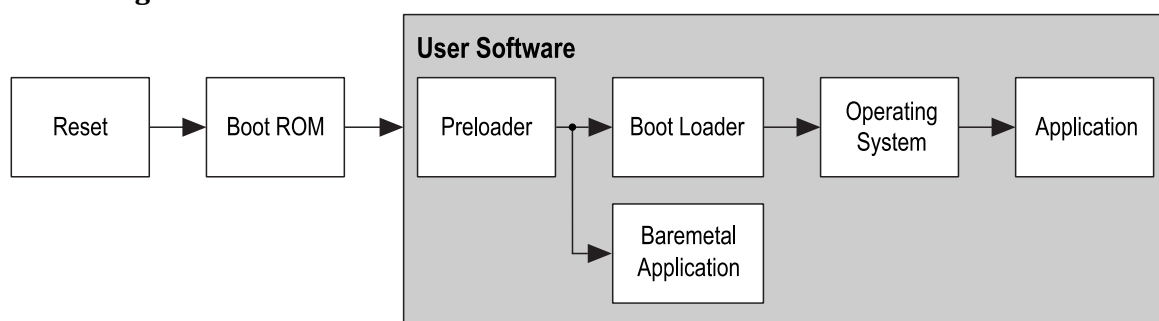


Figure 6-8. HPS Boot Flows [2, pp. A-3]

Booting software on the HPS is a multi-stage process. Each stage is responsible for loading the next stage. The first software stage is the *boot ROM*. The boot ROM code locates and executes the second software stage, called the *preloader*. The preloader locates, and **IF PRESENT**, executes the next software stage. The preloader and subsequent software stages are collectively referred to as *user software*.

The *reset*, *boot ROM*, and *preloader* stages are always present in the HPS boot flow. What comes after the preloader then depends on the type of application you want to run. The HPS can execute 2 types of applications:

- Bare-metal applications (no operating system)
- Applications on top of an operating system (Linux)

Figure 6-8 shows the HPS' available boot flows. The *Reset* and *Boot ROM* stages are the only *fixed* parts of the boot process. Everything in the *user software* stages can be *customized*.

*Although the DE1-SoC has a **DUAL**-processor HPS, CPU1 is under reset, and the boot flow only executes on CPU0. If you want to use both processors of the DE1-SoC, then **USER SOFTWARE** executing on CPU0 is responsible for releasing CPU1 from reset.*

6.6.2.1 Preloader

The preloader is one of the most important boot stages. It is actually what one would call the boot "*source*", as all stages before it are unmodifiable. The preloader can be stored on external flash-based memory, or in the FPGA fabric.

The preloader typically performs the following actions:

- Initialize the SDRAM interface
- Configure the HPS I/O through the scan manager
- Configure pin multiplexing through the system manager
- Configure HPS clocks through the clock manager
- Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
- Load the next boot software into the SDRAM and pass control to it

The preloader does **NOT** release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.

7 USING THE CYCLONE V

7.1 HARDWARE

The HPS component is a **SOFT** component, but it does **NOT** mean that the HPS is a softcore processor. In fact, the HPS exclusively contains **HARD LOGIC**. The reason it is considered a softcore component originates from the fact that it enables other soft components to interface with the HPS hard logic. As such, the HPS component has a *small footprint* in the FPGA fabric, as its only purpose is to connect the soft and hard logic together.

Therefore, it is possible to use the Cyclone V SoC in 3 different configurations:

- FPGA-only
- HPS-only
- HPS & FPGA

We will look at these different configurations below. The configurations using the HPS are more difficult to set up than the FPGA-only one.

7.1.1 FPGA-only

Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA. You can build a complete design in *Quartus II*, simulate it in *ModelSim-Altera*, then program the FPGA through the *Quartus II Programmer*.

The DE1-SoC has a lot of pins, which makes it tedious to start an FPGA design. It is recommended to use the **ENTITY** in Figure 9-1 for your **TOP-LEVEL VHDL FILE**, as it contains all the board's FPGA and HPS pins.

After having defined a top-level module, it is necessary to map your design's pins to the ones available on the DE1-SoC. The **TCL SCRIPT** in Figure 9-2 can be executed in *Quartus II* to specify the board's device ID and all its **PIN ASSIGNMENTS**.

7.1.2 HPS-only

This is where the Cyclone V starts getting complicated to use as many steps are needed before being able to use the HPS.

Bare-metal vs Linux

7.2 SOFTWARE

8 TODO

explain MSEL when reprogramming the FPGA from the HPS.

9 APPENDIX

9.1 DE1-SoC TOP-LEVEL VHDL ENTITY

The DE1-SoC has a lot of pins, which makes it tedious to start an FPGA design. It is recommended to use the following **ENTITY** for your **TOP-LEVEL VHDL FILE**, as it contains all the board's FPGA and HPS pins.

```
entity de1_soc is
  port (
    -- ADC
    ADC_CS_n      : out   std_logic;
    ADC_DIN       : out   std_logic;
    ADC_DOUT      : in    std_logic;
    ADC_SCLK      : out   std_logic;

    -- Audio
    AUD_ADCDAT    : in    std_logic;
    AUD_ADCLRCK   : inout std_logic;
    AUD_BCLK      : inout std_logic;
    AUD_DACDAT    : out   std_logic;
    AUD_ADCLRCK   : inout std_logic;
    AUD_XCK       : out   std_logic;

    -- CLOCK
    CLOCK_50      : in    std_logic;
    CLOCK2_50     : in    std_logic;
    CLOCK3_50     : in    std_logic;
    CLOCK4_50     : in    std_logic;

    -- SDRAM
    DRAM_ADDR     : out   std_logic_vector(12 downto 0);
    DRAM_BA       : out   std_logic_vector(1 downto 0);
    DRAM_CAS_N    : out   std_logic;
    DRAM_CKE      : out   std_logic;
    DRAM_CLK      : out   std_logic;
    DRAM_CS_N     : out   std_logic;
    DRAM_DQ       : inout std_logic_vector(15 downto 0);
    DRAM_LDQM     : out   std_logic;
    DRAM_RAS_N    : out   std_logic;
    DRAM_UDQM     : out   std_logic;
    DRAM_WE_N     : out   std_logic;

    -- I2C for Audio and Video-In
    FPGA_I2C_SCLK : out   std_logic;
    FPGA_I2C_SDAT : inout std_logic;

    -- SEG7
    HEX0          : out   std_logic_vector(6 downto 0);
    HEX1          : out   std_logic_vector(6 downto 0);
    HEX2          : out   std_logic_vector(6 downto 0);
    HEX3          : out   std_logic_vector(6 downto 0);
    HEX4          : out   std_logic_vector(6 downto 0);
    HEX5          : out   std_logic_vector(6 downto 0);

    -- IR
    IRDA_RXD      : in    std_logic;
    IRDA_TXD      : out   std_logic;
```

```

-- KEY
KEY          : in    std_logic_vector(3 downto 0);

-- LED
LEDR         : out   std_logic_vector(9 downto 0);

-- PS2
PS2_CLK      : inout std_logic;
PS2_CLK2     : inout std_logic;
PS2_DAT      : inout std_logic;
PS2_DAT2     : inout std_logic;

-- SW
SW           : in    std_logic_vector(9 downto 0);

-- Video-In
TD_CLK27     : inout std_logic;
TD_DATA      : out   std_logic_vector(7 downto 0);
TD_HS        : out   std_logic;
TD_RESET_N   : out   std_logic;
TD_VS        : out   std_logic;

-- VGA
VGA_B        : out   std_logic_vector(7 downto 0);
VGA_BLANK_N  : out   std_logic;
VGA_CLK      : out   std_logic;
VGA_G        : out   std_logic_vector(7 downto 0);
VGA_HS       : out   std_logic;
VGA_R        : out   std_logic_vector(7 downto 0);
VGA_SYNC_N   : out   std_logic;
VGA_VS       : out   std_logic;

-- GPIO_0, GPIO_0 connect to GPIO Default
GPIO_0       : inout std_logic_vector(35 downto 0);

-- GPIO_1, GPIO_1 connect to GPIO Default
GPIO_1       : inout std_logic_vector(35 downto 0);

-- HPS
HPS_CONV_USB_N : inout std_logic;
HPS_DDR3_ADDR  : out   std_logic_vector(14 downto 0);
HPS_DDR3_BA    : out   std_logic_vector(2 downto 0);
HPS_DDR3_CAS_N : out   std_logic;
HPS_DDR3_CK_N  : out   std_logic;
HPS_DDR3_CK_P  : out   std_logic;
HPS_DDR3_CKE   : out   std_logic;
HPS_DDR3_CS_N  : out   std_logic;
HPS_DDR3_DM    : out   std_logic_vector(3 downto 0);
HPS_DDR3_DQ    : inout std_logic_vector(31 downto 0);
HPS_DDR3_DQS_N : inout std_logic_vector(3 downto 0);
HPS_DDR3_DQS_P : inout std_logic_vector(3 downto 0);
HPS_DDR3_ODT   : out   std_logic;
HPS_DDR3_RAS_N : out   std_logic;
HPS_DDR3_RESET_N : out   std_logic;
HPS_DDR3_RZQ   : in    std_logic;
HPS_DDR3_WE_N  : out   std_logic;
HPS_ENET_GTX_CLK : out   std_logic;
HPS_ENET_INT_N : inout std_logic;
HPS_ENET_MDC   : out   std_logic;

```

```

HPS_ENET_MDIO      : inout std_logic;
HPS_ENET_RX_CLK    : in    std_logic;
HPS_ENET_RX_DATA   : in    std_logic_vector(3 downto 0);
HPS_ENET_RX_DV     : in    std_logic;
HPS_ENET_TX_DATA   : out   std_logic_vector(3 downto 0);
HPS_ENET_TX_EN     : out   std_logic;
HPS_FLASH_DATA     : inout std_logic_vector(3 downto 0);
HPS_FLASH_DCLK     : out   std_logic;
HPS_FLASH_NCSO     : out   std_logic;
HPS_GPIO0          : inout std_logic_vector(1 downto 0);
HPS_GSENSOR_INT    : inout std_logic;
HPS_I2C_CONTROL    : inout std_logic;
HPS_I2C1_SCLK      : inout std_logic;
HPS_I2C1_SDAT      : inout std_logic;
HPS_I2C2_SCLK      : inout std_logic;
HPS_I2C2_SDAT      : inout std_logic;
HPS_KEY            : inout std_logic;
HPS_LED            : inout std_logic;
HPS_SD_CLK         : out   std_logic;
HPS_SD_CMD         : inout std_logic;
HPS_SD_DATA        : inout std_logic_vector(3 downto 0);
HPS_SPIM_CLK       : out   std_logic;
HPS_SPIM_MISO      : in    std_logic;
HPS_SPIM_MOSI      : out   std_logic;
HPS_SPIM_SS        : inout std_logic;
HPS_UART_RX        : in    std_logic;
HPS_UART_TX        : out   std_logic;
HPS_USB_CLKOUT     : in    std_logic;
HPS_USB_DATA       : inout std_logic_vector(7 downto 0);
HPS_USB_DIR        : in    std_logic;
HPS_USB_NXT        : in    std_logic;
HPS_USB_STP        : out   std_logic;
);
end entity de1_soc;

```

Figure 9-1. DE1-SoC Top-level VHDL Entity

9.2 DE1-SoC PIN ASSIGNMENT TCL SCRIPT

After having defined a top-level module, it is necessary to map your design's pins to the ones available on the DE1-SoC. The following **TCL SCRIPT** can be executed in *Quartus II* to specify the board's device ID and all its **PIN ASSIGNMENTS**.

```
set_global_assignment -name FAMILY "Cyclone V"
set_global_assignment -name DEVICE 5CSEMA5F31C6
set_global_assignment -name DEVICE_FILTER_PACKAGE FBGA
set_global_assignment -name DEVICE_FILTER_PIN_COUNT 896
set_global_assignment -name DEVICE_FILTER_SPEED_GRADE 6

#=====
# ADC
#=====
set_location_assignment PIN_AJ4 -to ADC_CS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_CS_N
set_location_assignment PIN_AK4 -to ADC_DIN
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DIN
set_location_assignment PIN_AK3 -to ADC_DOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DOUT
set_location_assignment PIN_AK2 -to ADC_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_SCLK

#=====
# Audio
#=====
set_location_assignment PIN_K7 -to AUD_ADCDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCDAT
set_location_assignment PIN_K8 -to AUD_ADCLRCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCLRCK
set_location_assignment PIN_H7 -to AUD_BCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_BCLK
set_location_assignment PIN_J7 -to AUD_DACDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACDAT
set_location_assignment PIN_H8 -to AUD_DACLCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACLCK
set_location_assignment PIN_G7 -to AUD_XCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_XCK

#=====
# CLOCK
#=====
set_location_assignment PIN_AF14 -to CLOCK_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK_50
set_location_assignment PIN_AA16 -to CLOCK2_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK2_50
set_location_assignment PIN_Y26 -to CLOCK3_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK3_50
set_location_assignment PIN_K14 -to CLOCK4_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK4_50

#=====
# SDRAM
#=====
set_location_assignment PIN_AK14 -to DRAM_ADDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[0]
set_location_assignment PIN_AH14 -to DRAM_ADDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[1]
```



```

set_location_assignment PIN_AG15 -to DRAM_ADDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[2]
set_location_assignment PIN_AE14 -to DRAM_ADDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[3]
set_location_assignment PIN_AB15 -to DRAM_ADDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[4]
set_location_assignment PIN_AC14 -to DRAM_ADDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[5]
set_location_assignment PIN_AD14 -to DRAM_ADDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[6]
set_location_assignment PIN_AF15 -to DRAM_ADDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[7]
set_location_assignment PIN_AH15 -to DRAM_ADDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[8]
set_location_assignment PIN_AG13 -to DRAM_ADDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[9]
set_location_assignment PIN_AG12 -to DRAM_ADDR[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[10]
set_location_assignment PIN_AH13 -to DRAM_ADDR[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[11]
set_location_assignment PIN_AJ14 -to DRAM_ADDR[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[12]
set_location_assignment PIN_AF13 -to DRAM_BA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[0]
set_location_assignment PIN_AJ12 -to DRAM_BA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[1]
set_location_assignment PIN_AF11 -to DRAM_CAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CAS_N
set_location_assignment PIN_AK13 -to DRAM_CKE
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CKE
set_location_assignment PIN_AG11 -to DRAM_CS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CS_N
set_location_assignment PIN_AH12 -to DRAM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CLK
set_location_assignment PIN_AK6 -to DRAM_DQ[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[0]
set_location_assignment PIN_AJ7 -to DRAM_DQ[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[1]
set_location_assignment PIN_AK7 -to DRAM_DQ[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[2]
set_location_assignment PIN_AK8 -to DRAM_DQ[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[3]
set_location_assignment PIN_AK9 -to DRAM_DQ[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[4]
set_location_assignment PIN_AG10 -to DRAM_DQ[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[5]
set_location_assignment PIN_AK11 -to DRAM_DQ[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[6]
set_location_assignment PIN_AJ11 -to DRAM_DQ[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[7]
set_location_assignment PIN_AH10 -to DRAM_DQ[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[8]
set_location_assignment PIN_AJ10 -to DRAM_DQ[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[9]
set_location_assignment PIN_AJ9 -to DRAM_DQ[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[10]
set_location_assignment PIN_AH9 -to DRAM_DQ[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[11]
set_location_assignment PIN_AH8 -to DRAM_DQ[12]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[12]
set_location_assignment PIN_AH7 -to DRAM_DQ[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[13]
set_location_assignment PIN_AJ6 -to DRAM_DQ[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[14]
set_location_assignment PIN_AJ5 -to DRAM_DQ[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[15]
set_location_assignment PIN_AB13 -to DRAM_LDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_LDQM
set_location_assignment PIN_AE13 -to DRAM_RAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_RAS_N
set_location_assignment PIN_AK12 -to DRAM_UDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_UDQM
set_location_assignment PIN_AA13 -to DRAM_WE_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_WE_N

#=====
# I2C for Audio and Video-In
#=====
set_location_assignment PIN_J12 -to FPGA_I2C_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SCLK
set_location_assignment PIN_K12 -to FPGA_I2C_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SDAT

#=====
# SEG7
#=====
set_location_assignment PIN_AE26 -to HEX0[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[0]
set_location_assignment PIN_AE27 -to HEX0[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[1]
set_location_assignment PIN_AE28 -to HEX0[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[2]
set_location_assignment PIN_AG27 -to HEX0[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[3]
set_location_assignment PIN_AF28 -to HEX0[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[4]
set_location_assignment PIN_AG28 -to HEX0[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[5]
set_location_assignment PIN_AH28 -to HEX0[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[6]
set_location_assignment PIN_AJ29 -to HEX1[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[0]
set_location_assignment PIN_AH29 -to HEX1[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[1]
set_location_assignment PIN_AH30 -to HEX1[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[2]
set_location_assignment PIN_AG30 -to HEX1[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[3]
set_location_assignment PIN_AF29 -to HEX1[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[4]
set_location_assignment PIN_AF30 -to HEX1[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[5]
set_location_assignment PIN_AD27 -to HEX1[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[6]
set_location_assignment PIN_AB23 -to HEX2[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[0]
set_location_assignment PIN_AE29 -to HEX2[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[1]

```

```

set_location_assignment PIN_AD29 -to HEX2[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[2]
set_location_assignment PIN_AC28 -to HEX2[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[3]
set_location_assignment PIN_AD30 -to HEX2[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[4]
set_location_assignment PIN_AC29 -to HEX2[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[5]
set_location_assignment PIN_AC30 -to HEX2[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[6]
set_location_assignment PIN_AD26 -to HEX3[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[0]
set_location_assignment PIN_AC27 -to HEX3[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[1]
set_location_assignment PIN_AD25 -to HEX3[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[2]
set_location_assignment PIN_AC25 -to HEX3[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[3]
set_location_assignment PIN_AB28 -to HEX3[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[4]
set_location_assignment PIN_AB25 -to HEX3[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[5]
set_location_assignment PIN_AB22 -to HEX3[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[6]
set_location_assignment PIN_AA24 -to HEX4[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[0]
set_location_assignment PIN_Y23 -to HEX4[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[1]
set_location_assignment PIN_Y24 -to HEX4[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[2]
set_location_assignment PIN_W22 -to HEX4[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[3]
set_location_assignment PIN_W24 -to HEX4[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[4]
set_location_assignment PIN_V23 -to HEX4[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[5]
set_location_assignment PIN_W25 -to HEX4[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[6]
set_location_assignment PIN_V25 -to HEX5[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[0]
set_location_assignment PIN_AA28 -to HEX5[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[1]
set_location_assignment PIN_Y27 -to HEX5[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[2]
set_location_assignment PIN_AB27 -to HEX5[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[3]
set_location_assignment PIN_AB26 -to HEX5[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[4]
set_location_assignment PIN_AA26 -to HEX5[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[5]
set_location_assignment PIN_AA25 -to HEX5[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[6]

#####
# IR
#####
set_location_assignment PIN_AA30 -to IRDA_RXD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_RXD
set_location_assignment PIN_AB30 -to IRDA_TXD

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_TXD

#=====
# KEY
#=====
set_location_assignment PIN_AA14 -to KEY[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[0]
set_location_assignment PIN_AA15 -to KEY[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[1]
set_location_assignment PIN_W15 -to KEY[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[2]
set_location_assignment PIN_Y16 -to KEY[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[3]

#=====
# LED
#=====
set_location_assignment PIN_V16 -to LEDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[0]
set_location_assignment PIN_W16 -to LEDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[1]
set_location_assignment PIN_V17 -to LEDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[2]
set_location_assignment PIN_V18 -to LEDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[3]
set_location_assignment PIN_W17 -to LEDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[4]
set_location_assignment PIN_W19 -to LEDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[5]
set_location_assignment PIN_Y19 -to LEDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[6]
set_location_assignment PIN_W20 -to LEDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[7]
set_location_assignment PIN_W21 -to LEDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[8]
set_location_assignment PIN_Y21 -to LEDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[9]

#=====
# PS2
#=====
set_location_assignment PIN_AD7 -to PS2_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK
set_location_assignment PIN_AD9 -to PS2_CLK2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK2
set_location_assignment PIN_AE7 -to PS2_DAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT
set_location_assignment PIN_AE9 -to PS2_DAT2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT2

#=====
# SW
#=====
set_location_assignment PIN_AB12 -to SW[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[0]
set_location_assignment PIN_AC12 -to SW[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[1]
set_location_assignment PIN_AF9 -to SW[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[2]

```

```

set_location_assignment PIN_AF10 -to SW[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[3]
set_location_assignment PIN_AD11 -to SW[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[4]
set_location_assignment PIN_AD12 -to SW[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[5]
set_location_assignment PIN_AE11 -to SW[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[6]
set_location_assignment PIN_AC9 -to SW[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[7]
set_location_assignment PIN_AD10 -to SW[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[8]
set_location_assignment PIN_AE12 -to SW[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[9]

#=====
# Video-In
#=====
set_location_assignment PIN_H15 -to TD_CLK27
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_CLK27
set_location_assignment PIN_D2 -to TD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[0]
set_location_assignment PIN_B1 -to TD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[1]
set_location_assignment PIN_E2 -to TD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[2]
set_location_assignment PIN_B2 -to TD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[3]
set_location_assignment PIN_D1 -to TD_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[4]
set_location_assignment PIN_E1 -to TD_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[5]
set_location_assignment PIN_C2 -to TD_DATA[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[6]
set_location_assignment PIN_B3 -to TD_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[7]
set_location_assignment PIN_A5 -to TD_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_HS
set_location_assignment PIN_F6 -to TD_RESET_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_RESET_N
set_location_assignment PIN_A3 -to TD_VS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_VS

#=====
# VGA
#=====
set_location_assignment PIN_B13 -to VGA_B[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[0]
set_location_assignment PIN_G13 -to VGA_B[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[1]
set_location_assignment PIN_H13 -to VGA_B[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[2]
set_location_assignment PIN_F14 -to VGA_B[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[3]
set_location_assignment PIN_H14 -to VGA_B[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[4]
set_location_assignment PIN_F15 -to VGA_B[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[5]
set_location_assignment PIN_G15 -to VGA_B[6]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[6]
set_location_assignment PIN_J14 -to VGA_B[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[7]
set_location_assignment PIN_F10 -to VGA_BLANK_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_BLANK_N
set_location_assignment PIN_A11 -to VGA_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_CLK
set_location_assignment PIN_J9 -to VGA_G[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[0]
set_location_assignment PIN_J10 -to VGA_G[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[1]
set_location_assignment PIN_H12 -to VGA_G[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[2]
set_location_assignment PIN_G10 -to VGA_G[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[3]
set_location_assignment PIN_G11 -to VGA_G[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[4]
set_location_assignment PIN_G12 -to VGA_G[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[5]
set_location_assignment PIN_F11 -to VGA_G[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[6]
set_location_assignment PIN_E11 -to VGA_G[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[7]
set_location_assignment PIN_B11 -to VGA_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_HS
set_location_assignment PIN_A13 -to VGA_R[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[0]
set_location_assignment PIN_C13 -to VGA_R[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[1]
set_location_assignment PIN_E13 -to VGA_R[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[2]
set_location_assignment PIN_B12 -to VGA_R[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[3]
set_location_assignment PIN_C12 -to VGA_R[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[4]
set_location_assignment PIN_D12 -to VGA_R[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[5]
set_location_assignment PIN_E12 -to VGA_R[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[6]
set_location_assignment PIN_F13 -to VGA_R[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[7]
set_location_assignment PIN_C10 -to VGA_SYNC_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_SYNC_N
set_location_assignment PIN_D11 -to VGA_VS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_VS

#=====
# HPS
#=====
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_GTX_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_INT_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_MDC
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_MDIO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DV

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_EN
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_NCS0
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GPIO[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GPIO[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GSENSOR_INT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C_CONTROL
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_KEY
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LED
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CMD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MISO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MOSI
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_SS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_RX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_TX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_CLKOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DIR
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_NXT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_STP
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_CONV_USB_N

#=====
# GPIO_0, GPIO_0 connect to GPIO Default
#=====
set_location_assignment PIN_AC18 -to GPIO_0[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[0]
set_location_assignment PIN_Y17 -to GPIO_0[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[1]
set_location_assignment PIN_AD17 -to GPIO_0[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[2]
set_location_assignment PIN_Y18 -to GPIO_0[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[3]
set_location_assignment PIN_AK16 -to GPIO_0[4]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[4]
set_location_assignment PIN_AK18 -to GPIO_0[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[5]
set_location_assignment PIN_AK19 -to GPIO_0[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[6]
set_location_assignment PIN_AJ19 -to GPIO_0[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[7]
set_location_assignment PIN_AJ17 -to GPIO_0[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[8]
set_location_assignment PIN_AJ16 -to GPIO_0[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[9]
set_location_assignment PIN_AH18 -to GPIO_0[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[10]
set_location_assignment PIN_AH17 -to GPIO_0[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[11]
set_location_assignment PIN_AG16 -to GPIO_0[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[12]
set_location_assignment PIN_AE16 -to GPIO_0[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[13]
set_location_assignment PIN_AF16 -to GPIO_0[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[14]
set_location_assignment PIN_AG17 -to GPIO_0[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[15]
set_location_assignment PIN_AA18 -to GPIO_0[16]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[16]
set_location_assignment PIN_AA19 -to GPIO_0[17]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[17]
set_location_assignment PIN_AE17 -to GPIO_0[18]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[18]
set_location_assignment PIN_AC20 -to GPIO_0[19]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[19]
set_location_assignment PIN_AH19 -to GPIO_0[20]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[20]
set_location_assignment PIN_AJ20 -to GPIO_0[21]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[21]
set_location_assignment PIN_AH20 -to GPIO_0[22]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[22]
set_location_assignment PIN_AK21 -to GPIO_0[23]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[23]
set_location_assignment PIN_AD19 -to GPIO_0[24]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[24]
set_location_assignment PIN_AD20 -to GPIO_0[25]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[25]
set_location_assignment PIN_AE18 -to GPIO_0[26]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[26]
set_location_assignment PIN_AE19 -to GPIO_0[27]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[27]
set_location_assignment PIN_AF20 -to GPIO_0[28]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[28]
set_location_assignment PIN_AF21 -to GPIO_0[29]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[29]
set_location_assignment PIN_AF19 -to GPIO_0[30]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[30]
set_location_assignment PIN_AG21 -to GPIO_0[31]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[31]
set_location_assignment PIN_AF18 -to GPIO_0[32]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[32]
set_location_assignment PIN_AG20 -to GPIO_0[33]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[33]

```



```

set_location_assignment PIN_AG18 -to GPIO_0[34]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[34]
set_location_assignment PIN_AJ21 -to GPIO_0[35]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[35]

#=====
# GPIO_1, GPIO_1 connect to GPIO Default
#=====
set_location_assignment PIN_AB17 -to GPIO_1[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[0]
set_location_assignment PIN_AA21 -to GPIO_1[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[1]
set_location_assignment PIN_AB21 -to GPIO_1[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[2]
set_location_assignment PIN_AC23 -to GPIO_1[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[3]
set_location_assignment PIN_AD24 -to GPIO_1[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[4]
set_location_assignment PIN_AE23 -to GPIO_1[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[5]
set_location_assignment PIN_AE24 -to GPIO_1[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[6]
set_location_assignment PIN_AF25 -to GPIO_1[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[7]
set_location_assignment PIN_AF26 -to GPIO_1[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[8]
set_location_assignment PIN_AG25 -to GPIO_1[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[9]
set_location_assignment PIN_AG26 -to GPIO_1[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[10]
set_location_assignment PIN_AH24 -to GPIO_1[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[11]
set_location_assignment PIN_AH27 -to GPIO_1[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[12]
set_location_assignment PIN_AJ27 -to GPIO_1[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[13]
set_location_assignment PIN_AK29 -to GPIO_1[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[14]
set_location_assignment PIN_AK28 -to GPIO_1[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[15]
set_location_assignment PIN_AK27 -to GPIO_1[16]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[16]
set_location_assignment PIN_AJ26 -to GPIO_1[17]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[17]
set_location_assignment PIN_AK26 -to GPIO_1[18]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[18]
set_location_assignment PIN_AH25 -to GPIO_1[19]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[19]
set_location_assignment PIN_AJ25 -to GPIO_1[20]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[20]
set_location_assignment PIN_AJ24 -to GPIO_1[21]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[21]
set_location_assignment PIN_AK24 -to GPIO_1[22]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[22]
set_location_assignment PIN_AG23 -to GPIO_1[23]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[23]
set_location_assignment PIN_AK23 -to GPIO_1[24]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[24]
set_location_assignment PIN_AH23 -to GPIO_1[25]

```

```
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[25]
set_location_assignment PIN_AK22 -to GPIO_1[26]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[26]
set_location_assignment PIN_AJ22 -to GPIO_1[27]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[27]
set_location_assignment PIN_AH22 -to GPIO_1[28]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[28]
set_location_assignment PIN_AG22 -to GPIO_1[29]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[29]
set_location_assignment PIN_AF24 -to GPIO_1[30]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[30]
set_location_assignment PIN_AF23 -to GPIO_1[31]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[31]
set_location_assignment PIN_AE22 -to GPIO_1[32]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[32]
set_location_assignment PIN_AD21 -to GPIO_1[33]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[33]
set_location_assignment PIN_AA20 -to GPIO_1[34]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[34]
set_location_assignment PIN_AC22 -to GPIO_1[35]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[35]
```

Figure 9-2. DE1-SoC Pin Assignment TCL Script

10 REFERENCES

- [1] Terasic Technologies, "Terasic - DE Main Boards - Cyclone - DE1-SoC Board," [Online]. Available: <http://de1-soc.terasic.com>.
- [2] Altera Corporation, "Cyclone V Device Handbook, Volume 3: Hard Processor System Technical Reference Manual," 31 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf.
- [3] Altera Corporation, "Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration," 22 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_5v2.pdf.
- [4] Altera Corporation, "Documentation: Cyclone V Devices," [Online]. Available: http://www.altera.com/literature/lit-cyclone-v.jsp?ln=devices_fpga&l3=Low-Cost%20FPGAs-Cyclone%20V%20%28E,%20GX,%20GT,%20SE,%20SX,%20ST%29&l4=Documentation.
- [5] Altera Corporation, "Address Map for HPS," [Online]. Available: <http://www.altera.com/literature/hb/cyclone-v/hps.html>.
- [6] Altera Corporation, "A Look Inside: SoC FPGAs Embedded Development Tools (Part 5 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=NxZznvf5EKc>.
- [7] Altera Corporation, "A Look Inside: SoC FPGAs Introduction (Part 1 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=RVM-ESUMOMU>.
- [8] Altera Corporation, "A Look Inside: SoC FPGAs Reliability and Flexibility (Part 3 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=cWlaqt2RU84>.
- [9] Altera Corporation, "A Look Inside: SoC FPGAs System Cost and Power (Part 4 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=gUE669XKhUY>.
- [10] Altera Corporation, "A Look Inside: SoC FPGAs System Performance (Part 2 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=Ssxf8ggmQk4>.
- [11] Altera Corporation, "Cyclone V Device Datasheet," July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_51002.pdf.
- [12] ARM, "DS-5 Altera Edition: Bare-metal Debug and Trace," 21 October 2013. [Online]. Available: http://www.youtube.com/watch?v=u_xKybPhcHI.
- [13] ARM, "FPGA-adaptive debug on the Altera SoC using ARM DS-5," 16 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=2NBcUv2Txbl>.
- [14] EE Journal, "OpenCL on FPGAs Accelerating Performance and Design Productivity -- Altera," 28 November 2013. [Online]. Available: http://www.youtube.com/watch?v=M6vpq6s1h_A.
- [15] Altera Corporation, "Bare-Metal Debugging using ARM DS-5 Altera Edition," 3 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=CJ0EHJ9oQ7Y>.
- [16] Altera Corporation, "Cyclone V Device Overview," 7 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_51001.pdf.

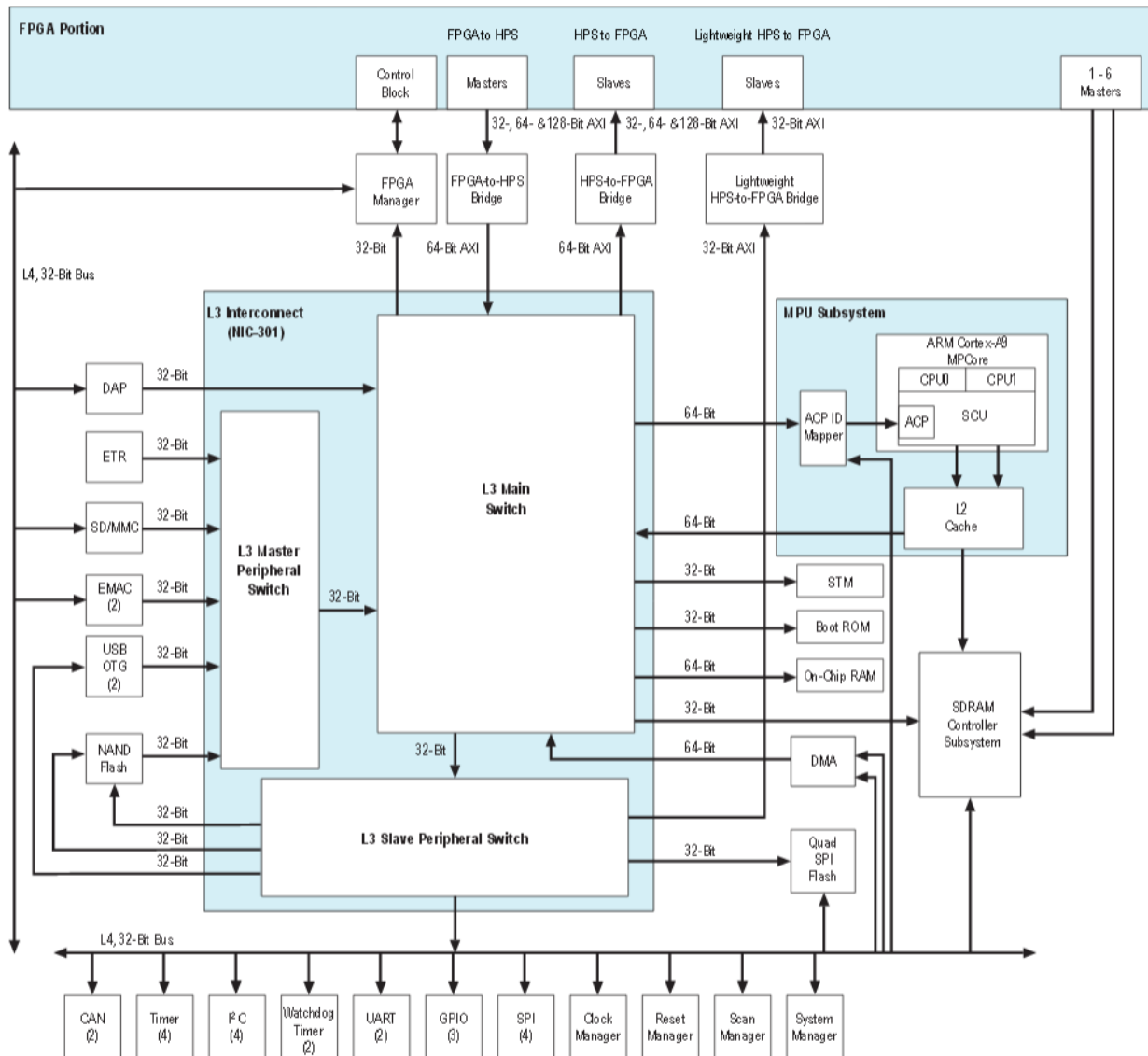
[17] Altera Corporation, "Linux Kernel Debug using ARM DS-5 Altera Edition," 3 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=QcA39O6ofGw>.

DRAFT

11 SoC PART TEST

11.1 HPS ARCHITECTURE

To be able to program the ARM9's processors it is almost necessary to have the global view of the HPS architecture.



11.2 HARDWARE DEVELOPMENT

11.2.1 Qsys integration

Starting with **QuartusII** and after creating a project, select **Tools → Qsys**

In **Qsys**, open **Library → Embedded Processors → Hard Processor System** the window with description of the parameters for the HPS is open.

The **FPGA Interface** tab allows the access from to the FPGA part with the HPS part.

Hard Processor System
altera_hps

Block Diagram
Show signals

FPGA Interfaces | Peripheral Pin Multiplexing | HPS Clocks | SDRAM

General

- ☐ Enable MPU standby and event signals
- ☒ Enable MPU general purpose signals
- ☐ Enable Debug APB interface
- ☐ Enable System Trace Macrocell hardware events
- ☐ Enable FPGA Cross Trigger Interface
- ☐ Enable FPGA Trace Port Interface Unit
- ☐ Enable boot from fpga signals
- ☐ Enable H.LGPI Interface

AXI Bridges

FPGA-to-HPS interface width: 64-bit
HPS-to-FPGA interface width: 64-bit
Lightweight HPS-to-FPGA interface width: 32-bit

FPGA-to-HPS SDRAM Interface

Click the '+' and '-' buttons to add and remove FPGA-to-HPS SDRAM ports.

Name	Type	Width
f2h_sram0	SDRAM	16

Resets

- ☐ Enable HPS-to-FPGA cold reset output
- ☐ Enable HPS warm reset handshake signals
- ☐ Enable FPGA-to-HPS debug reset request
- ☐ Enable FPGA-to-HPS warm reset request
- ☐ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	No
1	No
2	No
3	No
4	No
5	No

Presets

Project Library

- ELPIDA EDJ1108BASE-8C
- ELPIDA EDJ5308BASE-8C
- JEDEC DDR2-1066 256MB X8
- JEDEC DDR2-1066 512MB X8
- JEDEC DDR2-400 256MB X8
- JEDEC DDR2-400 512MB X8
- JEDEC DDR2-533 256MB X8
- JEDEC DDR2-533 512MB X8
- JEDEC DDR2-667 256MB X8
- JEDEC DDR2-667 512MB X8
- JEDEC DDR2-800 256MB X8
- JEDEC DDR2-800 512MB X8
- JEDEC DDR3-1066E 1GB X8
- JEDEC DDR3-1066E 2GB X8
- JEDEC DDR3-1066E 512MB X8
- JEDEC DDR3-1066F 1GB X8
- JEDEC DDR3-1066F 2GB X8
- JEDEC DDR3-1066F 512MB X8
- JEDEC DDR3-1066G 1GB X8
- JEDEC DDR3-1066G 2GB X8
- JEDEC DDR3-1066G 512MB X8
- JEDEC DDR3-1G4 1GB X8
- JEDEC DDR3-1G4 2GB X8
- JEDEC DDR3-1G6 1GB X8
- JEDEC DDR3-1G6 2GB X8
- JEDEC DDR3-800D 1GB X8
- JEDEC DDR3-800D 2GB X8
- JEDEC DDR3-800D 512MB X8
- JEDEC DDR3-800E 1GB X8
- JEDEC DDR3-800E 2GB X8
- JEDEC DDR3-800E 512MB X8
- JEDEC DDR3L-1066E 1GB X8
- JEDEC DDR3L-1066E 2GB X8
- JEDEC DDR3L-1066E 512MB X8
- JEDEC DDR3L-1066F 1GB X8
- JEDEC DDR3L-1066F 2GB X8
- JEDEC DDR3L-1066F 512MB X8
- JEDEC DDR3L-1066G 1GB X8
- JEDEC DDR3L-1066G 2GB X8
- JEDEC DDR3L-1066G 512MB X8
- JEDEC DDR3L-1G4 2GB X8
- JEDEC DDR3L-1G6 2GB X8
- JEDEC DDR3L-800D 1GB X8
- JEDEC DDR3L-800D 2GB X8
- JEDEC DDR3L-800D 512MB X8
- JEDEC DDR3L-800E 1GB X8
- JEDEC DDR3L-800E 2GB X8
- JEDEC DDR3L-800E 512MB X8
- MICRON MT41128M16HA-15E

Hard Processor System
altera_hps

Block Diagram
Show signals

Resets

- ☐ Enable HPS-to-FPGA cold reset output
- ☐ Enable HPS warm reset handshake signals
- ☐ Enable FPGA-to-HPS debug reset request
- ☐ Enable FPGA-to-HPS warm reset request
- ☐ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	No
1	No
2	No
3	No
4	No
5	No

Interrupts

- ☐ Enable FPGA-to-HPS Interrupts

HPS-to-FPGA

- ☐ Enable CAN interrupts
- ☐ Enable clock peripheral interrupts
- ☐ Enable CTI interrupts
- ☐ Enable DMA interrupts
- ☐ Enable EMAC interrupts
- ☐ Enable FPGA manager interrupt
- ☐ Enable GPIO interrupts
- ☐ Enable I2C-EMAC interrupts
- ☐ Enable I2C peripheral interrupts
- ☐ Enable L4 timer interrupts
- ☐ Enable NAND interrupt
- ☐ Enable OSC timer interrupts
- ☐ Enable QSPI interrupt
- ☐ Enable SD/MMC interrupt
- ☐ Enable SPI master interrupts
- ☐ Enable SPI slave interrupts
- ☐ Enable UART interrupts
- ☐ Enable USB interrupts
- ☐ Enable watchdog interrupts

Presets

Project Library

- ELPIDA EDJ1108BASE-8C
- ELPIDA EDJ5308BASE-8C
- JEDEC DDR2-1066 256MB X8
- JEDEC DDR2-1066 512MB X8
- JEDEC DDR2-400 256MB X8
- JEDEC DDR2-400 512MB X8
- JEDEC DDR2-533 256MB X8
- JEDEC DDR2-533 512MB X8
- JEDEC DDR2-667 256MB X8
- JEDEC DDR2-667 512MB X8
- JEDEC DDR2-800 256MB X8
- JEDEC DDR2-800 512MB X8
- JEDEC DDR3-1066E 1GB X8
- JEDEC DDR3-1066E 2GB X8
- JEDEC DDR3-1066F 1GB X8
- JEDEC DDR3-1066F 2GB X8
- JEDEC DDR3-1066F 512MB X8
- JEDEC DDR3-1066G 1GB X8
- JEDEC DDR3-1066G 2GB X8
- JEDEC DDR3-1066G 512MB X8
- JEDEC DDR3-1G4 1GB X8
- JEDEC DDR3-1G4 2GB X8
- JEDEC DDR3-1G6 1GB X8
- JEDEC DDR3-1G6 2GB X8
- JEDEC DDR3-800D 1GB X8
- JEDEC DDR3-800D 2GB X8
- JEDEC DDR3-800D 512MB X8
- JEDEC DDR3-800E 1GB X8
- JEDEC DDR3-800E 2GB X8
- JEDEC DDR3-800E 512MB X8
- JEDEC DDR3L-1066E 1GB X8
- JEDEC DDR3L-1066E 2GB X8
- JEDEC DDR3L-1066E 512MB X8
- JEDEC DDR3L-1066F 1GB X8
- JEDEC DDR3L-1066F 2GB X8
- JEDEC DDR3L-1066F 512MB X8
- JEDEC DDR3L-1066G 1GB X8
- JEDEC DDR3L-1066G 2GB X8
- JEDEC DDR3L-1066G 512MB X8
- JEDEC DDR3L-1G4 2GB X8
- JEDEC DDR3L-1G6 2GB X8
- JEDEC DDR3L-800D 1GB X8
- JEDEC DDR3L-800D 2GB X8
- JEDEC DDR3L-800D 512MB X8
- JEDEC DDR3L-800E 1GB X8
- JEDEC DDR3L-800E 2GB X8
- JEDEC DDR3L-800E 512MB X8
- MICRON MT41128M16HA-15E
- MICRON MT41128M16HA-187E
- MICRON MT41128M16HA-187F

Apply Update... Delete

With the **PeripheralPin Multiplexing**, some I/O interface can be used by the HPS part or the FPGA part. The selection is done here.

11.3 SOFTWARE DEVELOPMENT

11.3.1 ARM DS-5 tools

They are some differences between the versions of DS-5.

The one installed for the test is:

ARM DS-5 (DS-5 Altera Edition (Evaluation))
Version: 5.18.0
Build number: 5180018

11.3.2 Hello World on ARM HPS part

Copy the directory from Altera examples:

C:\altera\13.1\embedded\examples\software

And un-gz the file: Altera-SoCFPGA>HelloWorld-Baremetal-ARMCC.tar.gz

Then un-tar it.

The directory **Altera-SoCFPGA>HelloWorld-Baremetal-ARMCC** can then be copied in the Eclipse WorkSpace and Imported as a new project. The files inside are:

- .cproject used by Eclipse
- .project used by Eclipse
- *.launch ??
- Makefile for the Compiler/Assembler/Linker
- scatter.scat An important info is the flag for the cpu: --cpu=Cortex-A9.no_neon.no_vfp
Info for the compiler for the Code, Data, Stack and Heap addresses
in this case in the internal SRAM

11.3.2.1 Scatter.scat

```

;*****
;
; Copyright (c) 2013 Altera All Rights Reserved.
;*****
;
; Scatter-file for OnChip RAM based example
; This scatter-file places application code, data, stack and heap at suitable addresses in the memory map.

; Altera SoC-FPGA has 64kB of internal OnChip RAM

OCRAM 0xFFFF0000 0x10000
{
    APP_CODE +0

    {
        * (+RO, +RW, +ZI)
    }
}

```

```
ARM_LIB_STACKHEAP 0xFFFF8000 EMPTY 0x8000 ; Application heap and stack
{ }
}
```

11.3.2.2 Makefile

Makefile for the ARM compiler

```
# Copyright (C) ARM Limited, 2011. All rights reserved.
#
# This example is intended to be built with the ARM Compiler armcc

TARGET=Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.axf

CC=armcc
AS=armasm
LD=armlink
AR=armar

# Select build rules based on Windows or Unix
ifdef WINDIR
DONE=@if exist $(1) echo Build completed.
RM=if exist $(1) del /q $(1)
SHELL=$(WINDIR)\system32\cmd.exe
else
ifdef windir
DONE=@if exist $(1) echo Build completed.
RM=if exist $(1) del /q $(1)
SHELL=$(windir)\system32\cmd.exe
else
DONE=@if [ -f $(1) ]; then echo Build completed.; fi
RM=rm -f $(1)
endif
endif

all: $(TARGET)
    $(call DONE,$(TARGET))

rebuild: clean all

clean:
    $(call RM,*.o)
    $(call RM,$(TARGET))

hello.o: hello.c
    $(CC) -c -g --cpu=Cortex-A9.no_neon.no_vfp -O0 hello.c

$(TARGET): hello.o scatter.scats
    $(LD) hello.o -o $(TARGET) --cpu=Cortex-A9.no_neon.no_vfp --scatter=scatter.scats
```

11.3.3 [3]GPIO access

The references for gpio are:

- http://www.altera.com/literature/hb/cyclone-v/cv_54022.pdf

- <http://www.altera.com/literature/hb/cyclone-v/hps.html>
- Supports up to 71 I/O pins and 14 input-only pins depend on device variant

On de1-soc:

- Only 1 Button for HPS GPIO 1
- Only 1 LED for HPS GPIO 1

Pin Name	HPS GPIO	Register [bit]	Function	Address	Dir
HPS_KEY	GPIO54	GPIO1[25]	I/O	0xFF20 9000	In
HPS_LED	GPIO53	GPIO1[24]	I/O	0xFF20 9000	Out

HPS peripherals are mapped to HPS base address space 0xFC00 0000 with 64KB size.

Registers of GPIO0 controller are mapped to the base address 0xFF20 8000 - 0xFF20 8FFF (4KB size)

Registers of GPIO1 controller are mapped to the base address 0xFF20 9000 - 0xFF20 9FFF (4KB size)

Registers of GPIO2 controller are mapped to the base address 0xFF20 A000 - 0xFF20 8FFF (4KB size)

		http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf		
GPIO0	0xFF20 8000 - 0xFF20 8FFF	0xFF70 8000		
GPIO1	0xFF20 9000 - 0xFF20 9FFF	0xFF70 9000		
GPIO2	0xFF20 A000 - 0xFF20 8FFF	0xFF70 A000		
LWFGASLAVES		0xFF20 0000		

gpio0	0xFF70 8000	HPS_GPIO0_ADDRESS	HPS_GPIO0_OFFSET		
gpio_swporta_dr	0	HPS_GPIO0_GPIO_SWPORTA_DR_ADDRESS	GPIO_GPIO_SWPORTA_DR_OFFSET		
gpio_swporta_dds	0x04	HPS_GPIO0_GPIO_SWPORTA_DDR_ADDRESS	GPIO_GPIO_SWPORTA_DDR_OFFSET		
gpio_inten	0x30	HPS_GPIO0_GPIO_INTEN_ADDRESS	GPIO_GPIO_INTEN_OFFSET		
gpio_intmask	0x34	HPS_GPIO0_GPIO_INTMASK_ADDRESS	GPIO_GPIO_INTMASK_OFFSET		
gpio_inttype_level	0x38	HPS_GPIO0_GPIO_INTTYPE_LEVEL_ADDRESS	GPIO_GPIO_INTTYPE_LEVEL_OFFSET		
gpio_int_polarity	0x3c	HPS_GPIO0_GPIO_INT_POLARITY_ADDRESS	GPIO_GPIO_INT_POLARITY_OFFSET		
gpio_intstatus	0x40	HPS_GPIO0_GPIO_INTSTATUS_ADDRESS	GPIO_GPIO_INTSTATUS_OFFSET		
gpio_raw_intstatus	0x44	HPS_GPIO0_GPIO_RAW_INTSTATUS_ADDRESS	GPIO_GPIO_RAW_INTSTATUS_OFFSET		
gpio_debounce	0x48	HPS_GPIO0_GPIO_DEBOUNCE_ADDRESS	GPIO_GPIO_DEBOUNCE_OFFSET		
gpio_porta_eoi	0x4c	HPS_GPIO0_GPIO_PORTA_EOI_ADDRESS	GPIO_GPIO_PORTA_EOI_OFFSET		
gpio_ext_porta	0x50	HPS_GPIO0_GPIO_EXT_PORTA_ADDRESS	GPIO_GPIO_EXT_PORTA_OFFSET		
gpio_ls_sync	0x60	HPS_GPIO0_GPIO_LS_SYNC_ADDRESS	GPIO_GPIO_LS_SYNC_OFFSET		
gpio_id_code	0x64	HPS_GPIO0_GPIO_ID_CODE_ADDRESS	GPIO_GPIO_ID_CODE_OFFSET		
gpio_ver_id_code	0x6c	HPS_GPIO0_GPIO_VER_ID_CODE_ADDRESS	GPIO_GPIO_VER_ID_CODE_OFFSET		
gpio_config_reg2	0x70	HPS_GPIO0_GPIO_CONFIG_REG2_ADDRESS	GPIO_GPIO_CONFIG_REG2_OFFSET		
gpio_config_reg1	0x74	HPS_GPIO0_GPIO_CONFIG_REG1_ADDRESS	GPIO_GPIO_CONFIG_REG1_OFFSET		

--	--	--	--	--	--

11.3.3.1 Library installation

C:\altera\13.1\embedded\ip\altera\hps\altera_hps\hwlib

HERE

11.3.3.2 Reference files

hps.h		