Fault Simulation

Simulating Fault with Several Applications

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Abstract*—This electronic document is a report of fault simulation homework of test and testability course. *In this paper we try to report the result of fault simulation with Verilog and Atalanta and Hope applications.

Atalanta, Fault Collapsing, Fault Coverage, Fault injection, Fault Simulation, Hope

I. Introduction

This paper tries to test a processor c6288. In this paper we showed the result of testing c6288 with serial inputs. At first we use Atalanta Application to make circuit pattern then apply tests to this pattern and compare the fault coverage. Main topics of this paper are: (1) Use Atalanta as simulation application to achieve circuit pattern and fault coverage, (2) Use hope application to achieve fault coverage, and (3) Use Verilog to apply serial inputs to the circuit of c6288 and simulate the faulty and golden circuit with fault collapsing and fault injection PLIs.

II. Atalanta Simulation

A. *Apply our bench file for making circuit pattern*

First, we apply our c6288.bench file to Atalanta application with the command below:

Atalanta-M –t c6288.pat –W 1 c6288.bench

The output is our c6288.pat that is our circuit pattern.

B. *Apply the rest of commands in Atalanta*

We apply rest of commands base on Atalanta commands pdf file and receive c6288.msk c6288.flt c6288.rep c6288.ut files. Our c6288.pat file that created here will be use in the following processes.

We can see in our c6288.rep file the results of simulation and as we see we have 6508 faults total that 6479 of them are detected and 29 of them are still undetected (as we see in Fig.1) and if we calculate the coverage we can see the coverage amount is :

6479 / 6508 * 100% = 0.99554394591272280270436 3

```
gates: 2922
iv: 32
ov: 32
i_patterns: 87
patterns: 54
faults: 6508
d_faults: 6479
r_faults: 29
time: 0.093
```

Fig.1 Atalanta Simulation Results

III. Hope Simulation

Before using Hope application we have to use Atalanta application to create our circuit pattern then change every columns of our pattern by adding column number + : at the beginning of every column then change the file extension to .test.

After that we apply our pattern and bench file to Hope application with command below:

Hope –t c6288.test c6288.bench

The result is in Fig.2. As we see we have 99.554% coverage and 32 inputs and 32 outputs 6508 collapsed fault. As we see 6479 faults detected and only 29 faults remain undetected.

```
C:\Users\Mamad\HW#3\hope>hope -t c432.test c6288.bench
        ××××××××××××××××××××××××××××××××××××××××××××××××××××××××××××
        ×                                                            ×
        ×            Welcome to HOPE (version 2.0)                   ×
        ×                                                            ×
        ×               Dong S. Ha (ha@vt.edu)                       ×
        ×             Web: http://www.ee.vt.edu/ha                   ×
        ×  Virginia Polytechnic Institute & State University         ×
        ×                                                            ×
        ××××××××××××××××××××××××××××××××××××××××××××××××××××××××××××

××××××   SUMMARY OF SIMULATION RESULTS   ××××××
1. Circuit structure
   Name of circuit                          : c6288.bench
   Number of primary inputs                 : 32
   Number of primary outputs                : 32
   Number of flip-flops                     : 0
   Number of gates                          : 2922
   Level of the circuit                     : 109

2. Simulator input parameters
   Simulation mode                          : file (c432.test)

3. Simulation results
   Number of test patterns applied          : 55
   Fault coverage                           : 99.554 %
   Number of collapsed faults               : 6508
   Number of detected faults                : 6479
   Number of undetected faults              : 29

4. Memory used                              : 8810 Kbytes

5. CPU time
   Initialization                           : 2548998.167 secs
   Fault simulation                         : 0.000 secs
   Total                                    : 2548998.167 secs
```

Fig.2 Hope application fault simulation results

IV. Verilog Simulation

After simulating our circuit bench with Atalanta and Hope applications we go throw Verilog simulation. In this phase we need two PLIs. First faultcollapsing.dll that include $FaultCollapsing command which can collapse our faults because many of our faults can be masked by our faults or may not propagate to outputs. Second PLI is faultinjection.dll that include $InjectFault command which apply a fault to our circuit and $RemoveFault command which remove our injected fault. We need to make a fault directory that include single stack at faults of all circuit wires and gates inputs and outputs and also a dictionary of fault syndromes.

We need to write a test bench that automatically apply or vector with serial method. As we know we have ($2^{32} = 4294967296$) vectors! It takes huge time to apply it as serial. Our PC spends about 8 hours to apply this vector and then makes a fault dictionary of 6479 faults with fault coverage 99.5544% (Fig.3). We can see the difference between golden model circuit and faulty model circuit outputs as waveform in Fig.4.

```
6505
6506
6507
6508
6509   Coverage: 0.995544
6510
```

Fig.3 fault dictionary and coverage

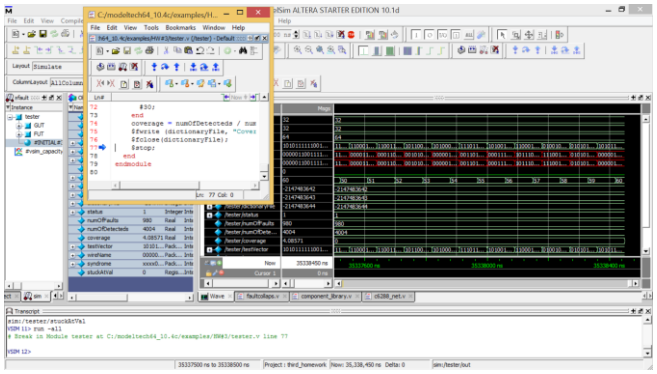

Fig.4 output waveform

REFERENCES

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