NetlistGen Manual

– Prerequisite

- Xilinx ISE web pack installation
  - Download windows based Xilinx ISE web pack edition from: http://xilinx.com
  - Click on "*setup.exe*" and follow the setup process.
  - Choose web pack edition for installation.
  - Leave the default options of checked boxes unchanged.
  - Click on the install button to start installation.

– Verilog code style

- Port declaration format for behavioral top module should list input and output declarations after the module header. *NetlistGen* **cannot translate input or output in the port identifier list**. Same applies to port reg declaration.
- Each input or output should be declared separately. For example you cannot define clock and reset signals at the same line.
- As the software uses Xilinx for netlist generation, you cannot use parameters in your code. You should use the actual value of each parameter.

Wrong format	Right format
module x(input [2:0] a,output [2:0] y);	module x(a,y); input [2:0] a; output [2:0] y;
input clk, reg;	input clk; input reg;
input [CNT_WIDTH-1:0] counter;	input [15:0] counter;

– Procedure (should be exactly followed)

- Put all Verilog codes of the design and NetlistGen_main.exe in same folder.
- Run *NetlistGen_main.exe*
- When prompted, choose a name for your project. This name will become the project name of the synthesis process of ISE.
- When prompted for the name of module, enter the name of the top module of your project. **The name of the Verilog file of the top module should be the same as the name of the module**. After that, *NetlistGen* reads the behavioral Verilog file. If you want to add any other Verilog files to your design, you can add them in the next step (Any other Verilog

files which are used in your top module should be added). Added files should be available in the root directory.

- Now you should synthesize your design with Xilinx ISE. For that, choose "y" to synthesize your design. The NetlistGen uses the intermediate EDIF format that is converted from Xilinx Synthesis Technology (*xst.exe*) NGC output, for generating netlist.
- NetlistGen runs *xst.exe* in TCL shell environment. The synthesis process will be done automatically if the location of the *xtclsh.exe* file is specified correctly. If you installed the ISE in a different location, or you use other versions of ISE, **you should enter the correct path of the installation**. For example if you use Xilinx_ISE_DS_Win_12.2 version, you should enter C:\Xilinx\12.2\ISE_DS\ISE\bin\nt, which is the path of *xtclsh.exe* file for the 32-bit Windows NT OS, in the installation path request prompt.
- After selecting the location of the *xtclsh.exe* file, the synthesis process will start. The process will be completed successfully if there are no compilation and synthesis errors.
- NetlisGen will generate the netlist in the ***netlist_MODULENAME_V1.v*** file. It also generates ***MODULENAME*.bench** file.