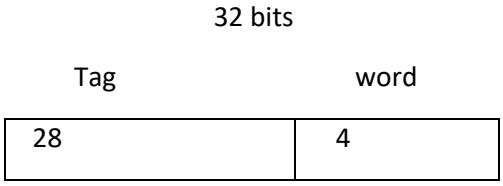
1) 1. **A cache memory capacity is indicated as 512 KB. Memory word size is 4 bytes and address bus width is 32 bits. A memory block contains 4 memory words. Size of the main memory is 1 GB.**

Cache memory 512 KB
Memory word=4 bytes
Address bus width=32 bits
1 block =4 words=16 bytes
Size of the main memory is 1 GB.

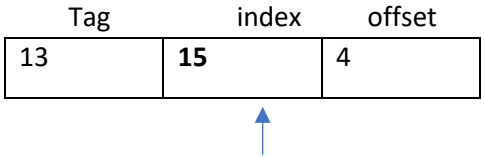
I. How many lines the cache have?
512*2^10/16 bytes
2^19/2^4
2^15

II. Indicate the format of memory address if it is an associative mapping cache

2^4=16
4 bits for words,



III. Indicate the format of memory address if it is a direct mapping cache



No of Cache lines=2^**15**

IV. If the cache is 8-way set associative, How many sets does the cache have?
8 way set associative,

2^15/2^3
No of sets = 2^12

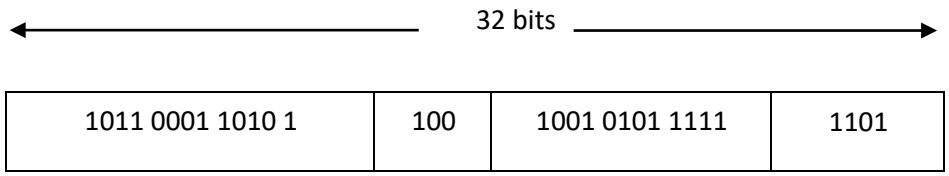
V. Indicate the format of memory address if it is a 8-way set associative mapping cache

Tag Index offset

VI. Calculate the set number of the memory address 0x B1AC95F9 in binary form

0x B1AC9F9 in binary form 1011 0001 1010 1100 1001 0101 1111 1001

VII.



Set number = 100

2. **Write down the instructions to complete the equation X =(A*B-C) + (A/C) in following Instruction Set Architectures**

I. Stack based

PUSH A

PUSH B

MUL

PUSH C

SUB

PUSH A

PUSH C

DIV

ADD

POP X

II. Accumulator based

LOAD A

MUL B

SUB C

STORE Y

LOAD A

DIV C

ADD Y

STORE X

III. Memory-memory based

3 operand

MUL Y,A,B

SUB Y,Y,C

DIV P,A,C

ADD X,Y,P

2 operand

MOV Y,A

MUL Y,B

SUB Y,C

MOV P,A

DIV P,C

ADD Y,P

IV. Register-Register based

LOAD R1,A

LOAD R2,B

LOAD R3,C

MUL R4, R1, R2

SUB R5, R4, R3

DIV R6, R1, R3

ADD R7,R5,R6

STORE X,R7

.

3) **Write down the sequence of events (cycles) in Booth's algorithm for the multiplication (-6)*9. (Use 5 bits registers to store data and express each step according to cycles. Define the terms you use.)**

6=00110

1's complement =11001

2's complement =11010=-6=M

N=5;

n	A	Q	Q_1	M	Steps	
5	00000	01001	0	11010	Initial values	
4	00110	01001	0	11010	A ← A-M	First Cycle
	00011	00100	1	11010	Right Shift	
3	11101	00100	1	11010	A ← A+M	Second Cycle
	11110	10010	0	11010	Right Shift	
2	11111	01001	0	11010	Right Shift	Third Cycle
1	00101	01001	0	11010	A ← A-M	Fourth Cycle
	00010	10100	1	11010	Right Shift	
0	11100	10100	1	11010	A ← A+M	Fifth Cycle
	11110	01010	0	11010	Right Shift	

(-6)*9 = 2's complement of 1111001010 = 0000110101+1 = (-)0000110110 $_2$= -54$_{10}$

4) . **Write down the Fetch-Execute cycle in RTL.**

PC ← 0 MAR
←PC
PC ← PC + 1
MDR ←M[MAR]
IR ← MDR
MAR ← MDR(L)
ACC ← M[MAR]

MAR ← PC
PC ← PC + 1
MDR ← M[MAR]
IR ← MDR
MAR ← MDR(L)
MDR ← M[MAR]

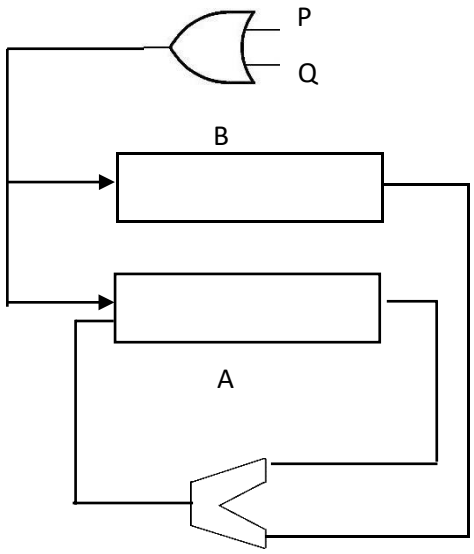
$ACC \leftarrow ACC + MDR$

$MAR \leftarrow PC$
$PC \leftarrow PC + 1$
$MDR \leftarrow M[MAR]$
$IR \leftarrow MDR$
$MDR \leftarrow ACC\ MAR$
$\leftarrow IR(L)\ M[MAR]$
$\leftarrow MDR$

5). Describe the following RTL micro-operations with aid of logic diagrams.

I. $P + Q : A \leftarrow A + B$

If P both Q are true or even one of them is true the content in register A is added with the content in B register and the result will be stored in register A.



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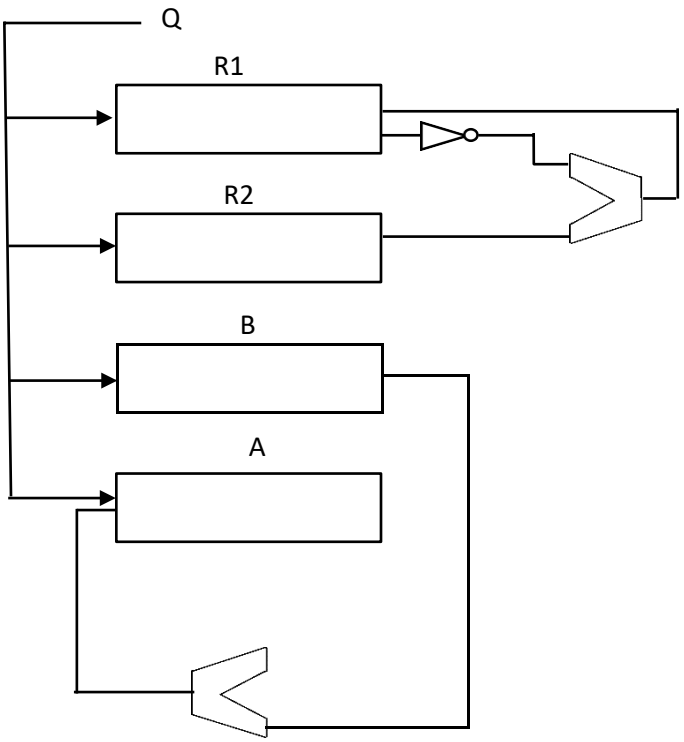
II. $Q : A \leftarrow A + B, R1 \leftarrow R1' + R2$



If Q is genuine then the substance in A register will be added with the substance in the B register and afterward the outcome will be put away back in A register. At that point at the same time the supplement of the substance in register R1 will be added with the substance in the register R2 and the outcome will be put away back in R1 register.