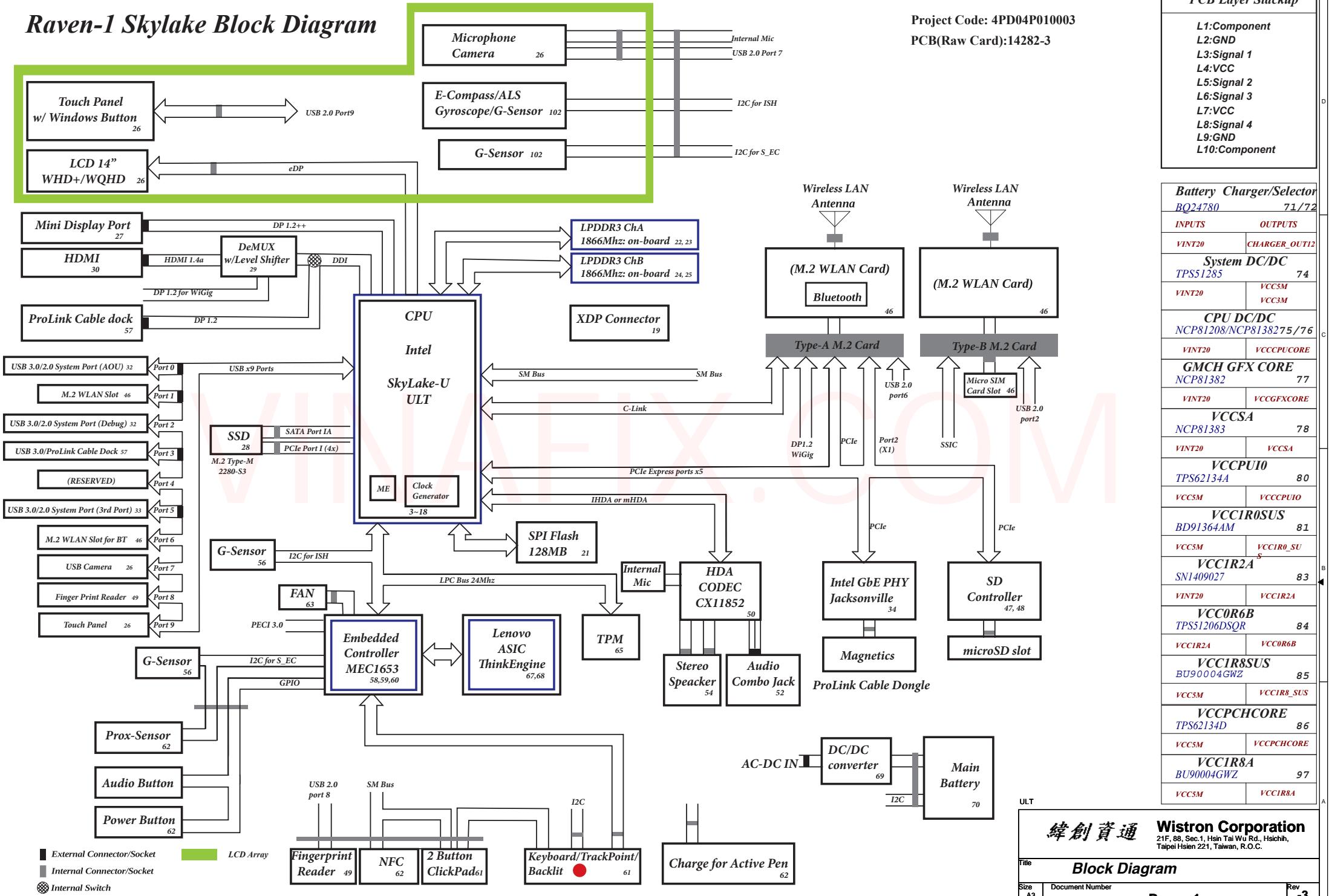


Raven-1 Skylake Block Diagram



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating	Size
			0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance

For the value, it can be read by the number before R. (R means resistor)

For the tolerance, it can be read from the last letter.

For the rating, we don't show on the symbol name.

For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is

Capacitor type + value + rating + size + tolerance + material

SCD1U10V2MX-1

SC=> SMT Ceremic, TC=> POS cap or SP cap

D1U => 0.1uF

10V => the voltage rating is 10V

2=> 0402, 3=>0603, 5=>0805

M=>tolerance M, K, Z

X=> X7R/X5R, Y=> Y5V

-1 => symbol version, nonsense to EE characteristic

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Title **Description**

Size A4 Document Number

Raven-1

Rev -3

Date: Monday, July 20, 2015

Sheet 2 of 102

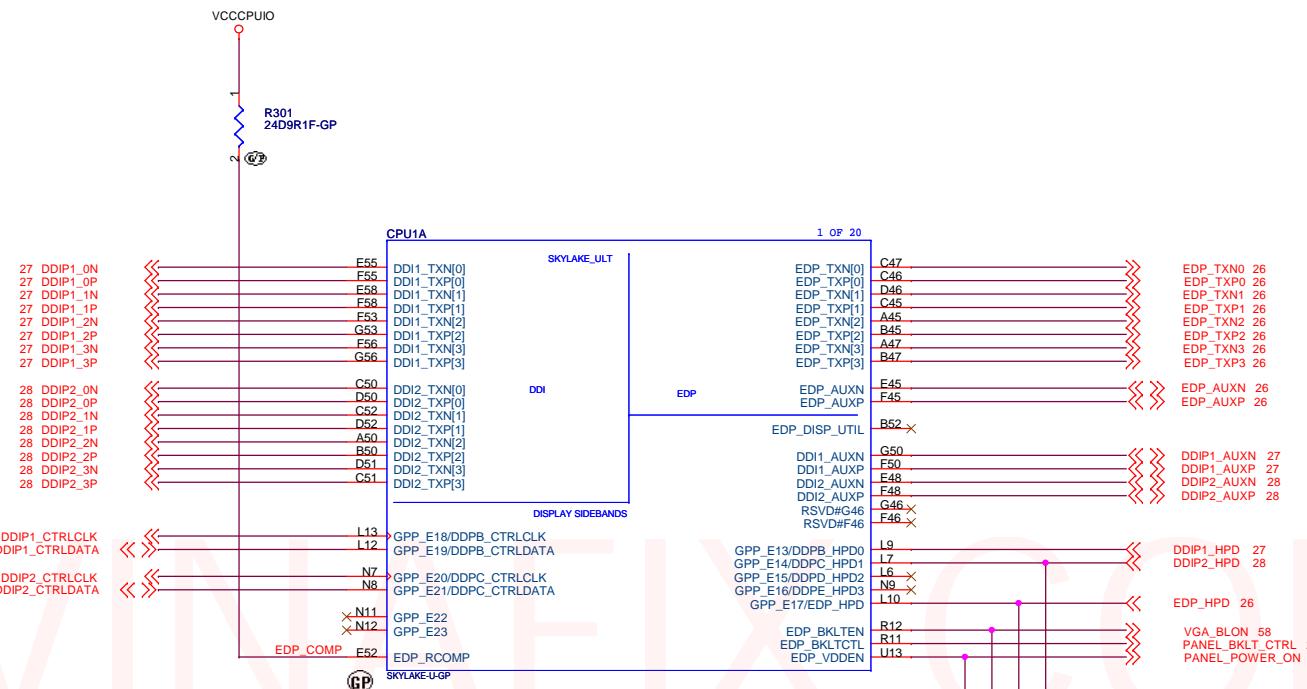


TABLE: Functional Strap

DDPB_CTRLDATA

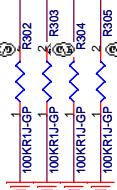
HIGH Port B is detected.

LOW Port B is not detected.

DDPC_CTRLDATA

HIGH Port C is detected.

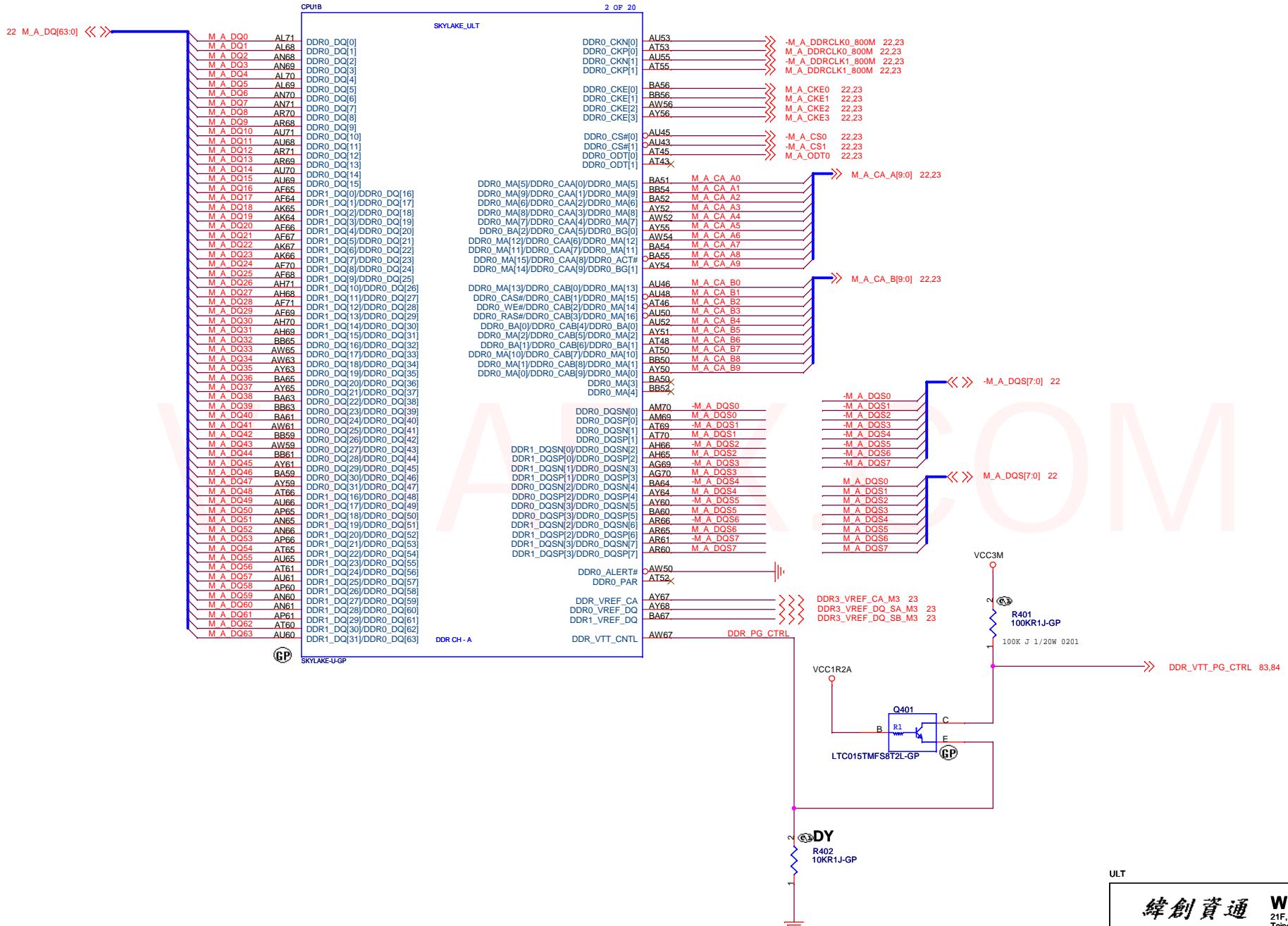
LOW Port C is not detected.



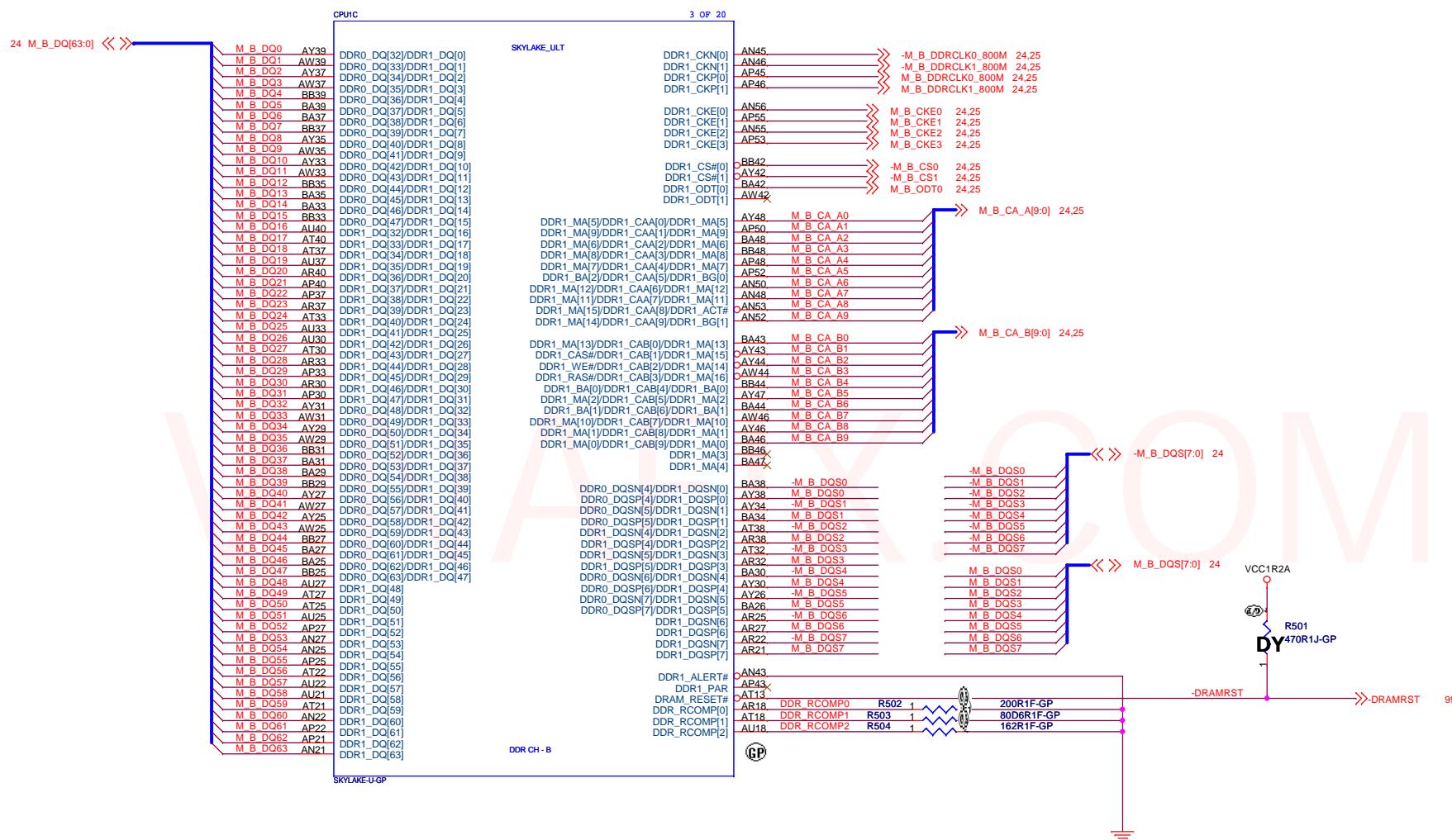
ULT

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Title	CPU(1/16) : DDI/EDP	Rev -3
Size	Document Number	Date: Monday, July 20, 2015

Raven-1



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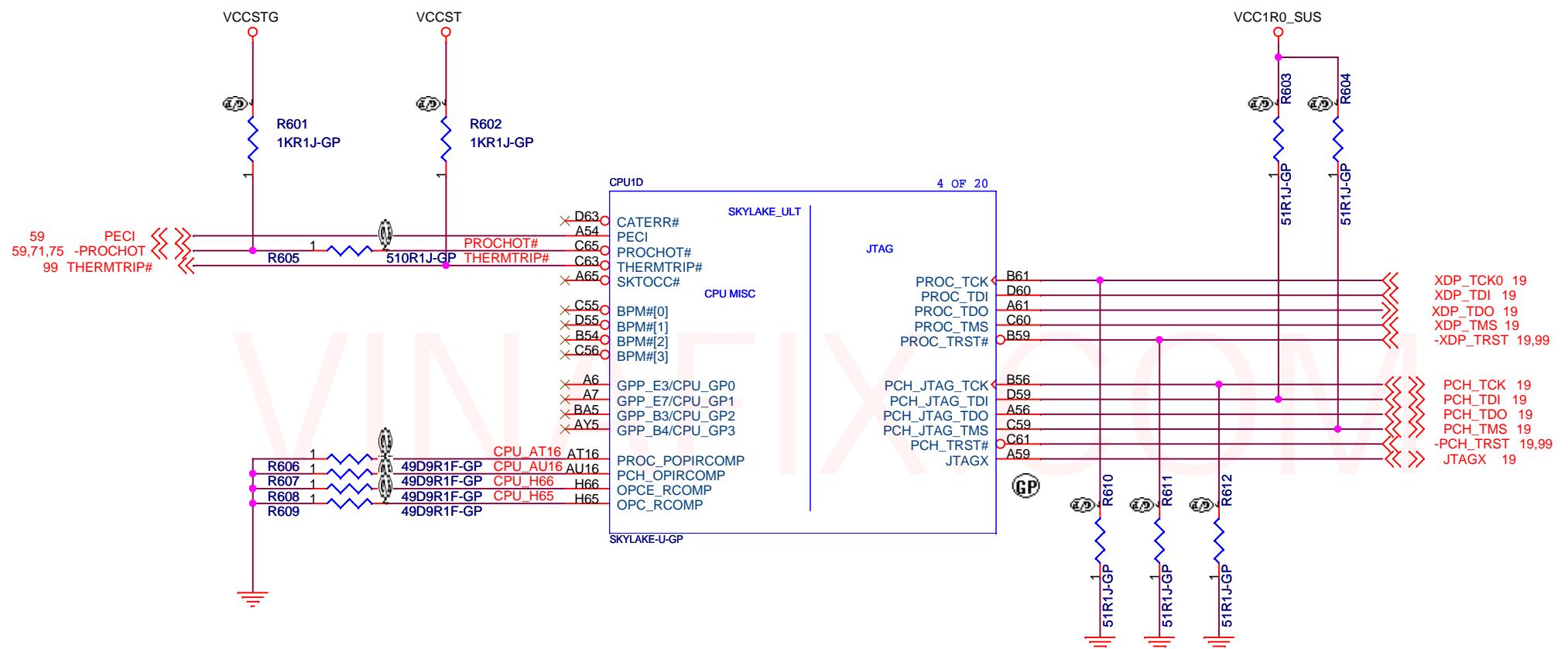


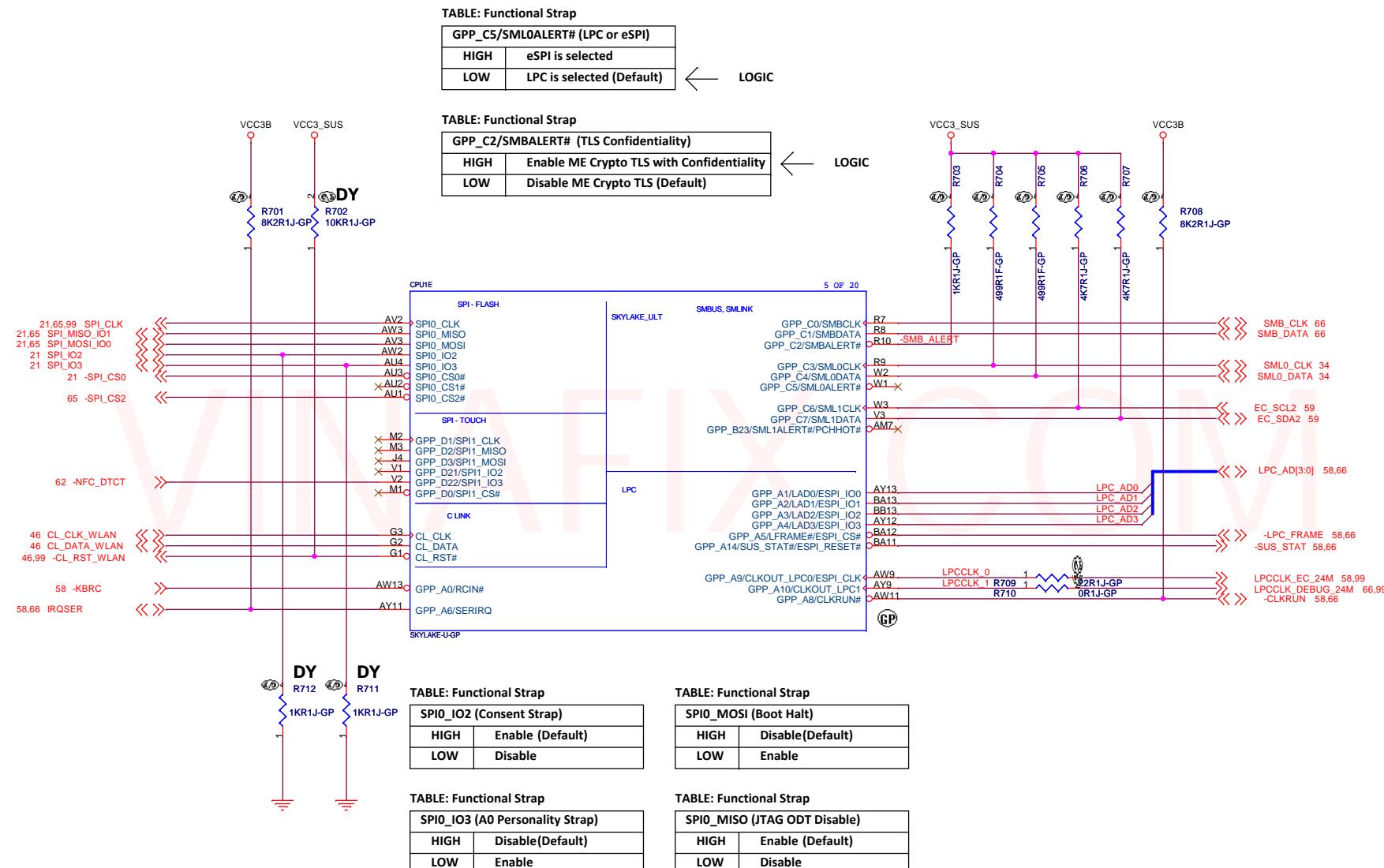
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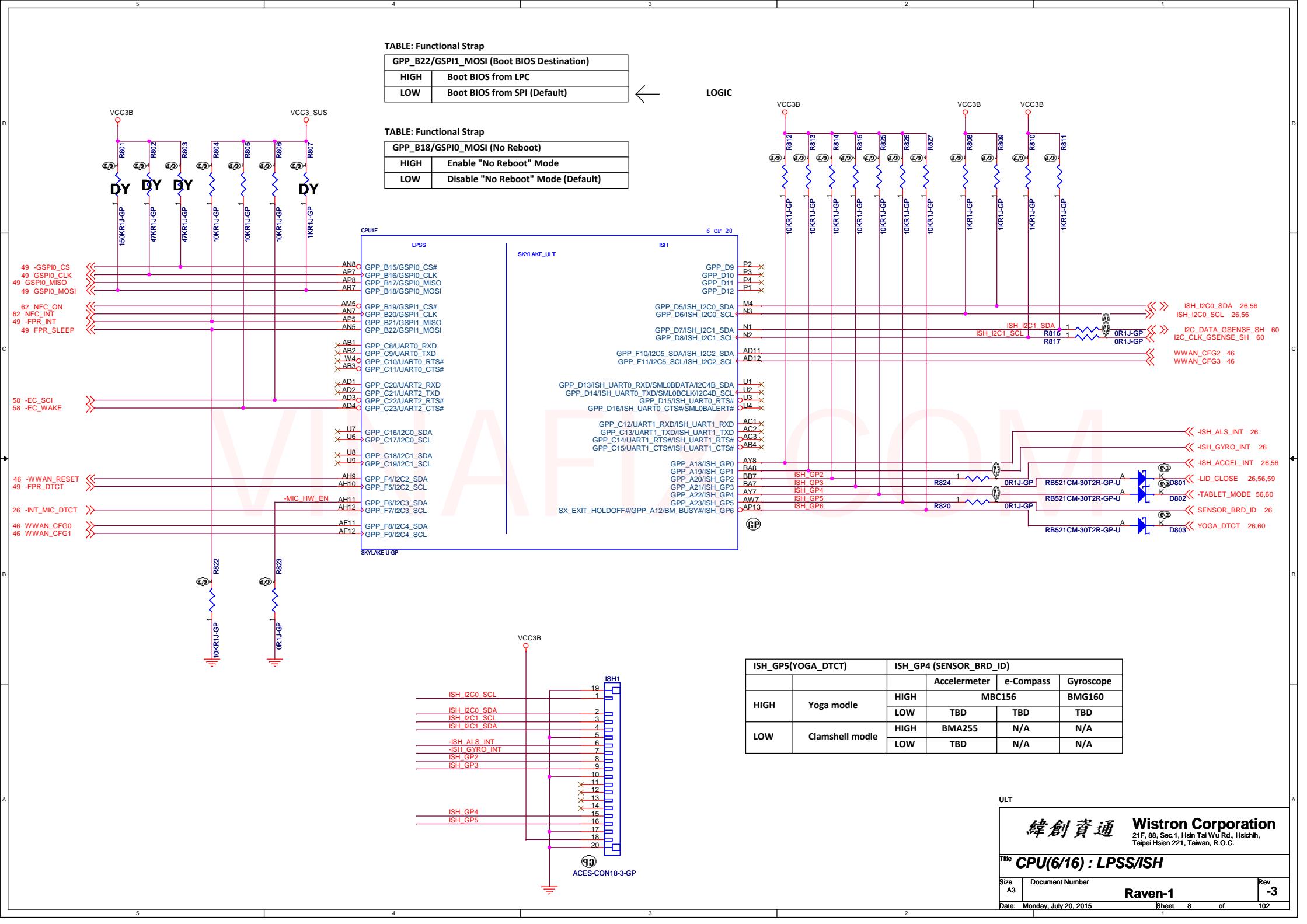
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

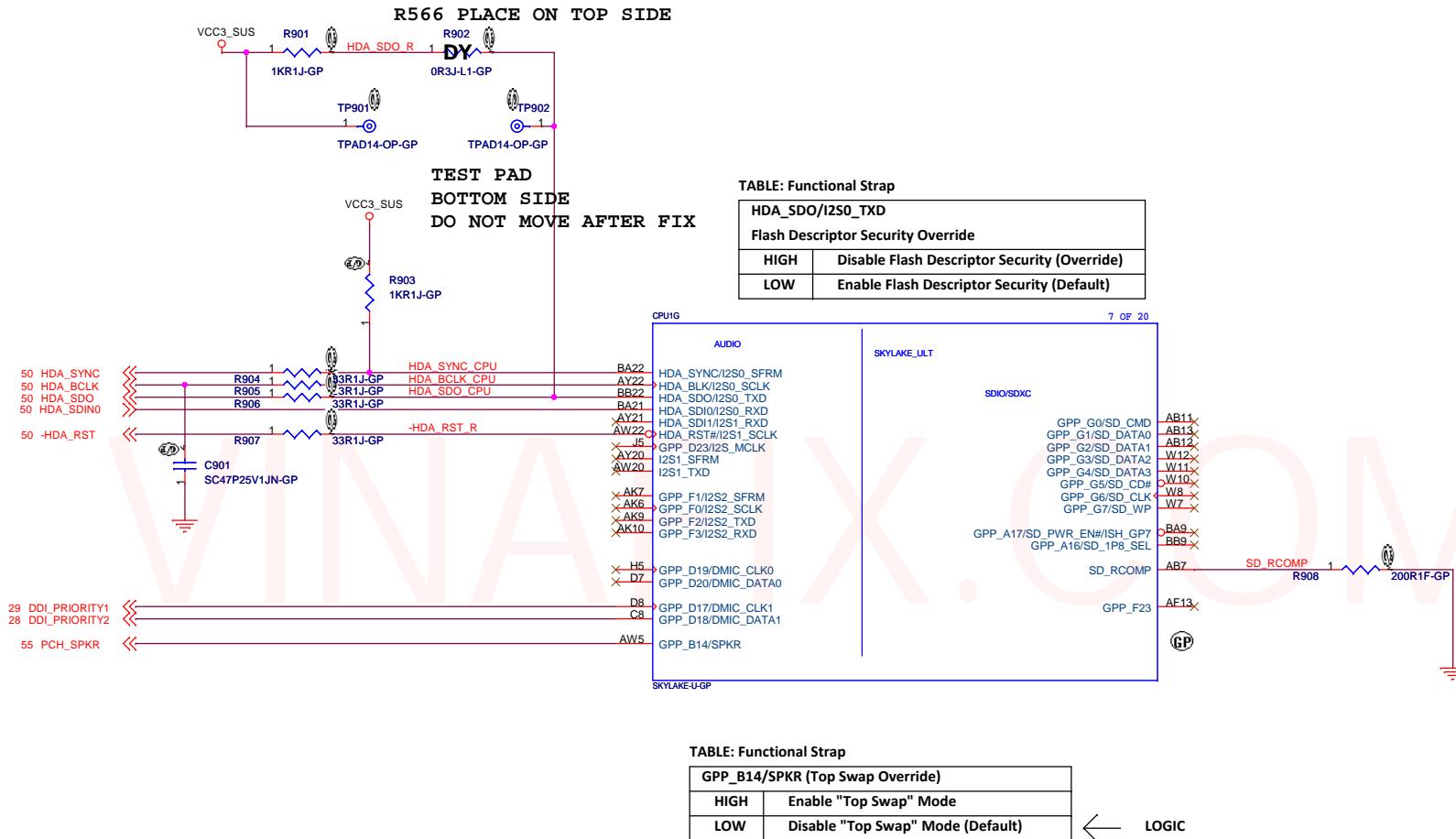
Title **CPU(3/16) · DDR CH-B**

Size A3	Document Number Raven-1	Rev -3
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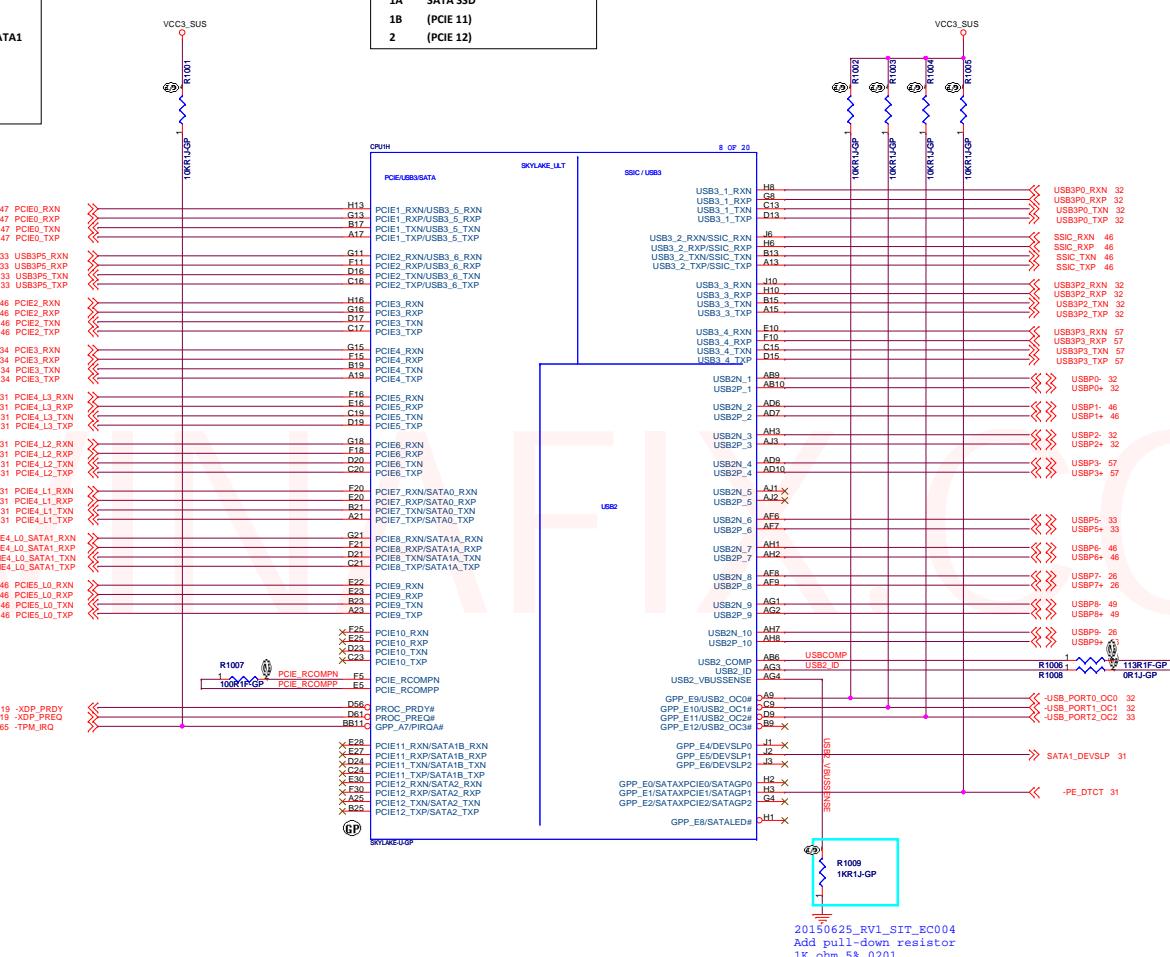




Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	SSIC	SSIC
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	USB3 6	USB3P5
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4 (GbE)	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCI9 (GbE)	PCI9 (x4)	PCI9_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	NA
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	NA
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	NA

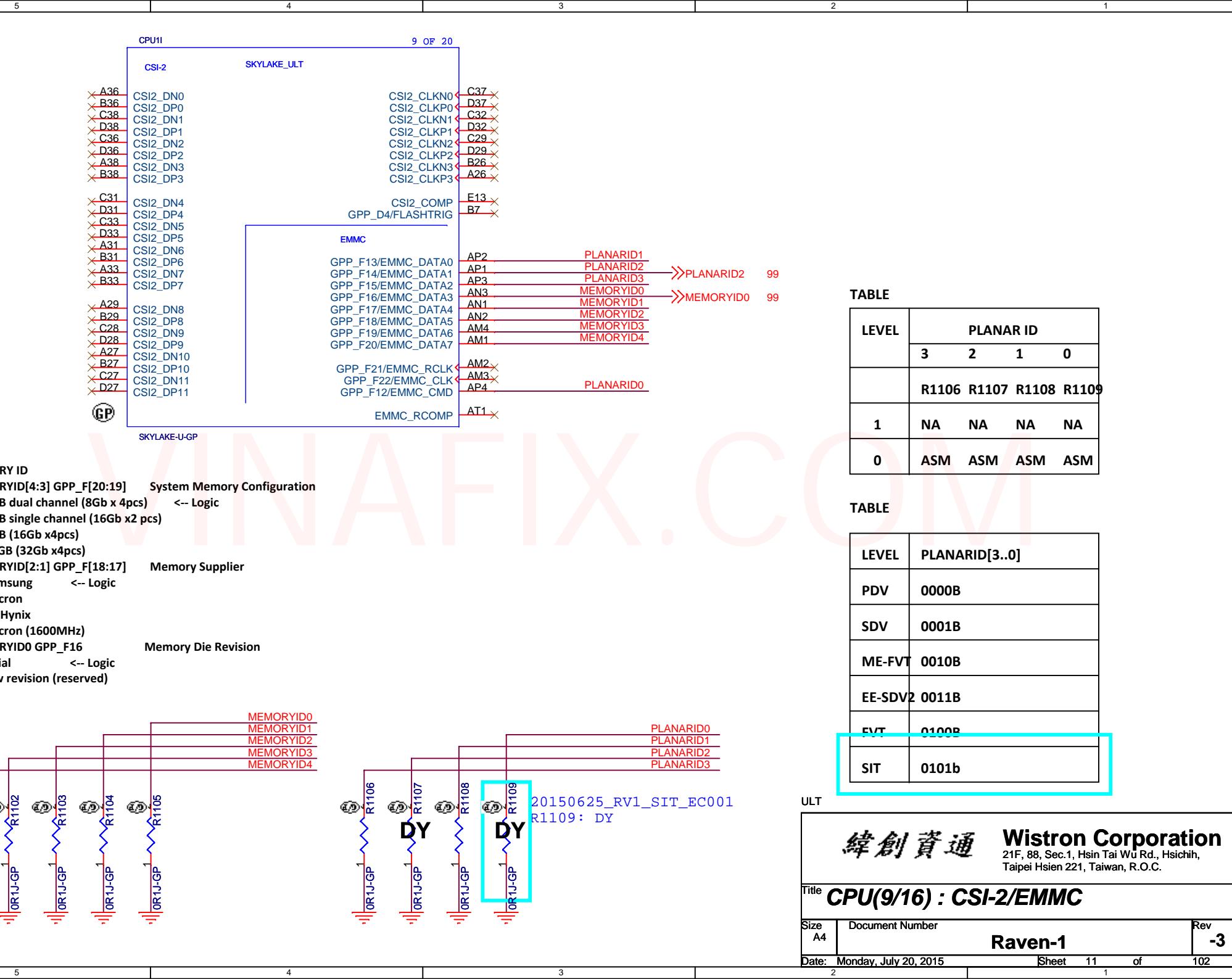
PCIe Port Assignment			
0	Media Card Controller	1	(USB3 6)
2	M.2 WLAN Slot Port 0 for WLAN	3	GbE PHY
4 (x4)	PCIe SSD		
5_L0	M.2 WLAN Slot Port 1 for WiGig		

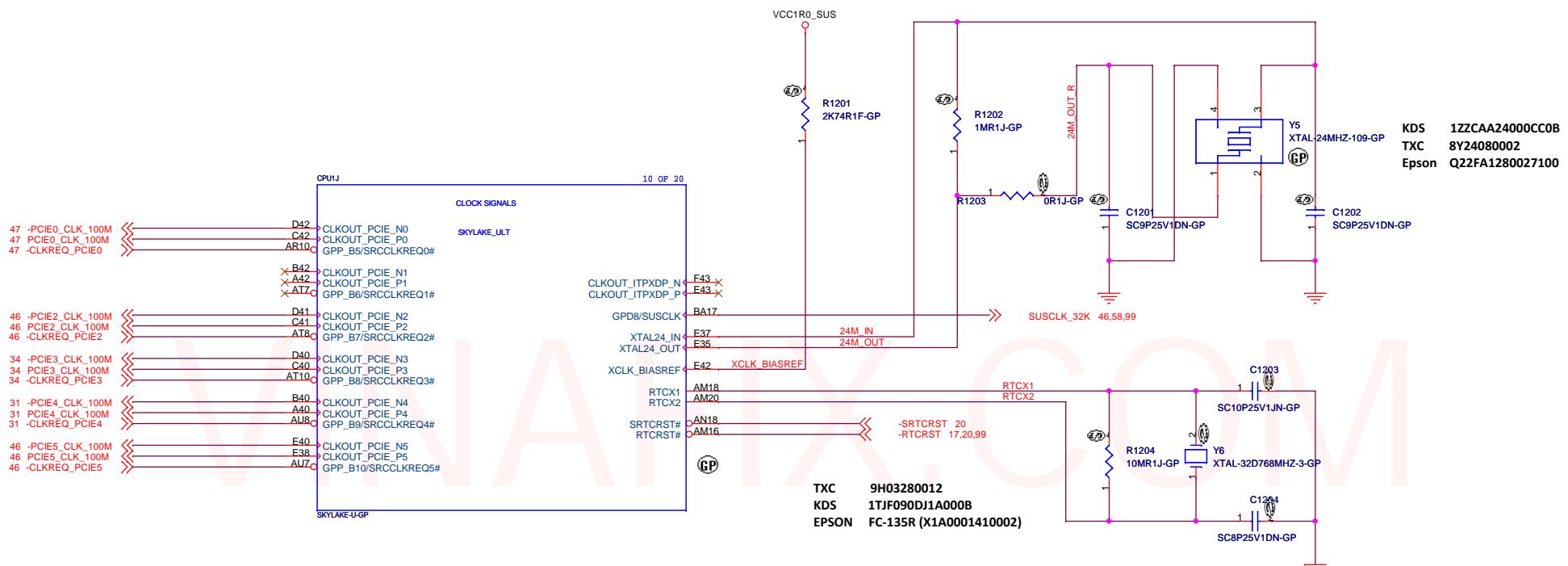
SATA Port Assignment			
0	(PCIE 7)	1A	SATA SSD
1B	(PCIE 11)		
2	(PCIE 12)		

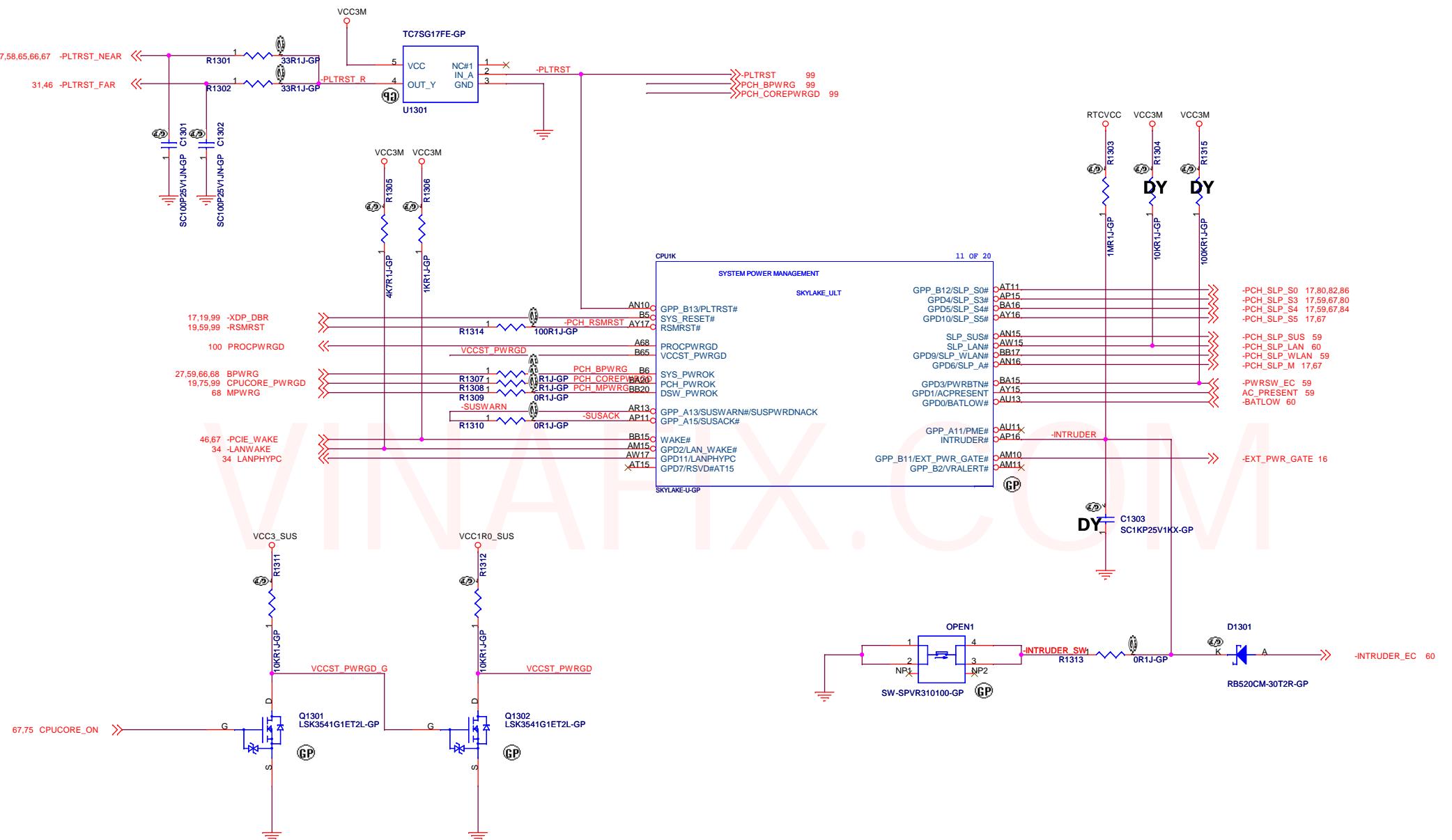


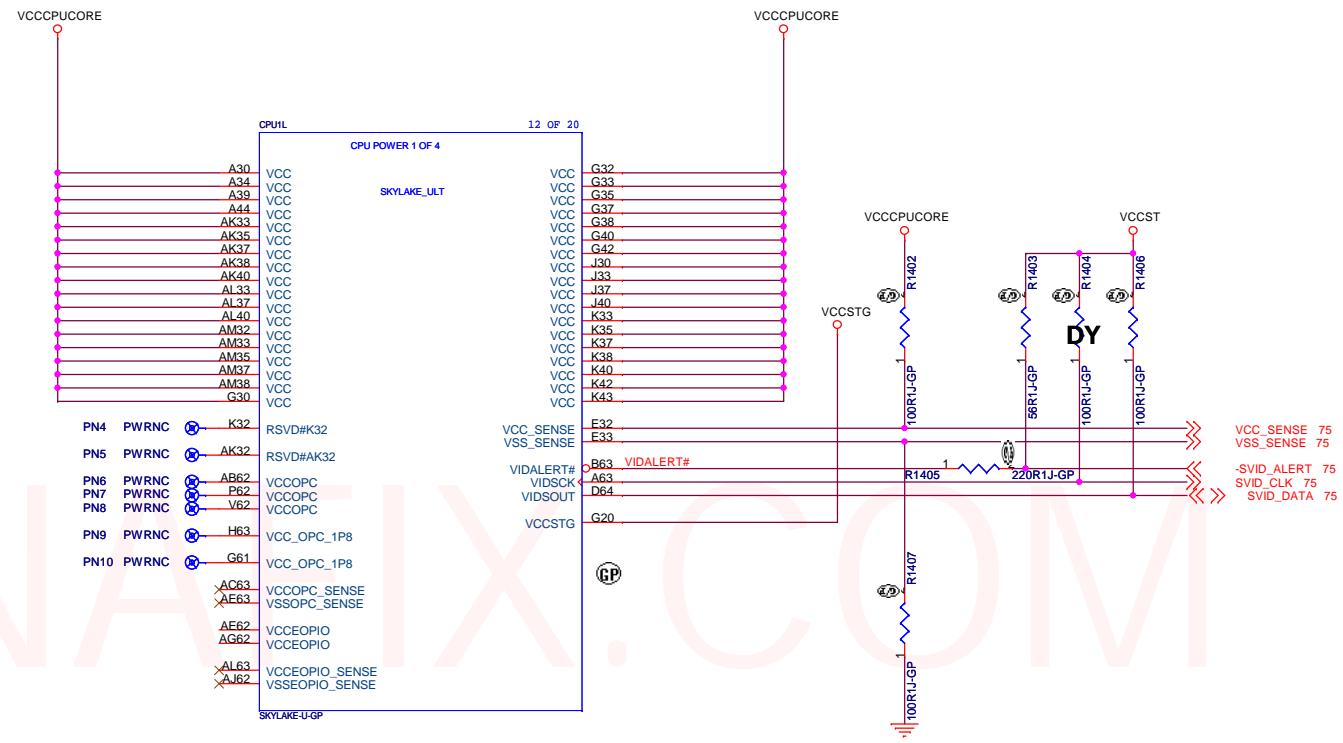
USB Port Assignment			
0	USB 3.0 System Port (AOU)	1	M.2 WWAN Slot
2	USB 3.0 System Port	3	Prolink Dock
4	(RESERVED)	5	USB 3.0 System Port (3rd Port)
6	M.2 WLAN Slot for BT	7	USB Camera
8	Fingerprint Reader	9	Touch Panel

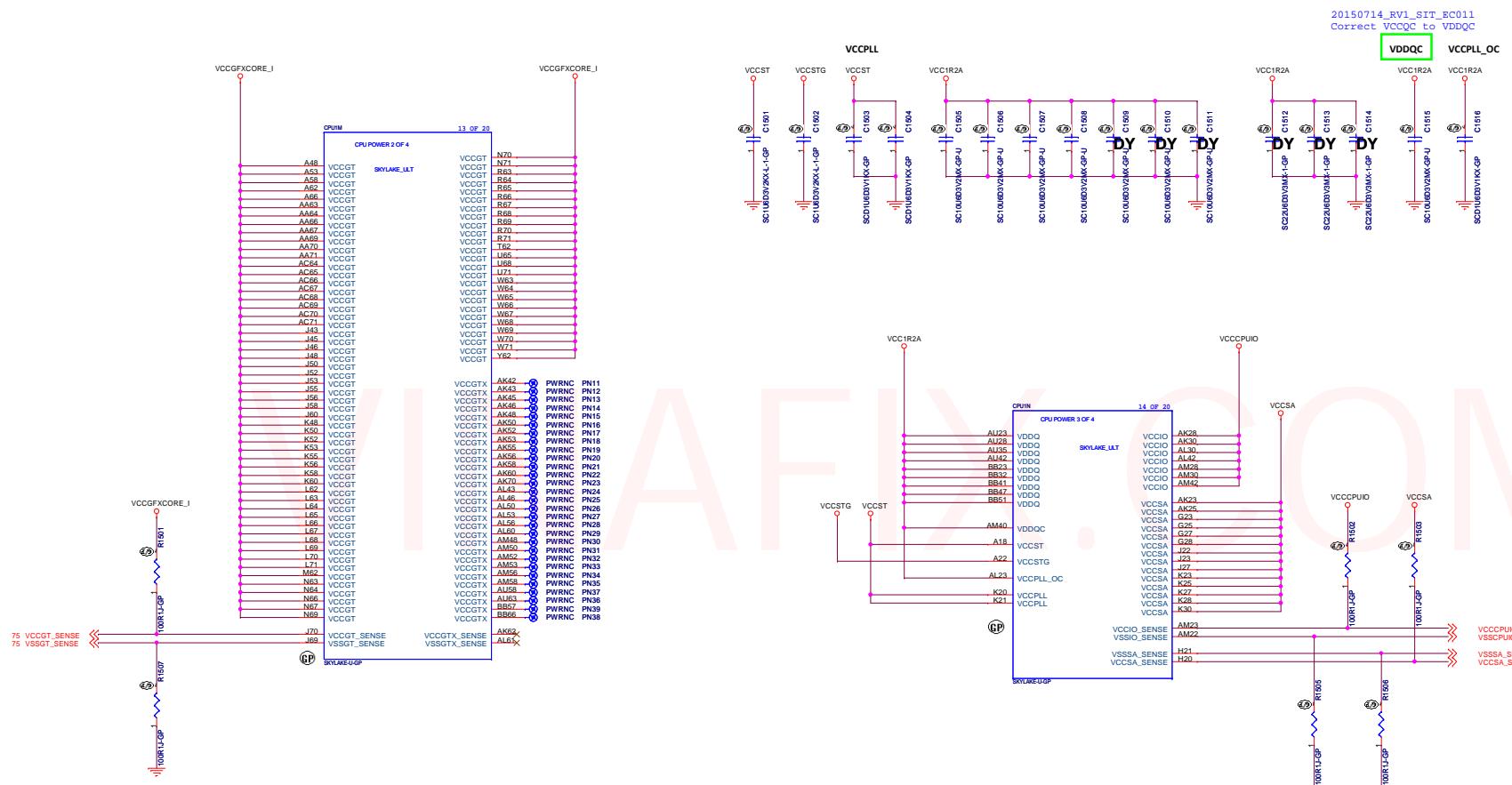
USB 3.0 Port Assignment			
0	USB 3.0 System Port (AOU)	1	M.2 WWAN Slot (SSIC)
2	USB 3.0 System Port	3	Prolink Dock
4	(PCIE 1)	5	USB 3.0 System Port (3rd Port)

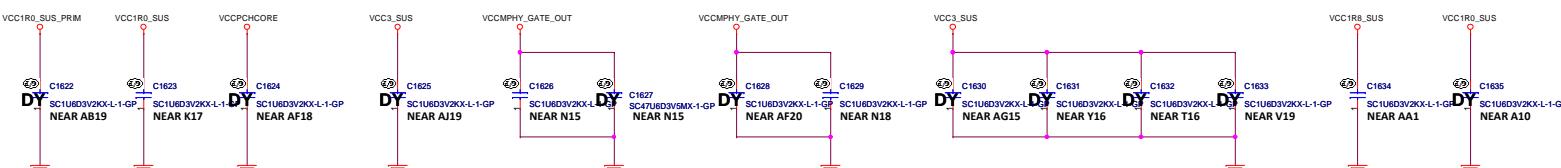
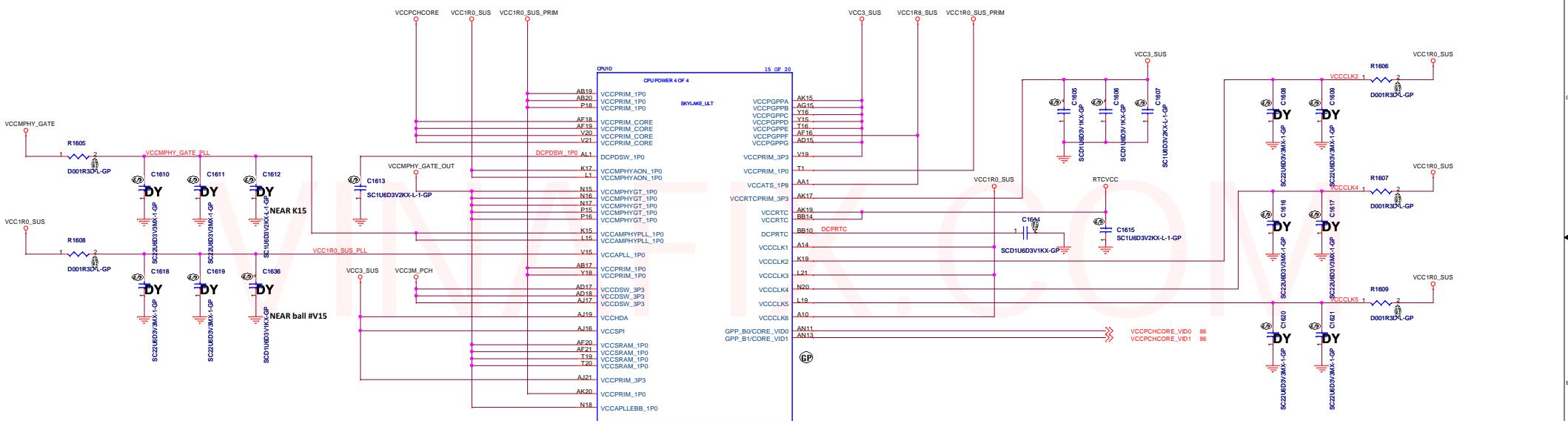
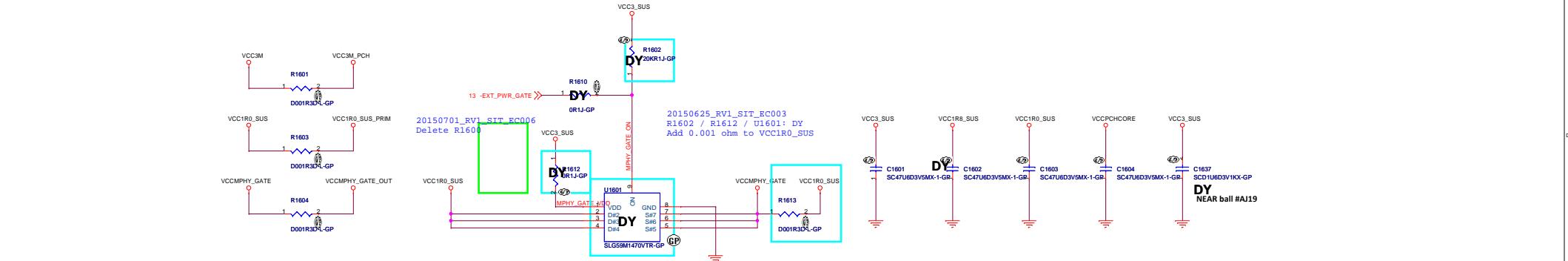


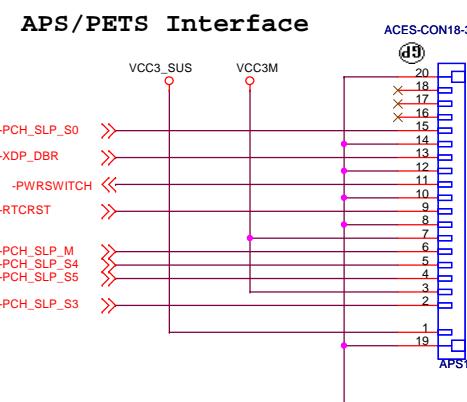
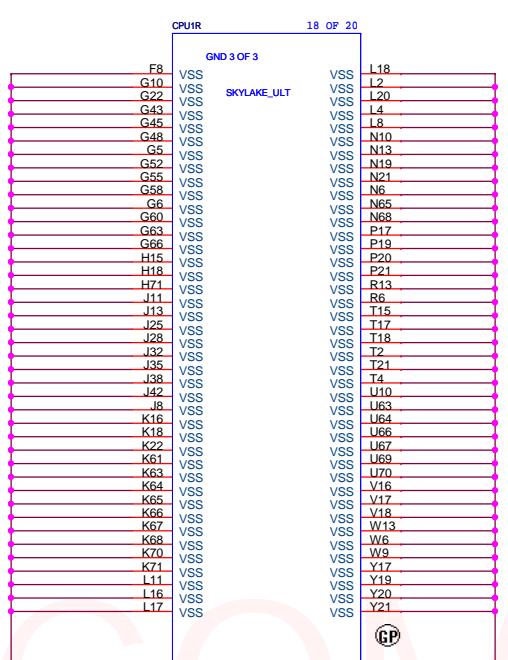
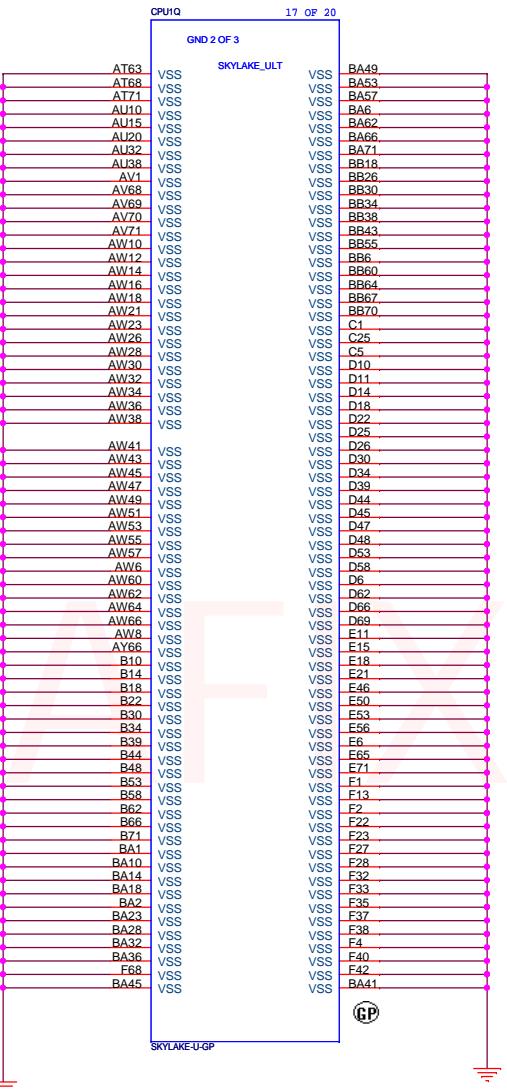
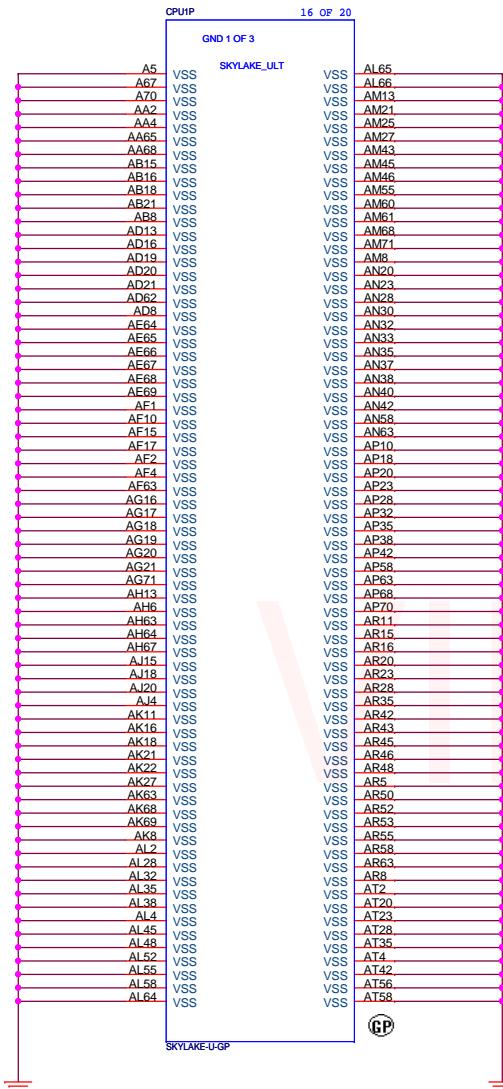












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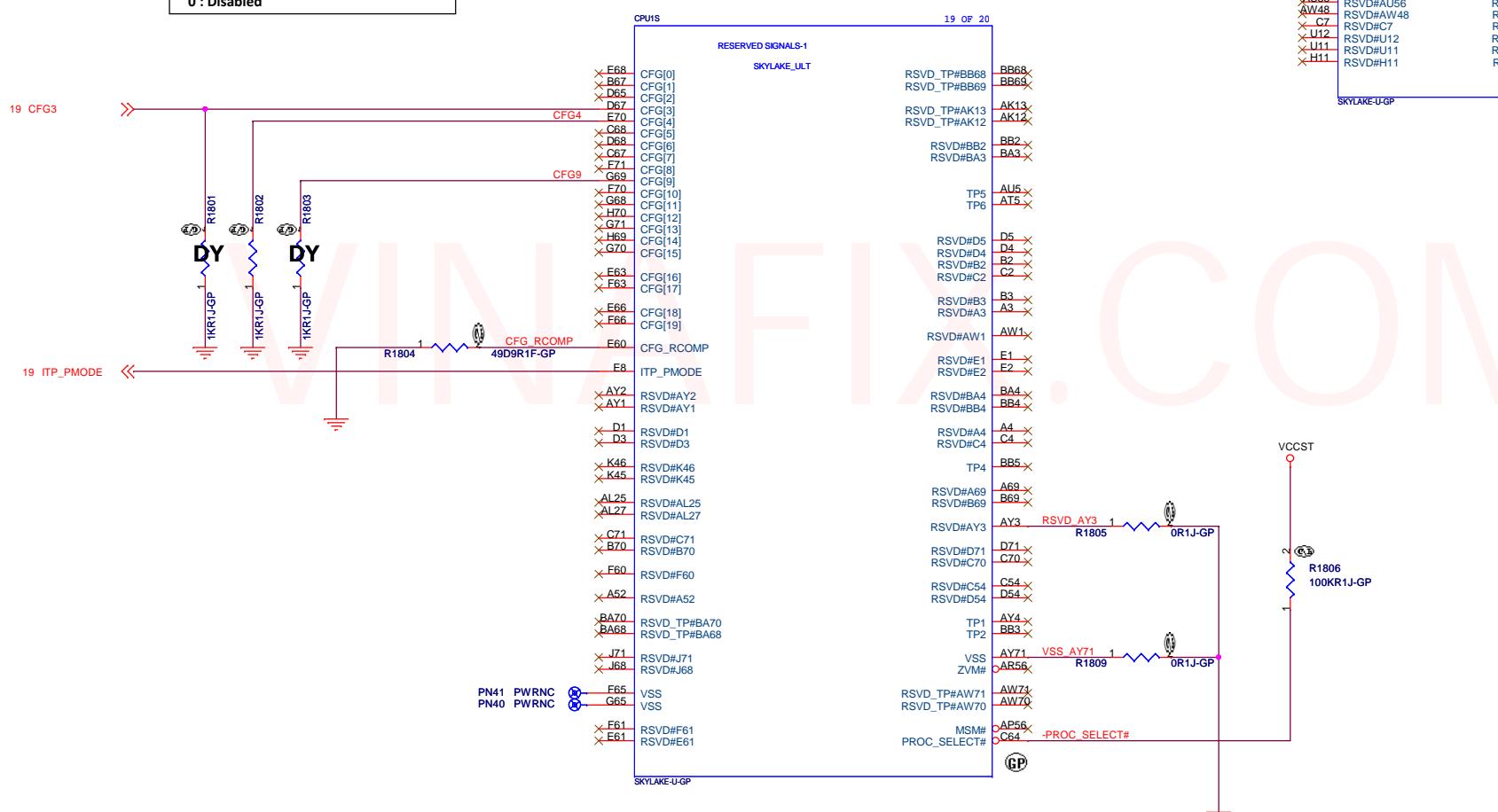
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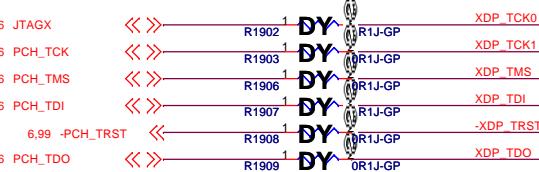
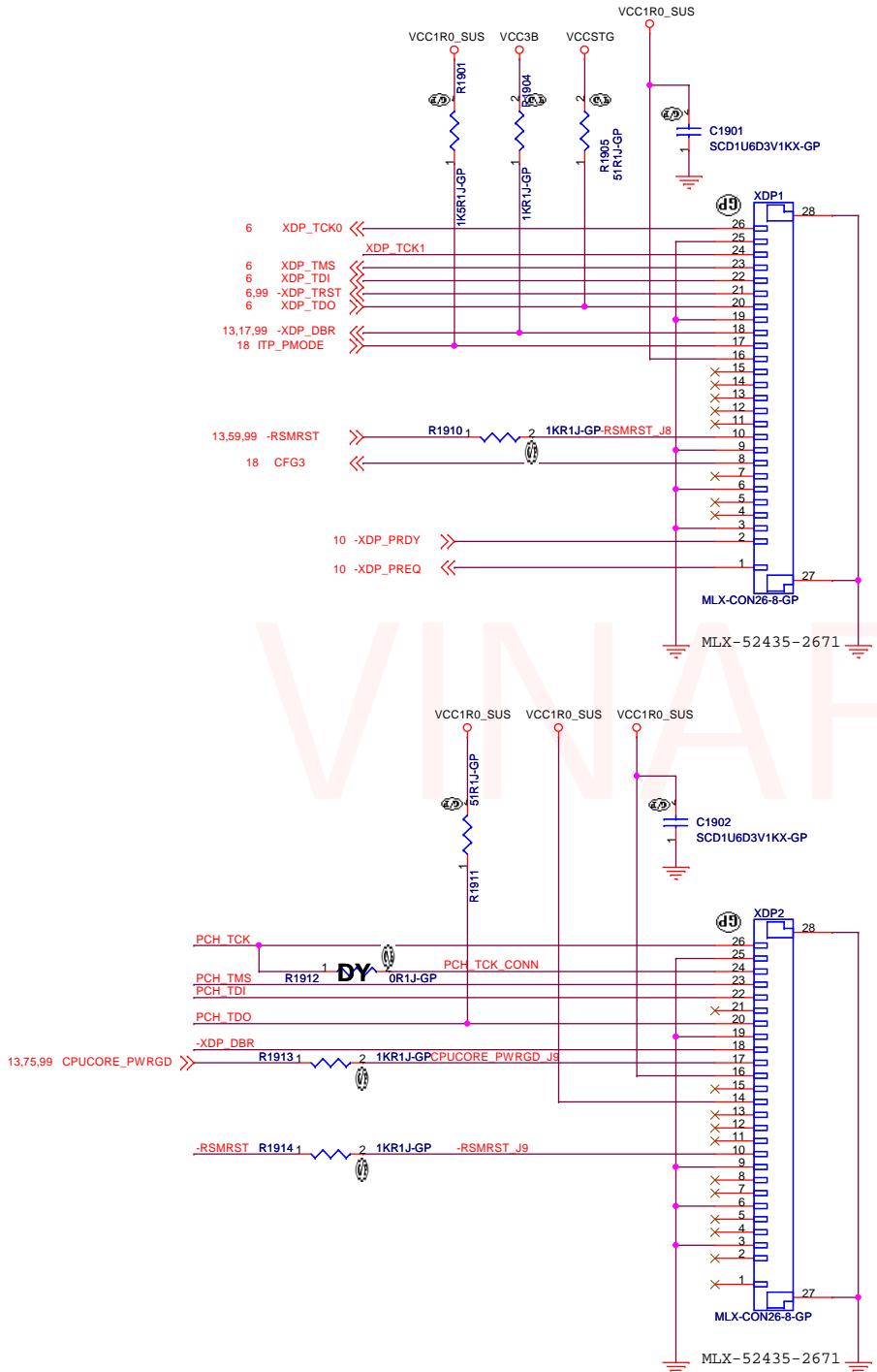
CPU(15/16) : GND

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TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled



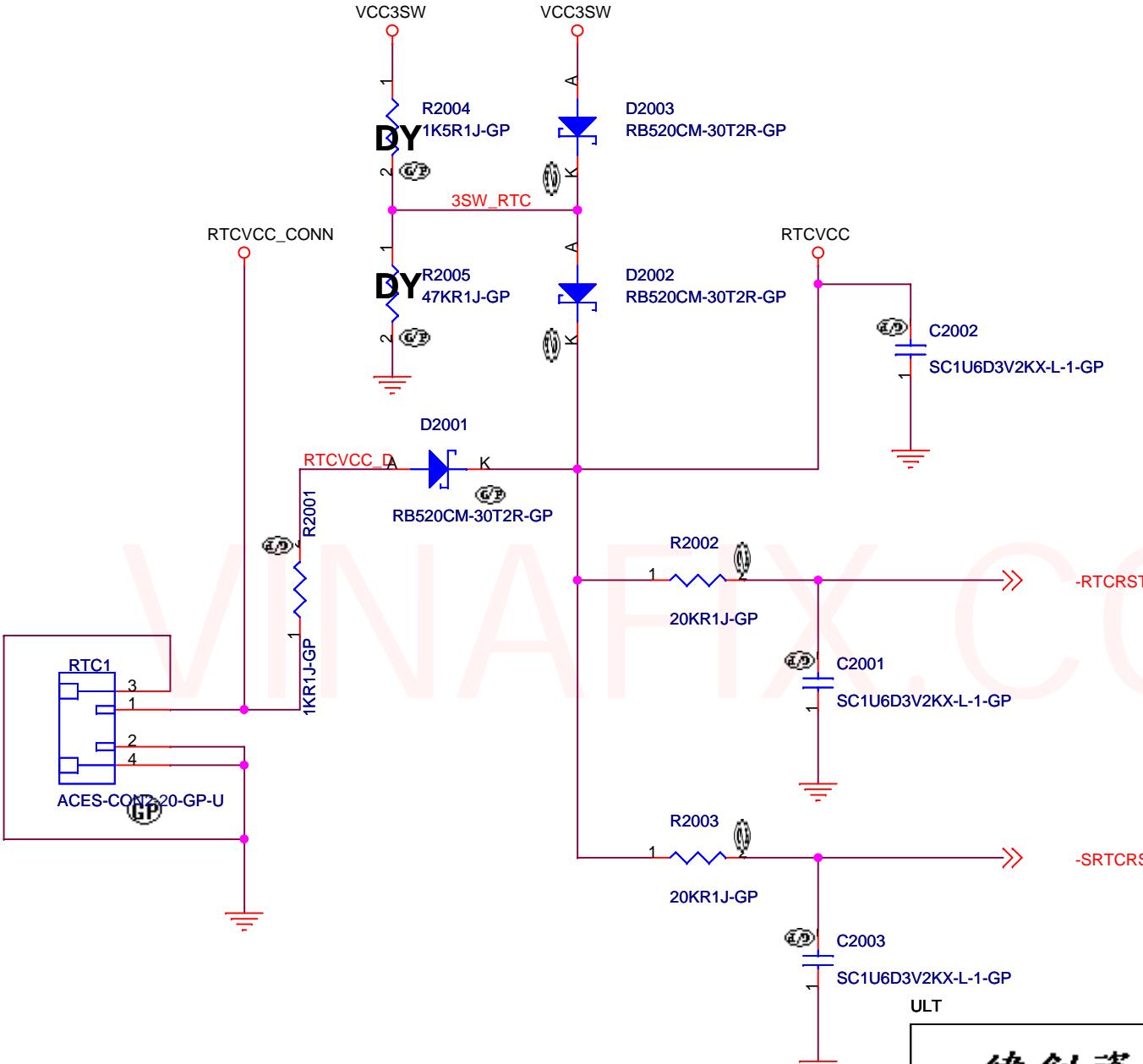


TABLE

	Individual Port	Merged Port	DCI 2.0 w/o Connector
R610	ASM	ASM	ASM
R611	ASM	NO_ASM	NO_ASM
R612	ASM	NO_ASM	NO_ASM
R603	ASM	NO_ASM	NO_ASM
R604	ASM	NO_ASM	NO_ASM
R1905	ASM	ASM	ASM
J8	ASM	ASM	NO_ASM
C1901	ASM	ASM	NO_ASM
R1904	ASM	ASM	ASM
R1901	ASM	ASM	NO_ASM
R1910	ASM	ASM	NO_ASM
R1912	NO_ASM	NO_ASM	NO_ASM
R1911	ASM	NO_ASM	NO_ASM
J9	ASM	ASM	NO_ASM
C1902	ASM	ASM	NO_ASM
R1913	ASM	ASM	NO_ASM
R1914	ASM	ASM	NO_ASM
R1902	NO_ASM	ASM	ASM
R1903	NO_ASM	ASM	NO_ASM
R1906	NO_ASM	ASM	ASM
R1907	NO_ASM	ASM	ASM
R1908	NO_ASM	ASM	ASM
R1909	NO_ASM	ASM	ASM

LOGIC
↑

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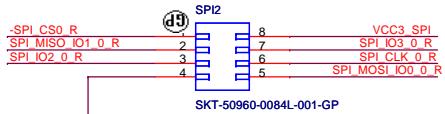
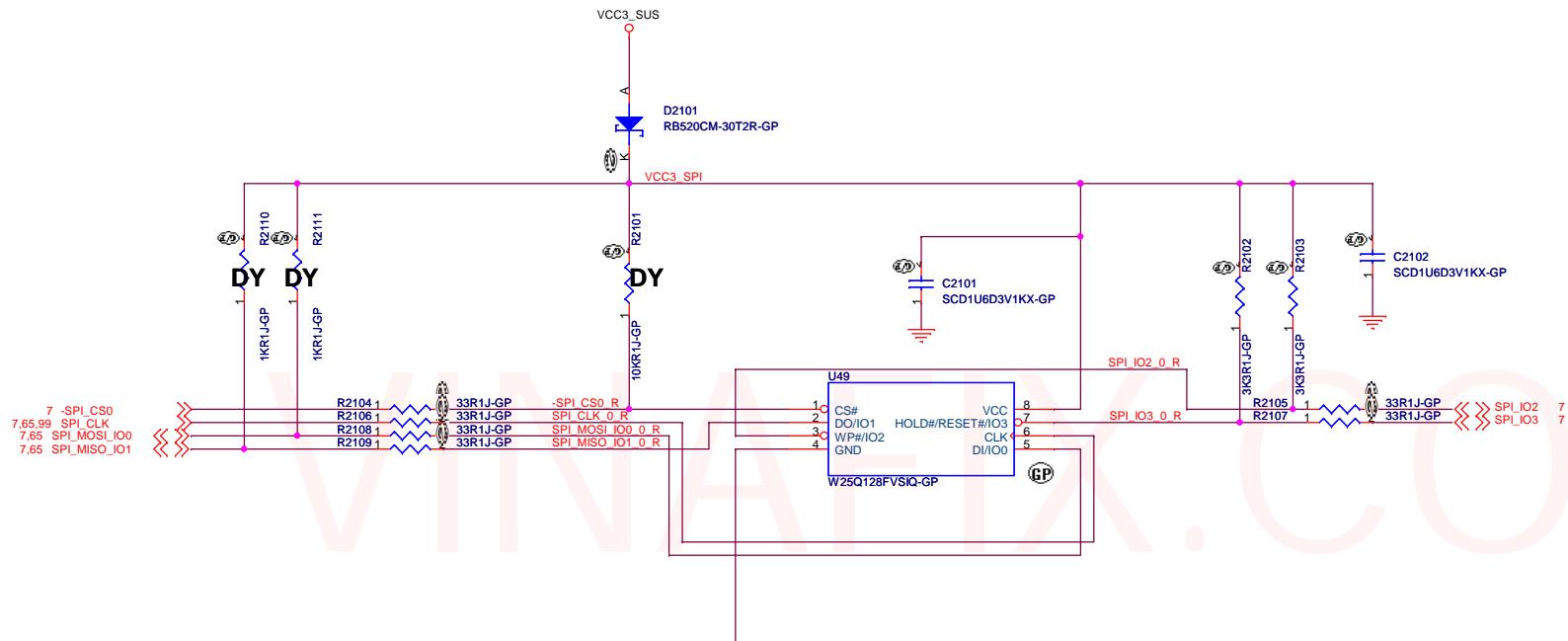


TABLE

Skylake	R2111	R2110	R2102	R711
PreES / ES	ASM	ASM	DY	ASM
After QS	DY	DY	ASM	DY

LOGIC

16MB SOIC8
WINBOND W25Q128FVSIQ
MACRONIX MX25L12873FM2I-10G
MICRON N25Q128A13ESED0F
EON EN25QH128A-104HIP



Co-Layout Design on U49

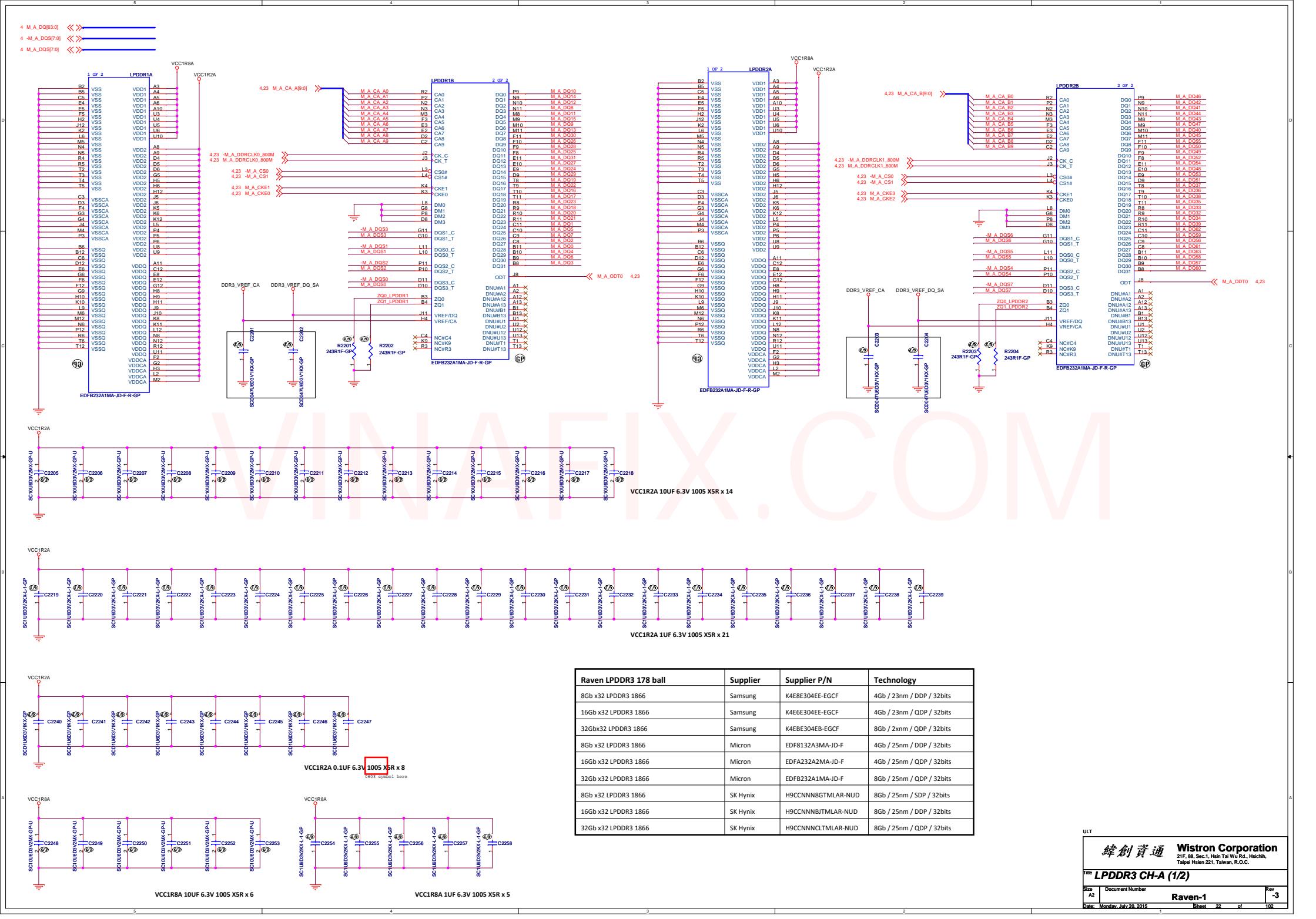
TABLE

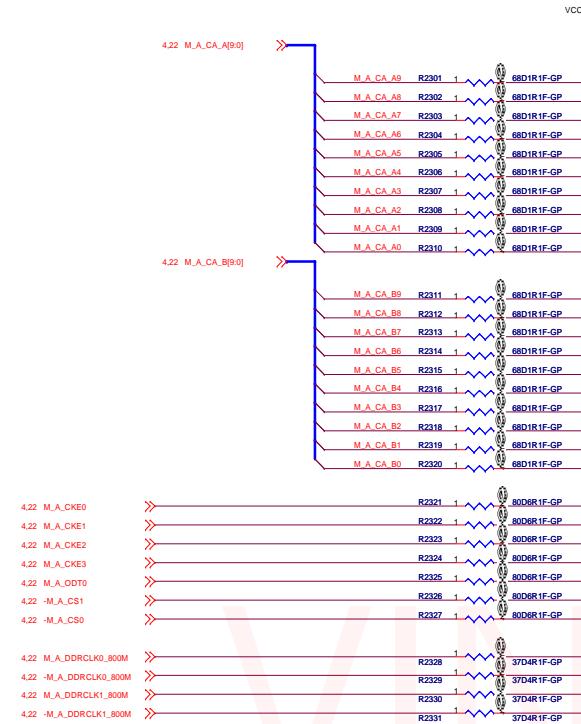
SF100 PIN HEADER INTERFACE (TOP VIEW)

1	VCC	D2101.K	GND	GND	2
3	CS#	R2104.2	R2106.2	CLK	4
5	MISO	R2109.2	R2108.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

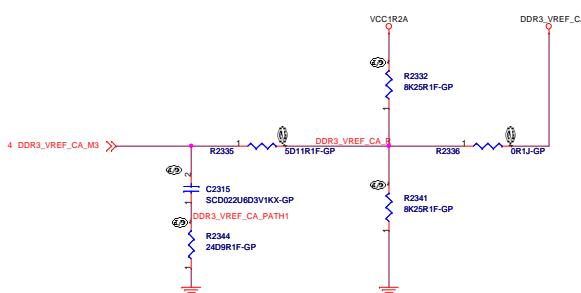
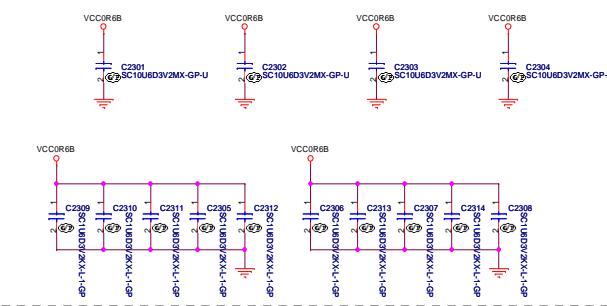
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SPI FLASH	
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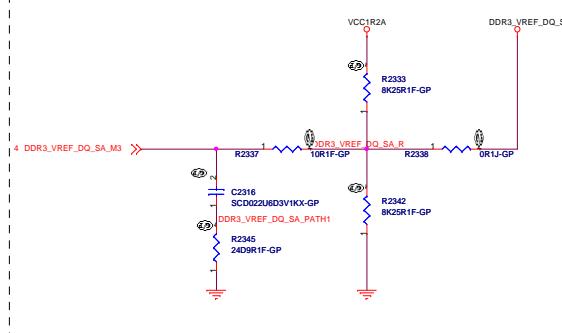




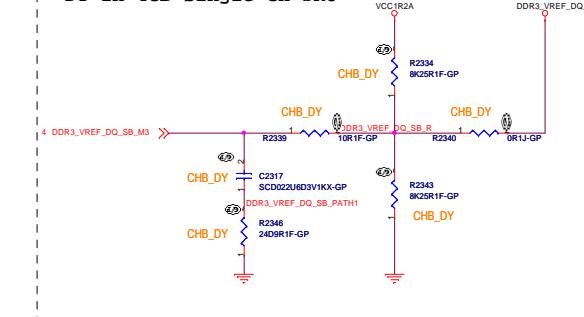
LPDDR3 Vtt Decoupling



PLACE NEAR A Channel

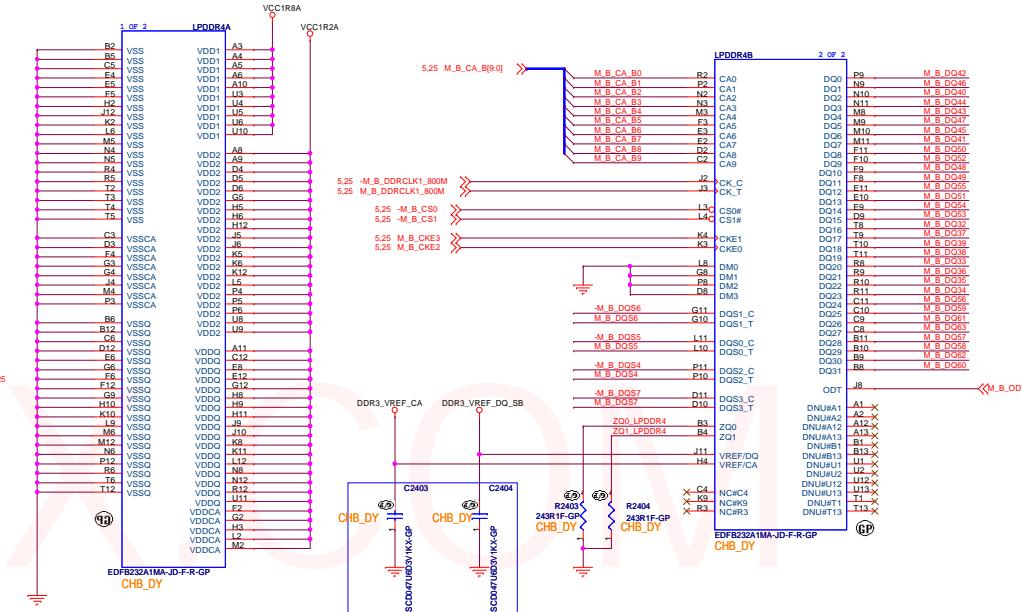
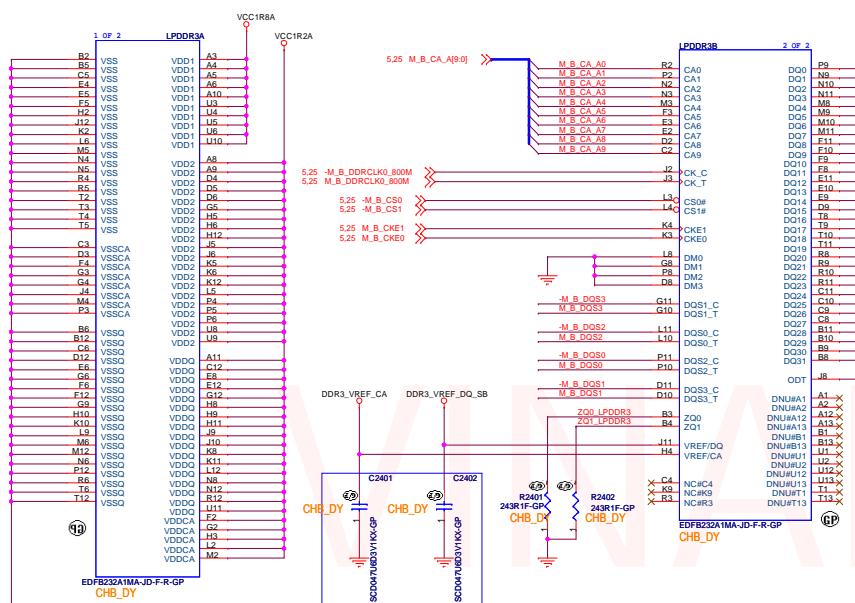


PLACE NEAR B Channel DY in 4GB single CH SKU

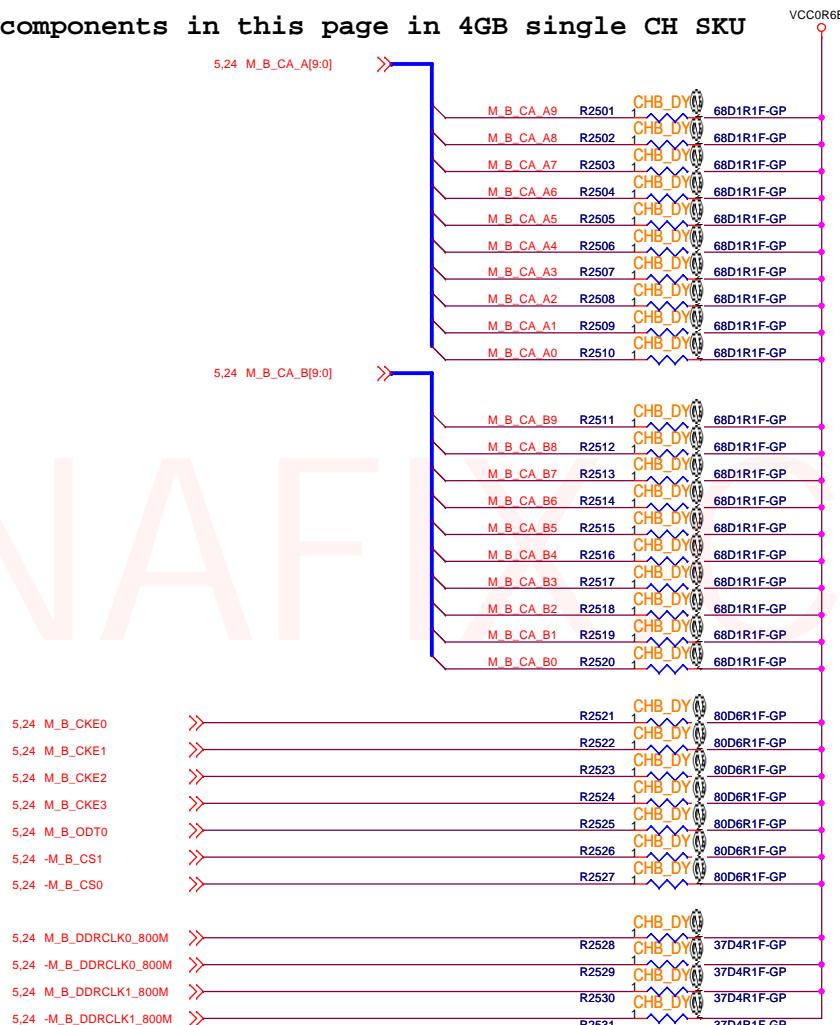


DY all components in this page in 4GB single CH SKU

5 M_B_DQ[63:0] <>
5 -M_B_DQS[7:0] <> 
5 M_B_DQS[7:0] <> 

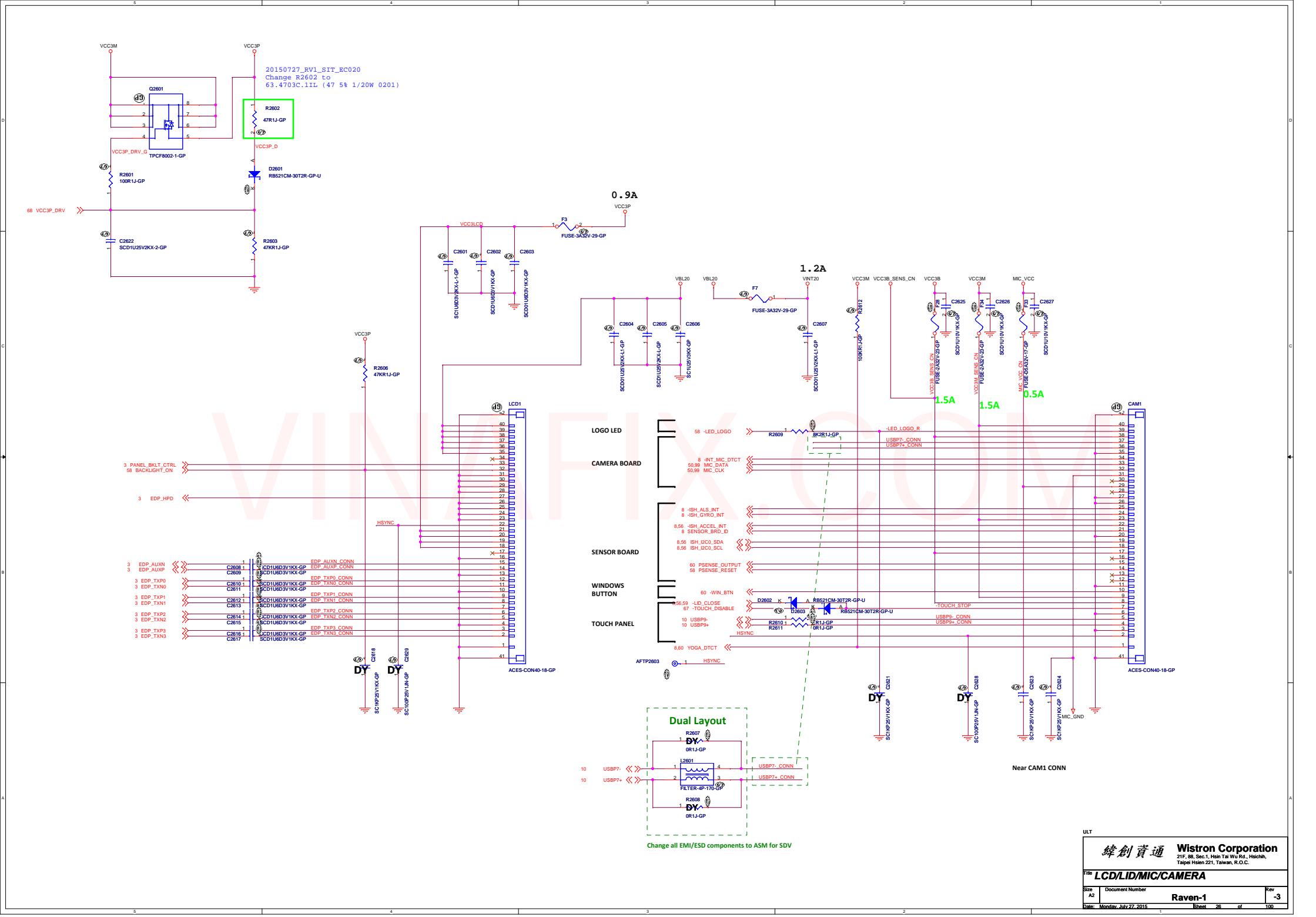


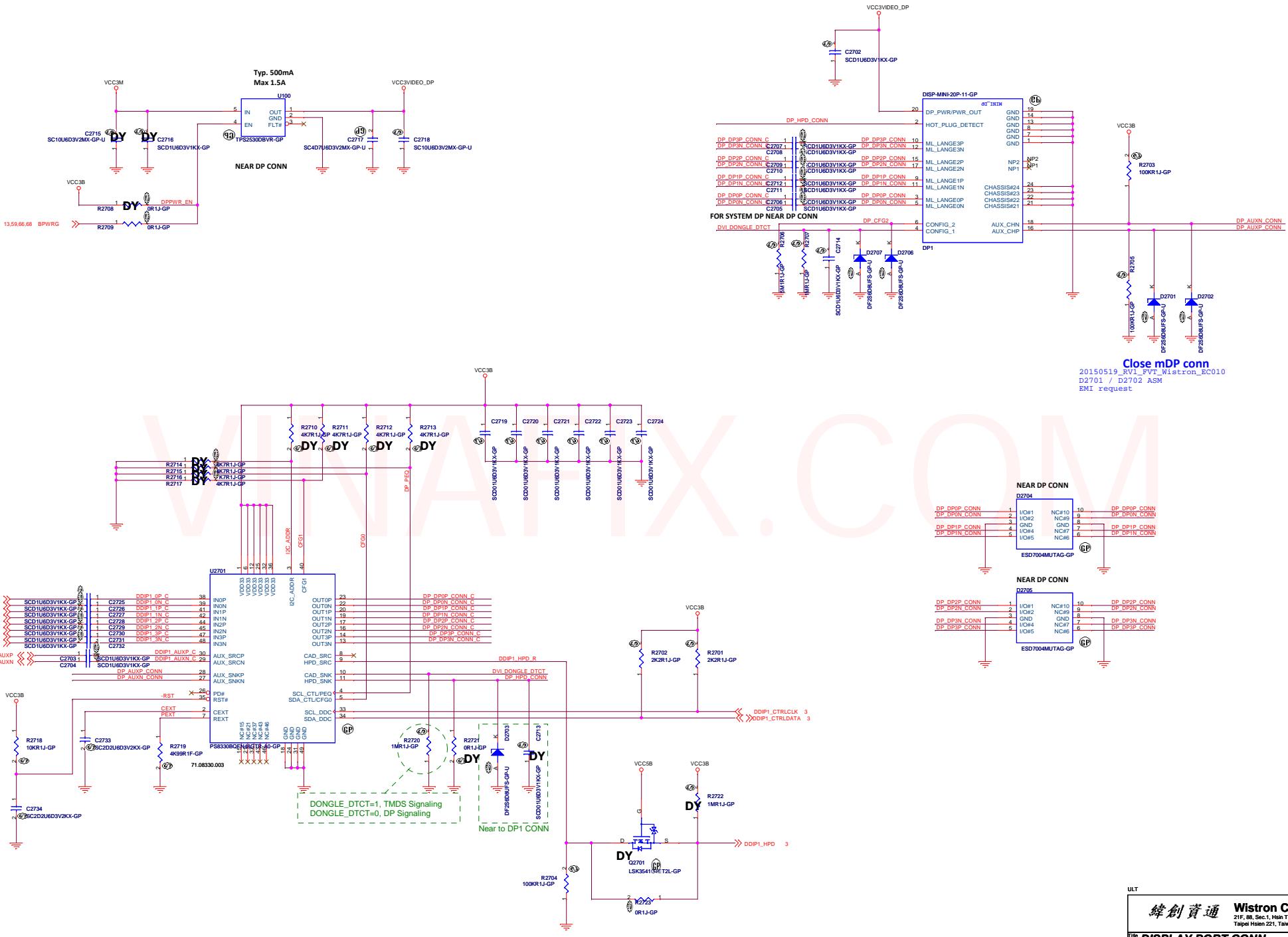
DY all components in this page in 4GB single CH SKU



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Title LPDDR3_CH-B (2/2)		
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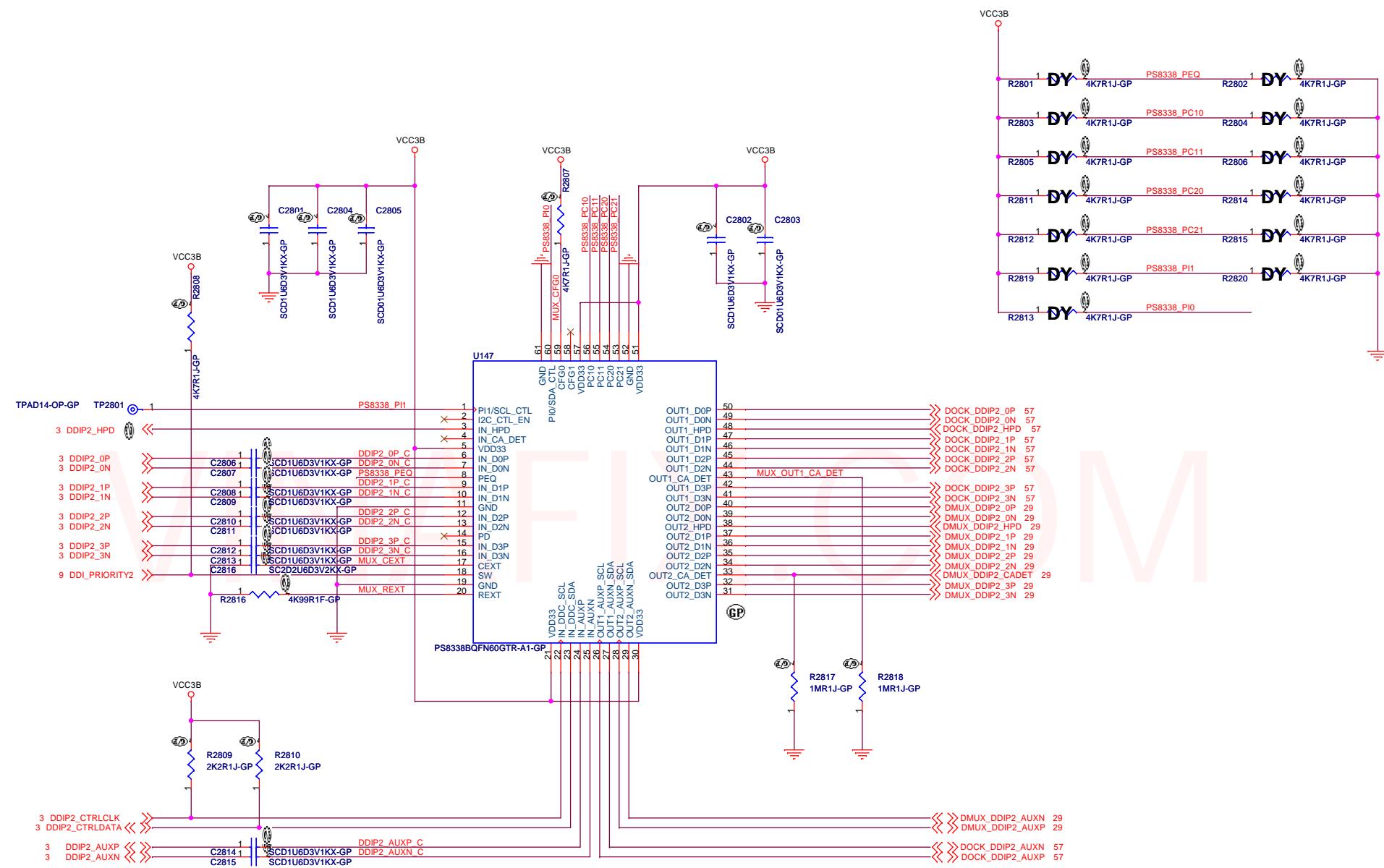
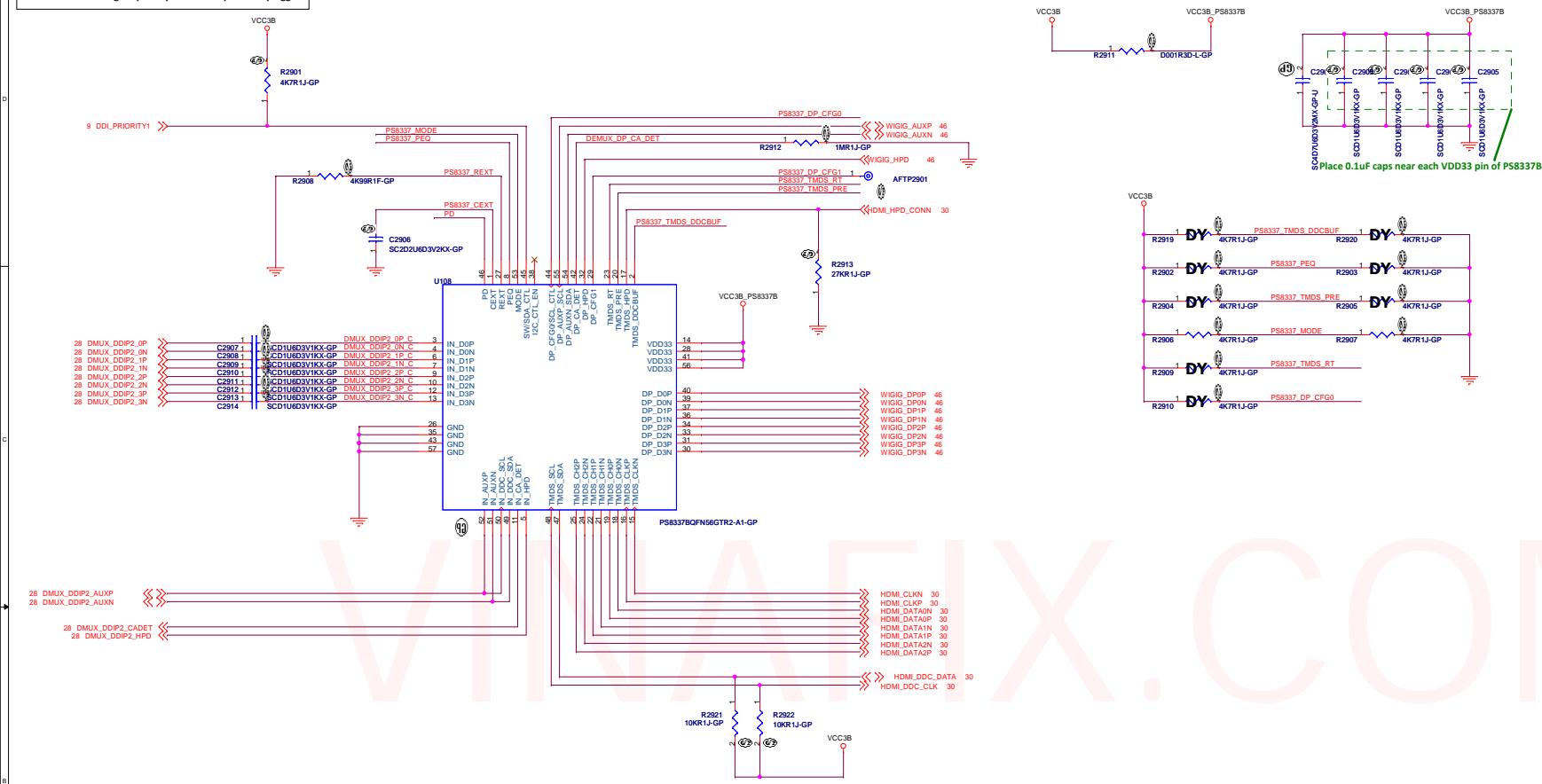
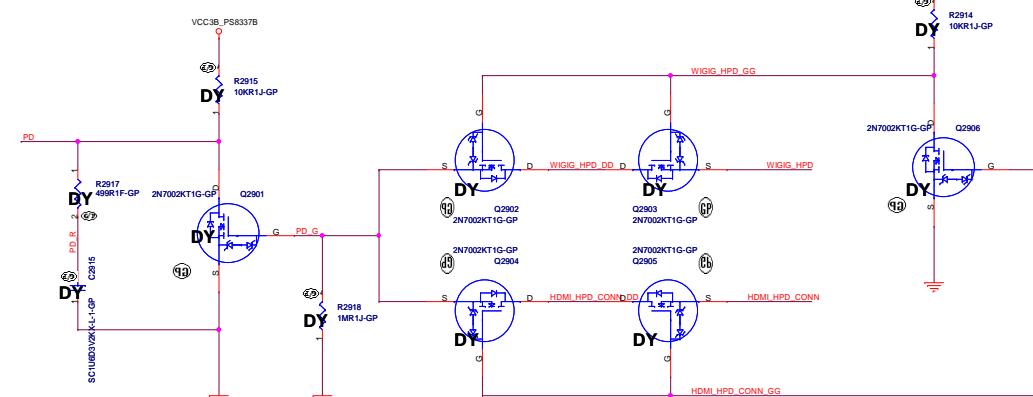


TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged
H TMDS Port has higher priority when both ports are plugged



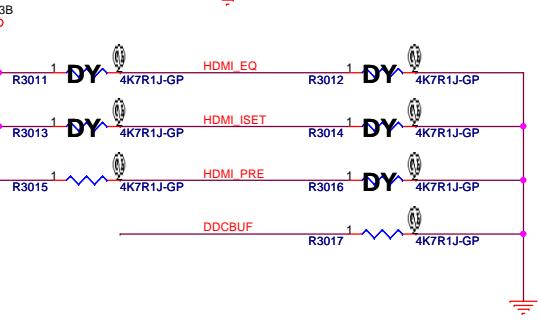
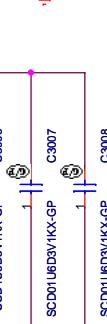
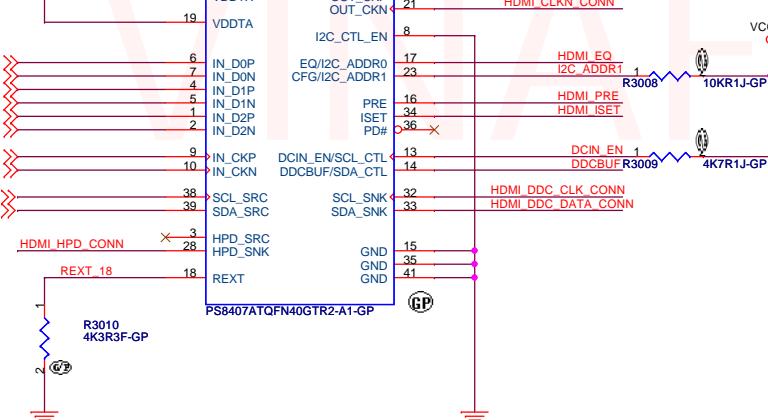
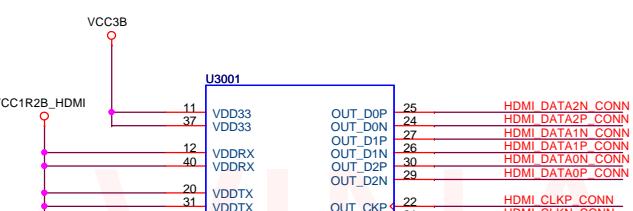
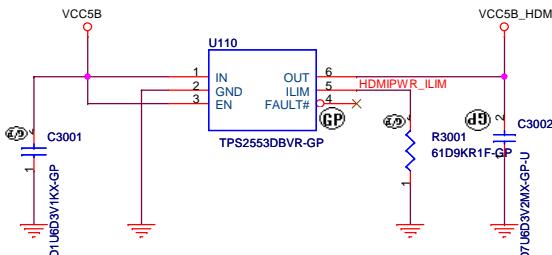
HPD/PD control circuit for PS8337



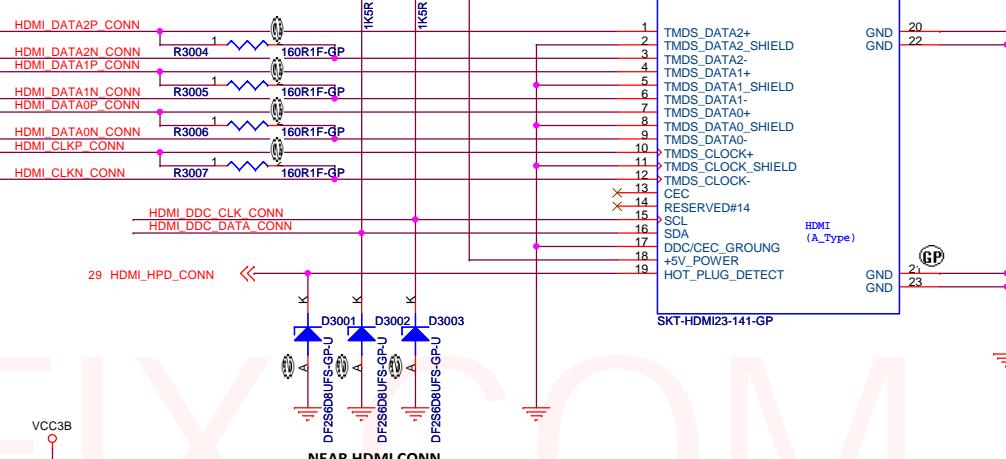
U110

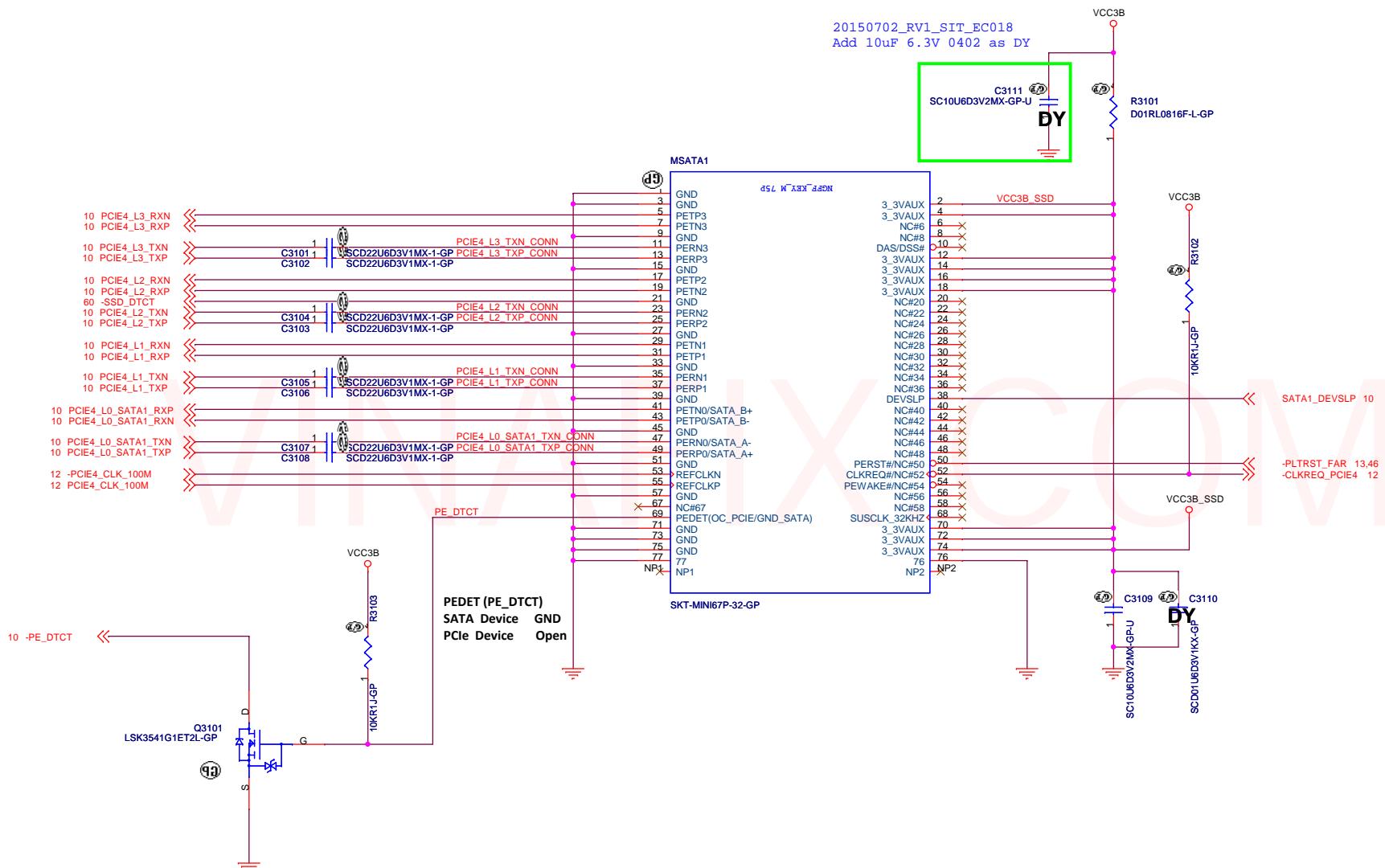
main TI TPS2253DBVR
2nd GMT G517AL1TB1U

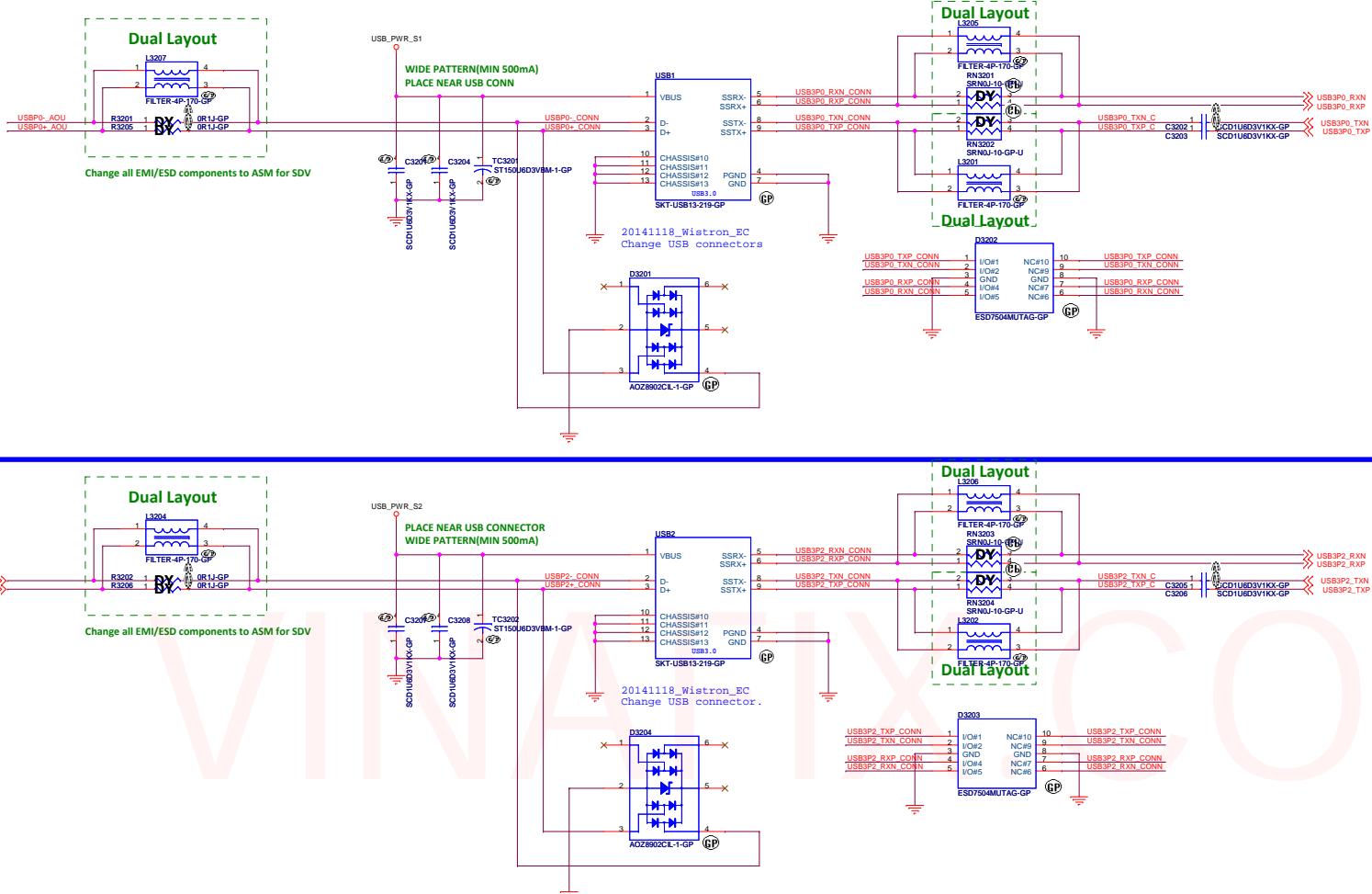
Current Limit Target : 400mA
Requirement : 350mA
HDMI Spec : 50mA - 500mA

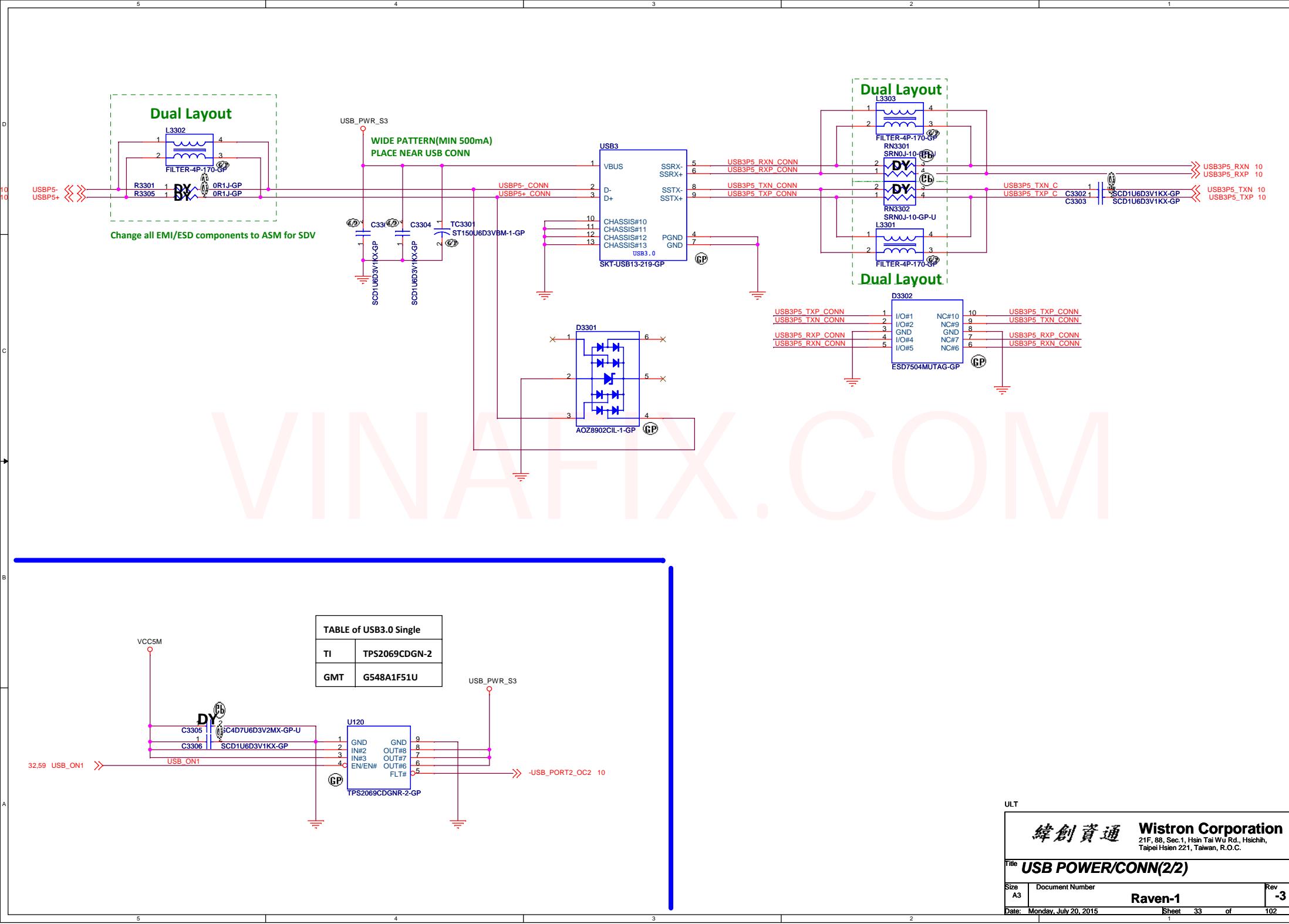


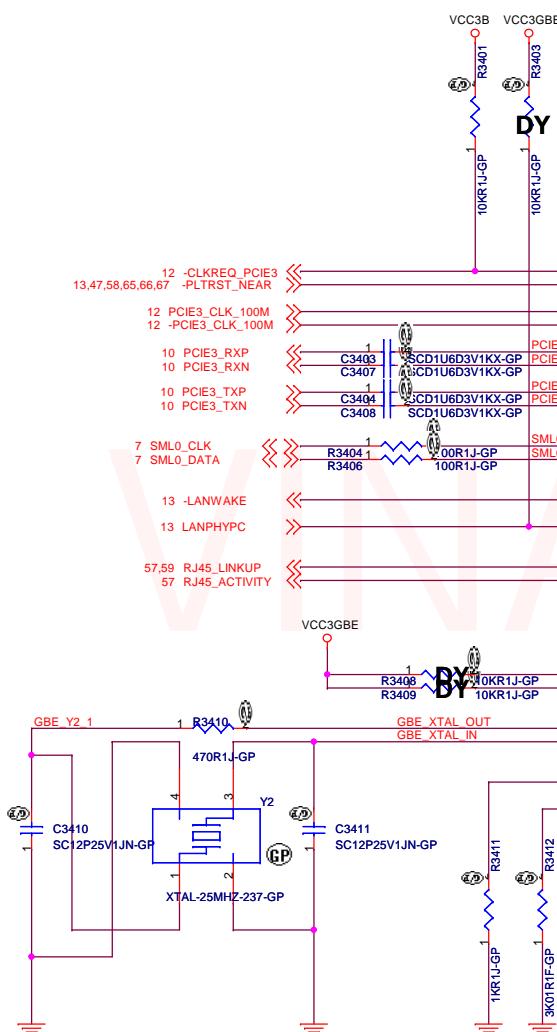
No need diode here because TPS2553 has reverse voltage protection function.







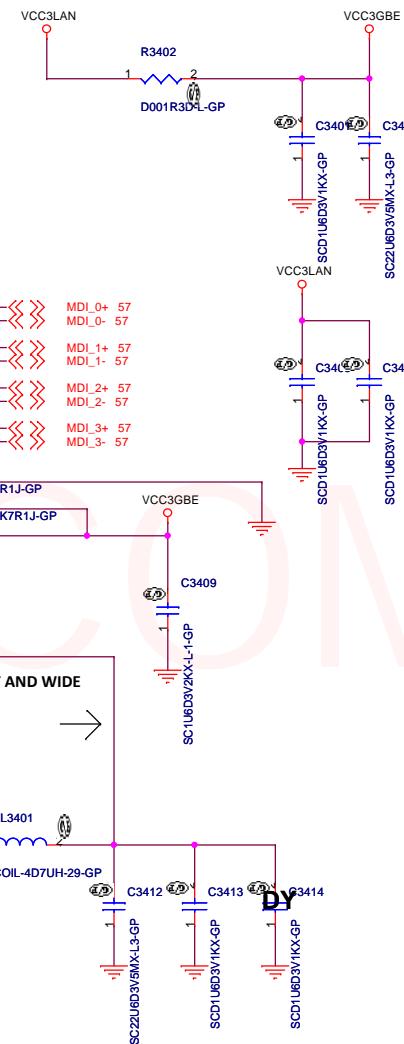




TABLE

vPro Capability		
GbE PHY	Yes	No
U?	Jacksonville-LM	Jacksonville-V

LOGIC

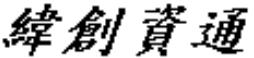


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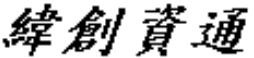
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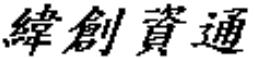
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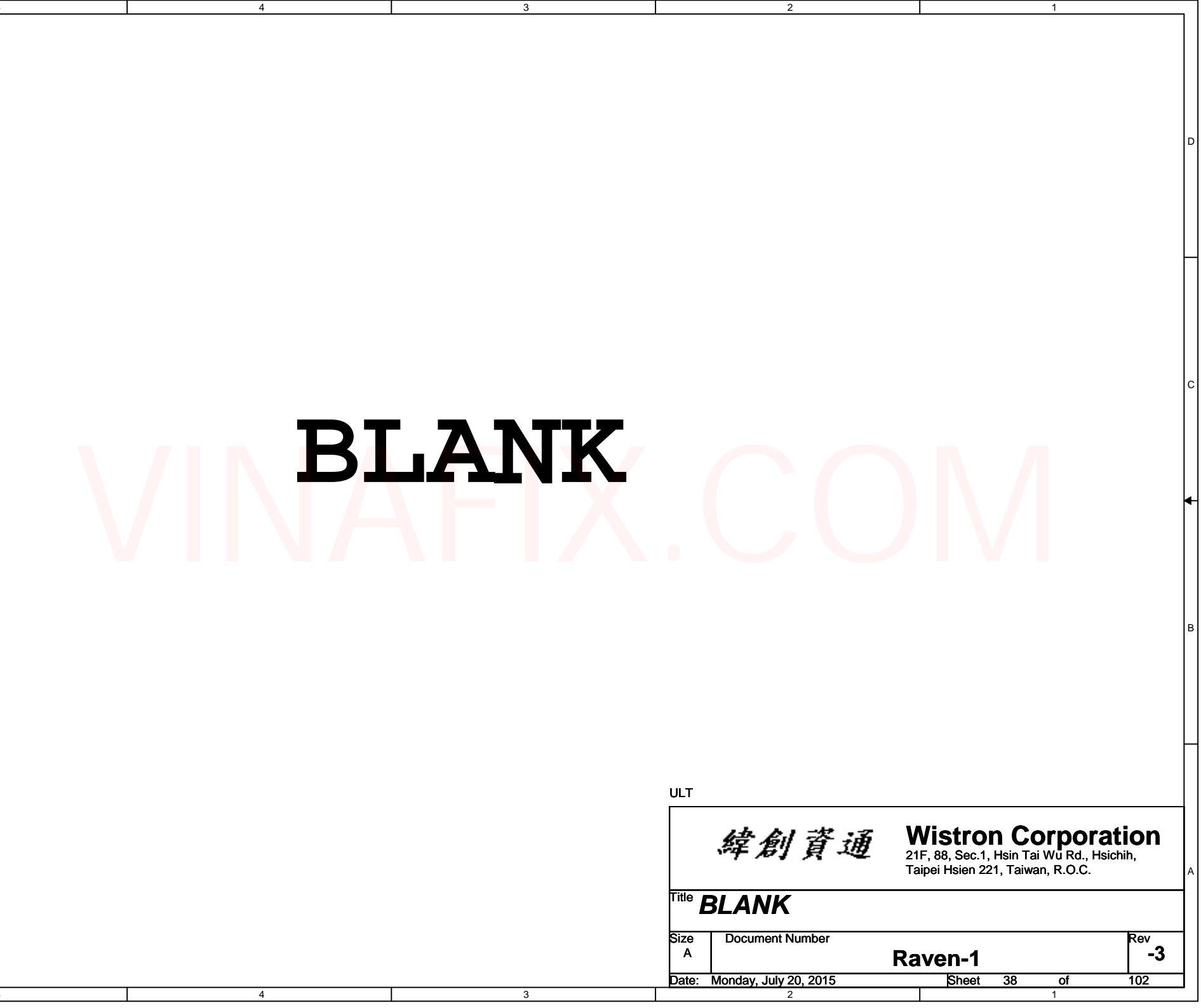
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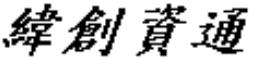
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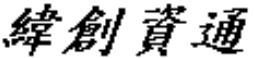
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Size A	Document Number	Rev -3
Raven-1		Date: Monday, July 20, 2015
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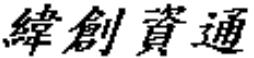
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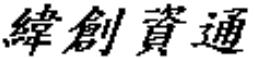
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Size A	Document Number	Rev -3
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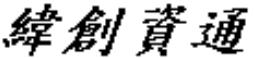
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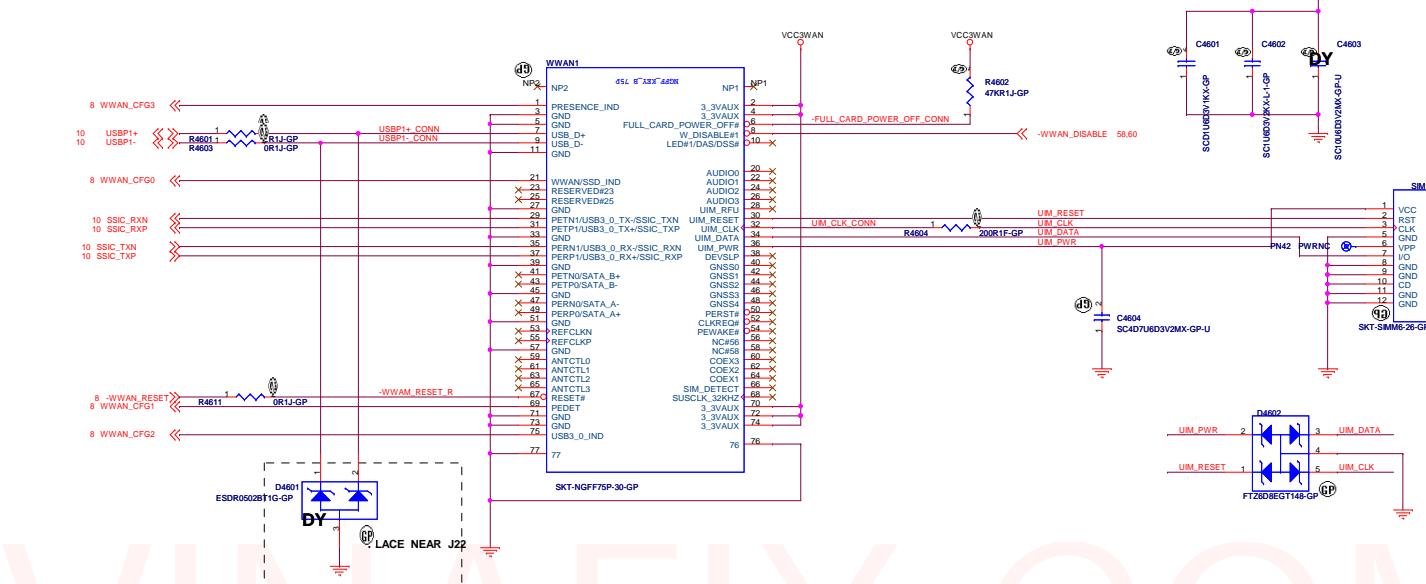
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Raven-1		Date: Monday, July 20, 2015
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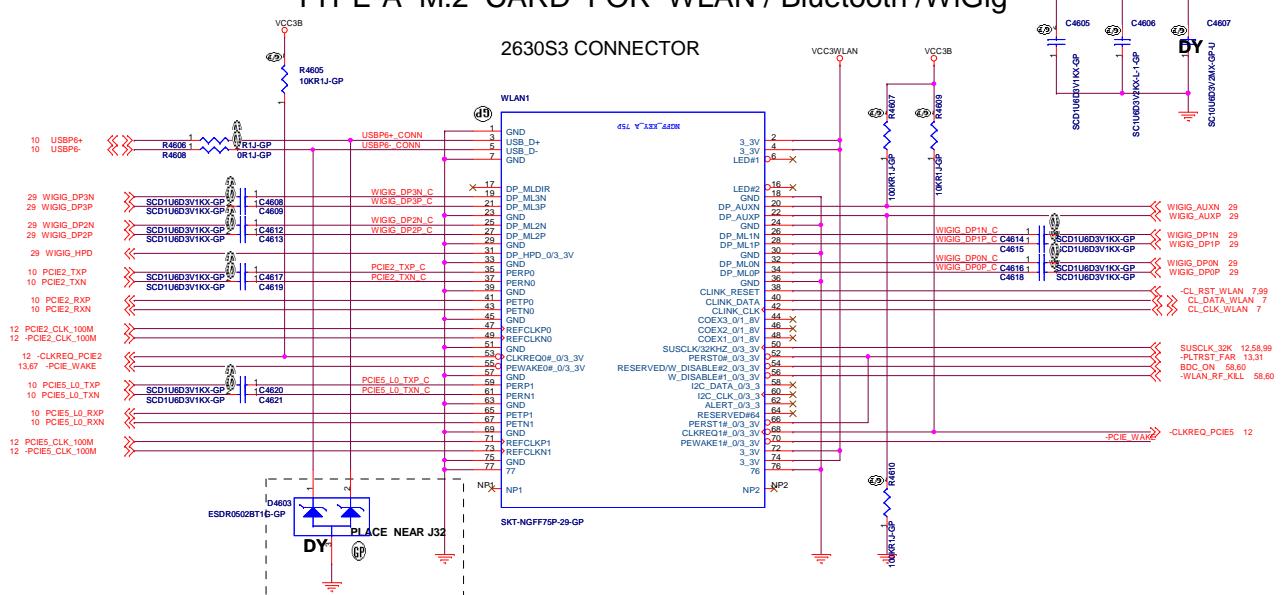
TYPE-B M.2 CARD FOR WWAN

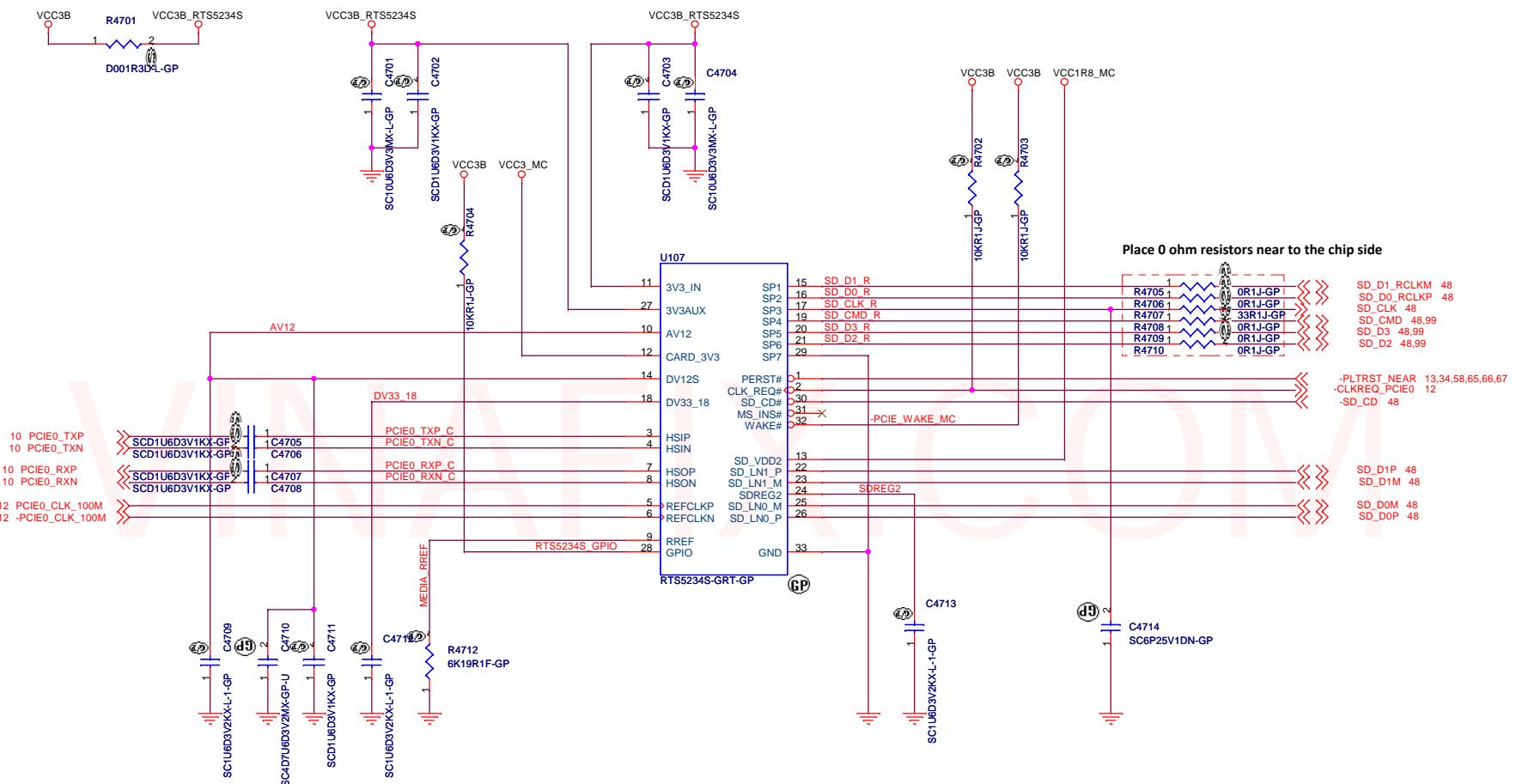
3042S3 CONNECTOR



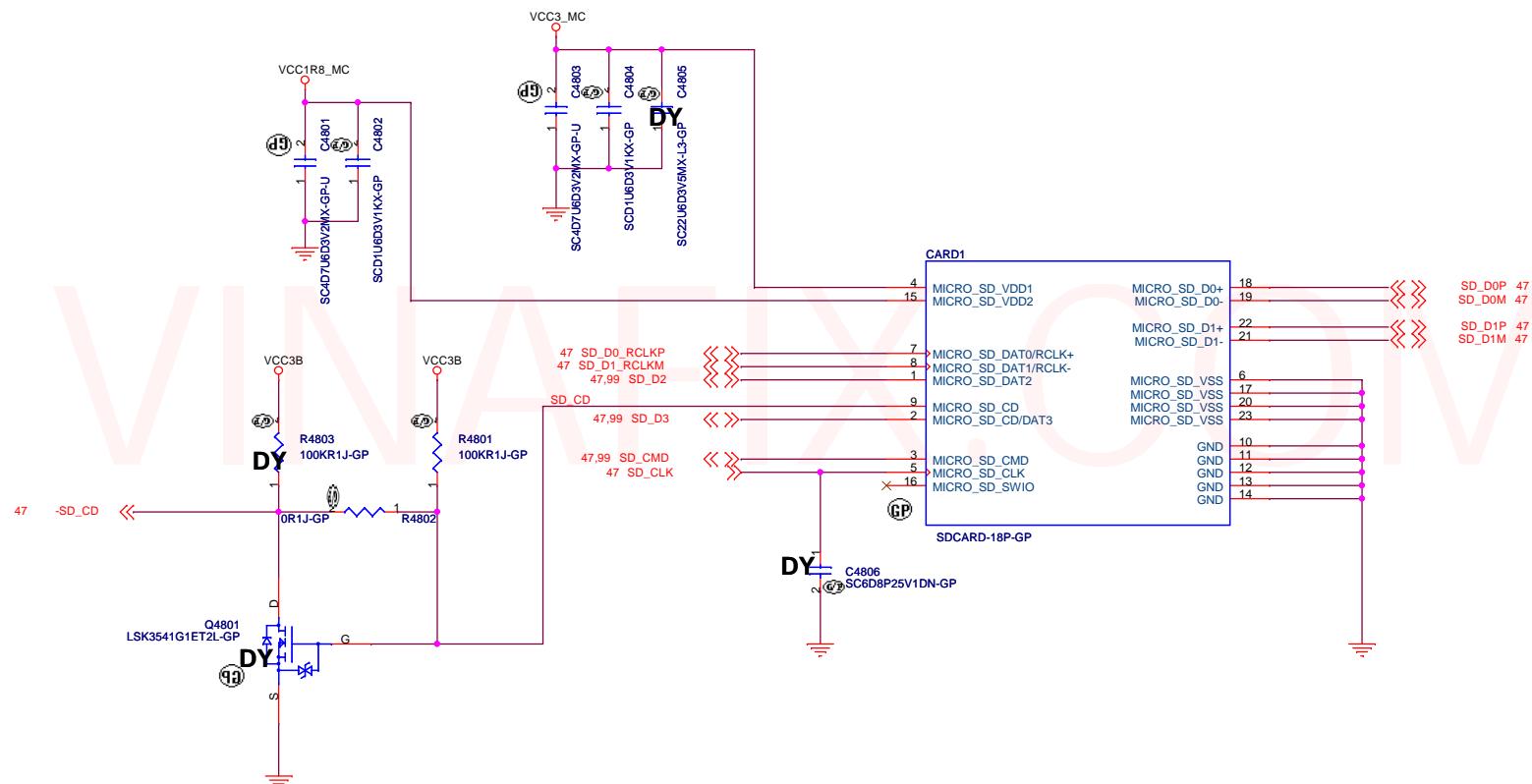
TYPE-A M.2 CARD FOR WLAN / Bluetooth /WiGig

2630S3 CONNECTOR



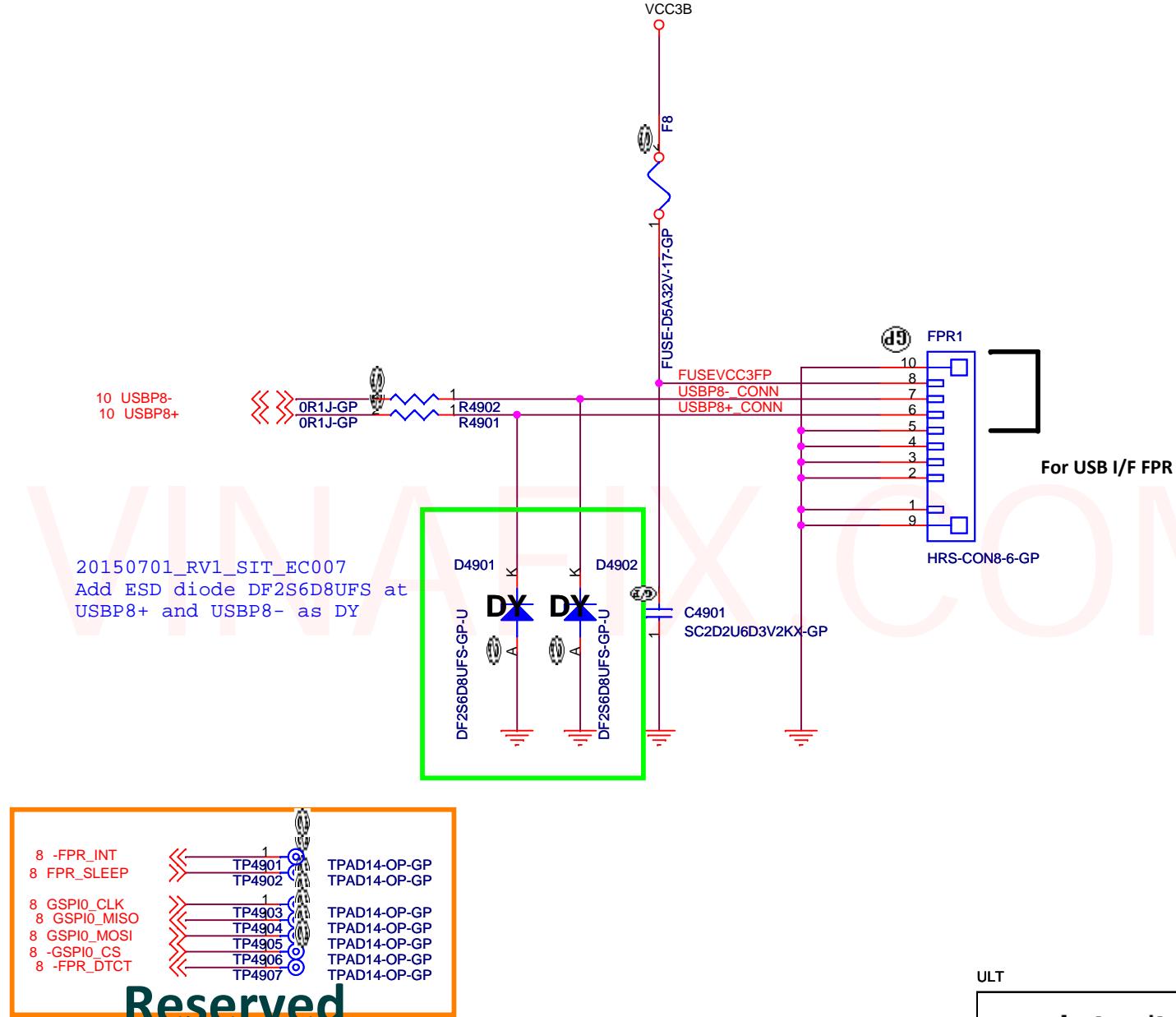


MicroSD Slot (UHS-II)



ULT

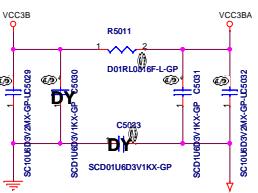
Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title MEDIA CARD INTERFACE		
Size A3	Document Number	Rev -3
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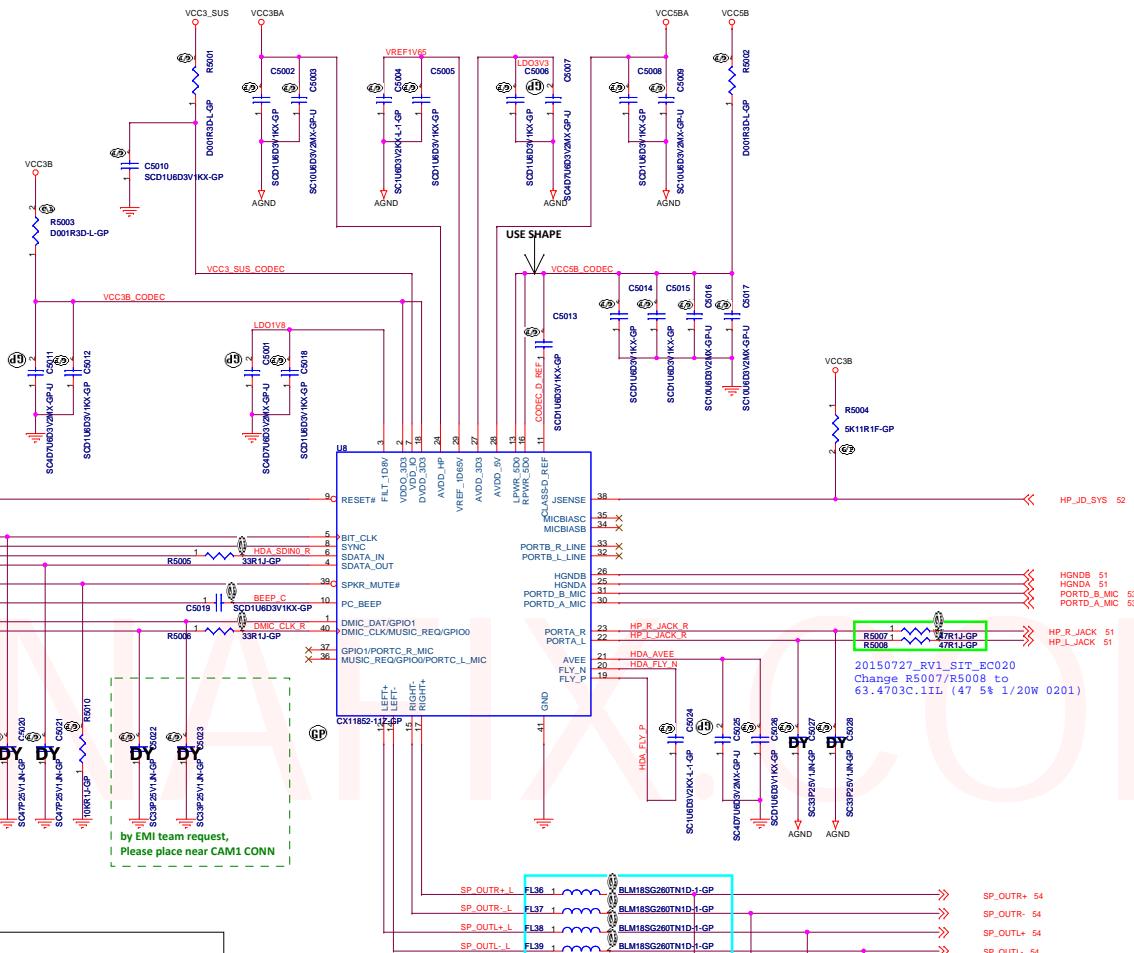
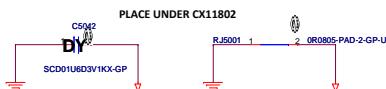
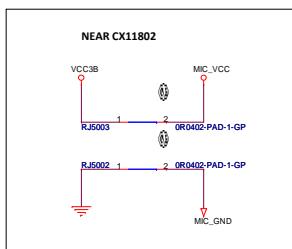
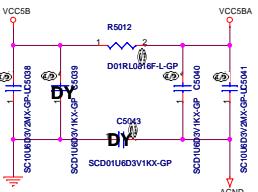
20141023_Wistron_EC032 (Canceled)
Delete FPR SPI interface and reserved testpoints.

Reserved

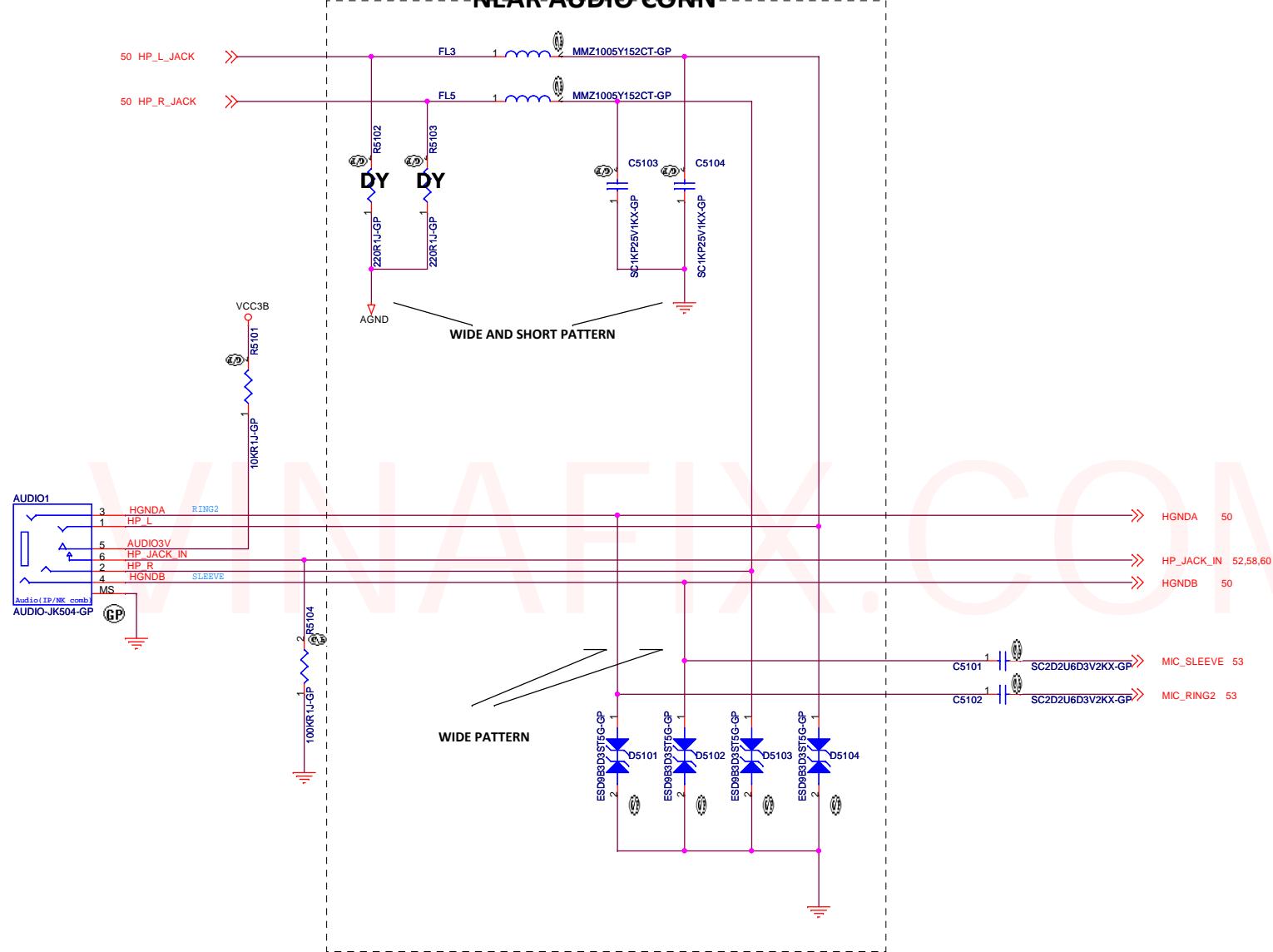
R7
Place TOP Layer > 0.01 0816_1/3W
Place BOTTOM Layer > 0.001 1608 1/10W



R7
Place TOP Layer > 0.01 0816_1/3W
Place BOTTOM Layer > 0.001 1608 1/10W

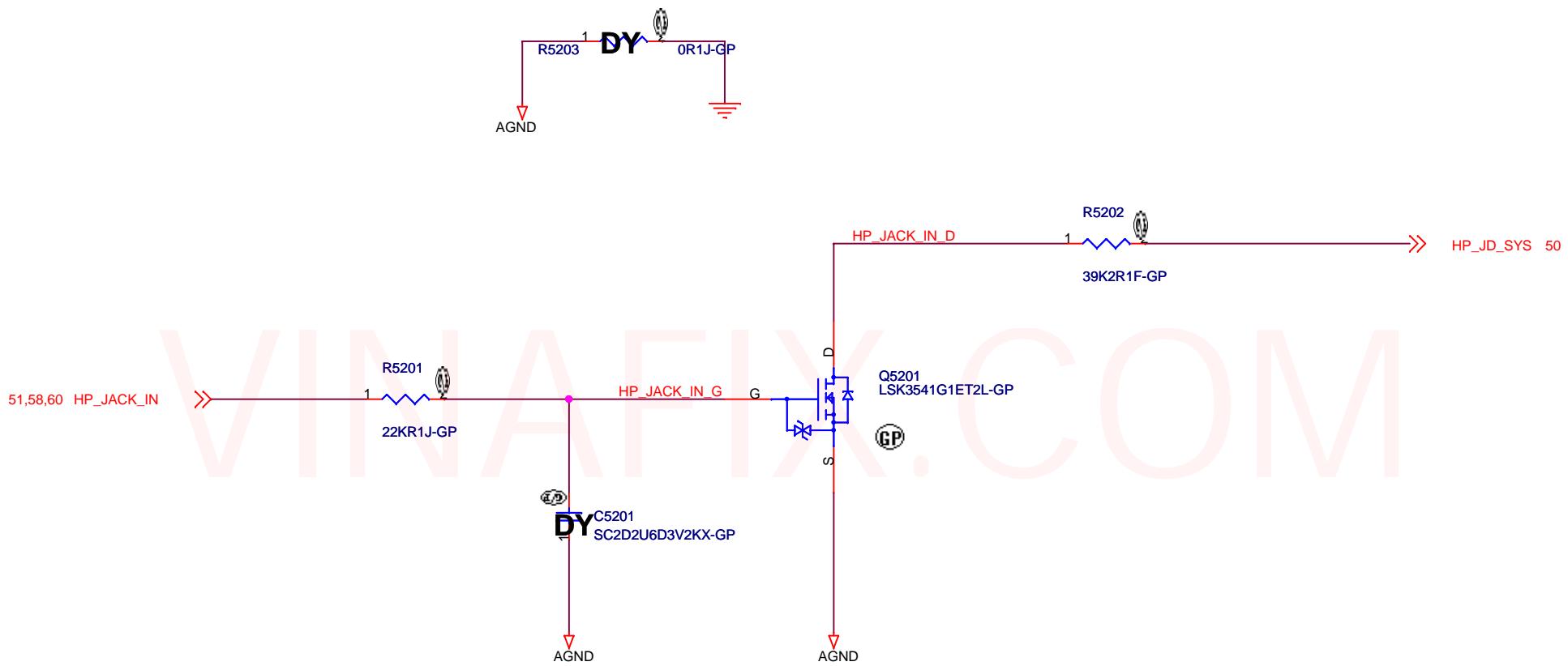


NEAR AUDIO CONN



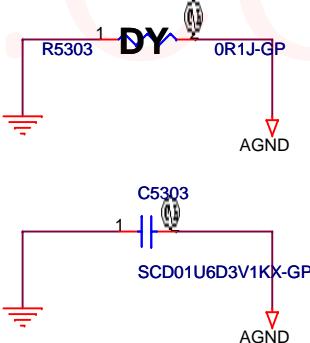
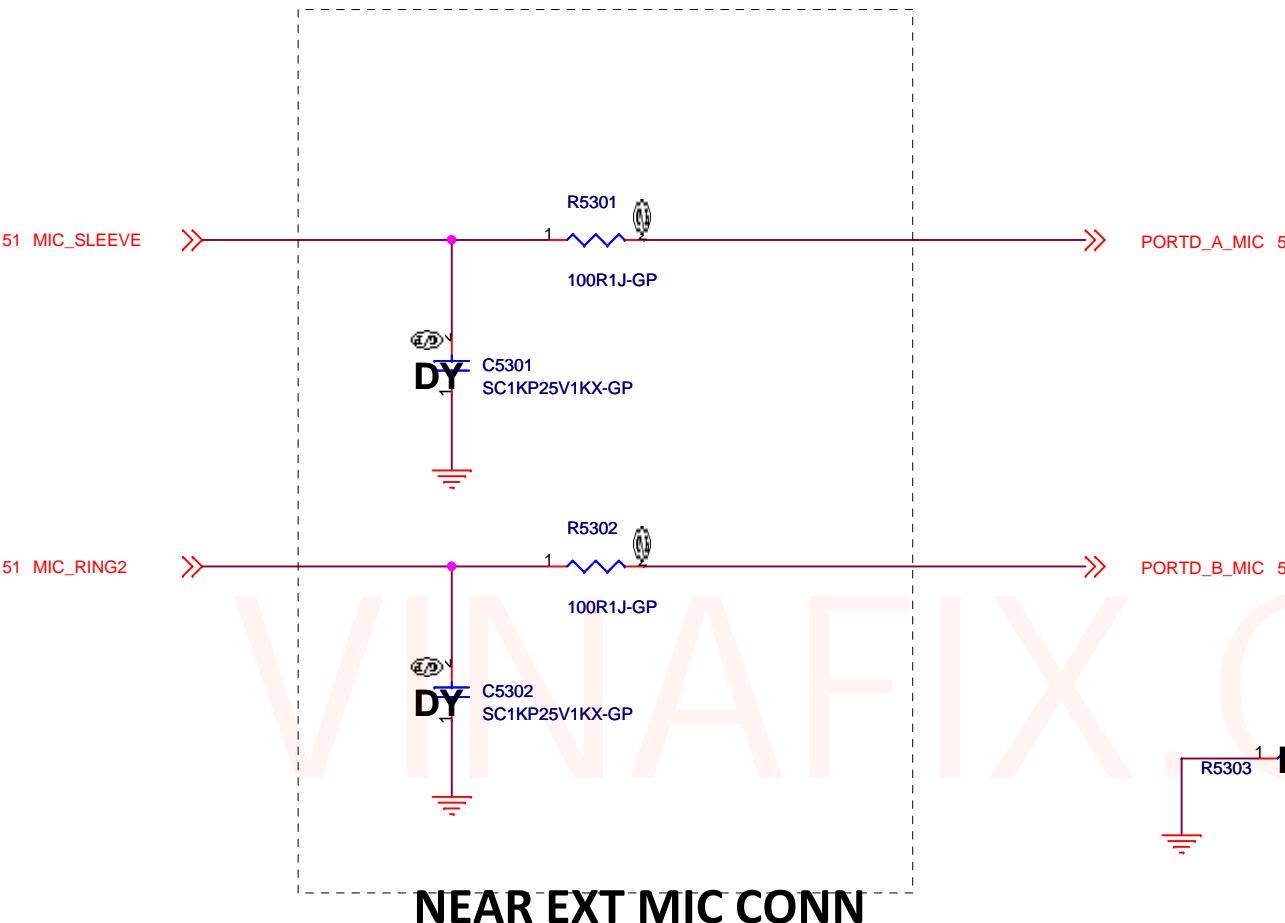
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Title AUDIO CONNECTOR		
Size A3	Document Number	Rev -3
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
AUDIO JACK SENSE		
Size A4	Document Number Raven-1	Rev -3
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50 SP_OUTL+

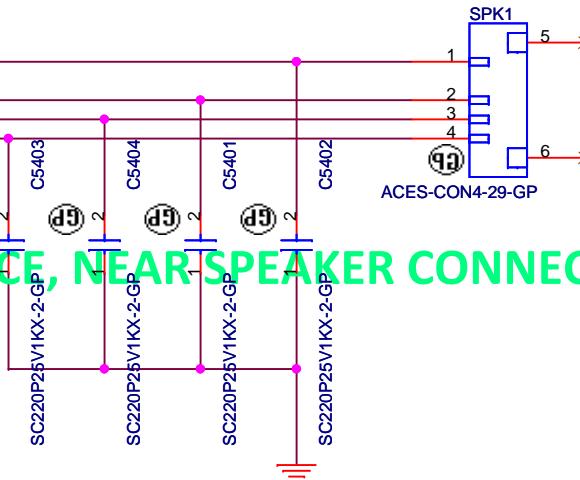
50 SP_OUTL-

50 SP_OUTR+

50 SP_OUTR-



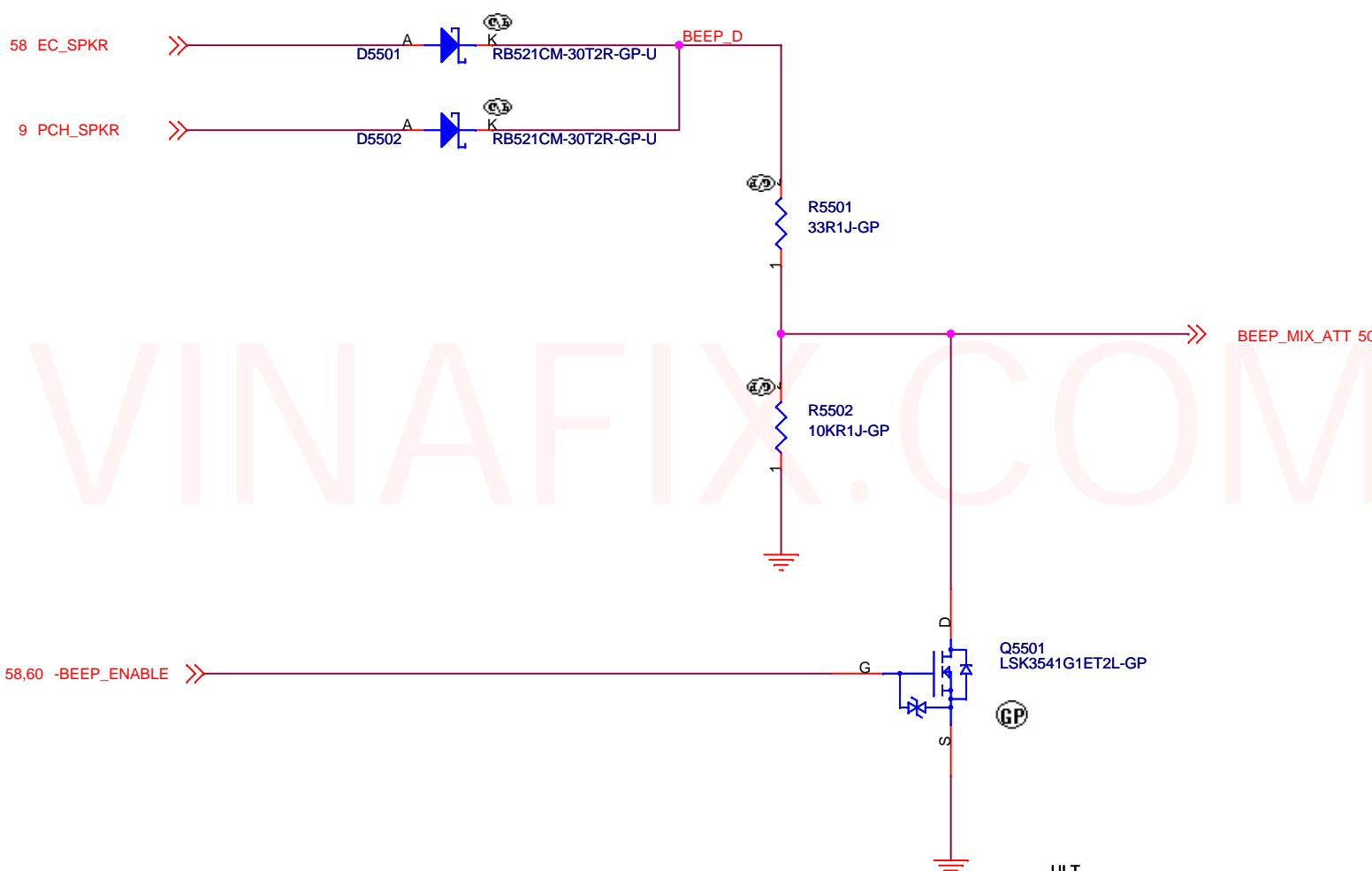
PLACE, NEAR SPEAKER CONNECTOR SPK1



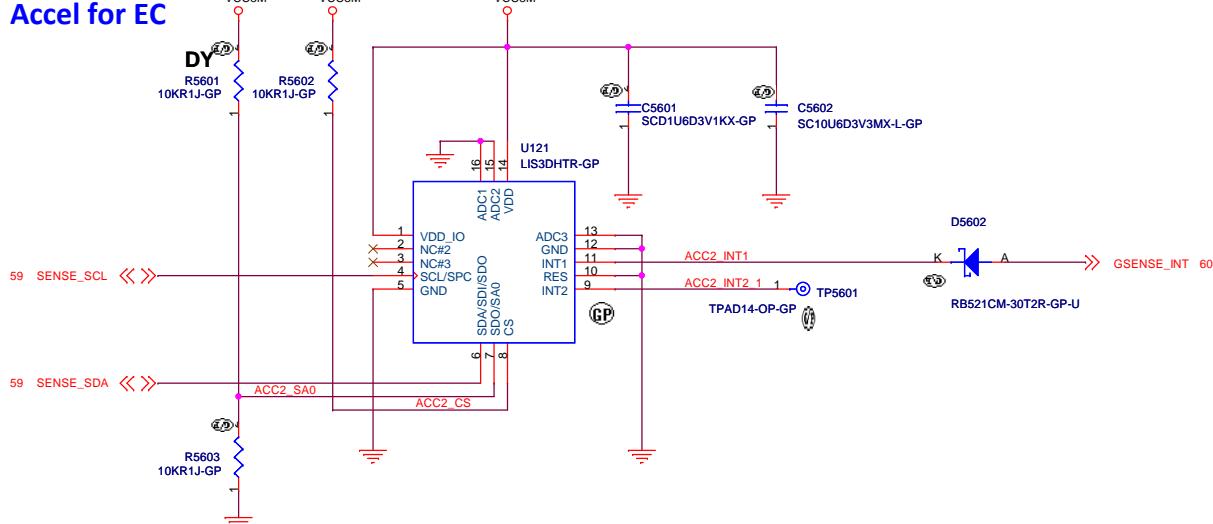
20150714_RV1_SIT_Wistron_EC005
Remove SPK2 related components

ULT

緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
AUDIO SPEAKER		
Size A4	Document Number Raven-1	Rev -3
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Accel for EC

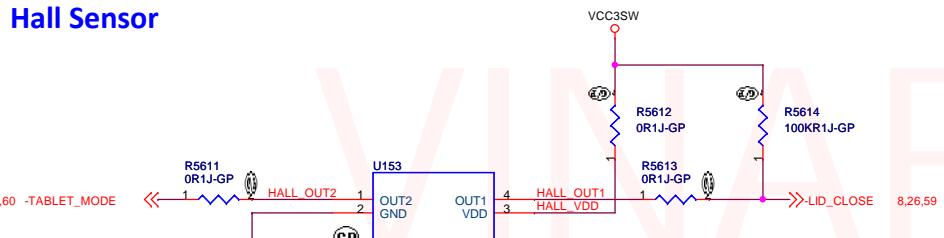


TABLE

CS	Mode Selection
H	I ² C Mode
L	SPI Mode

← Logic

Hall Sensor

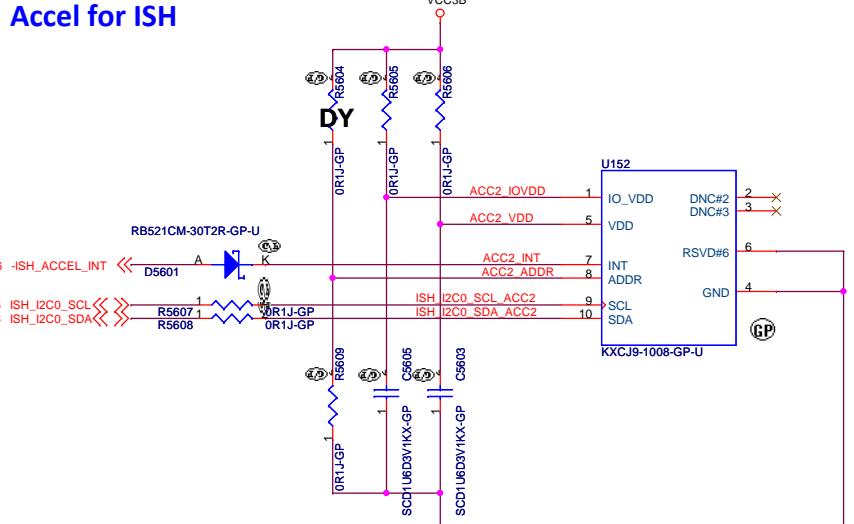


TABLE

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

 Log

Accel for ISH

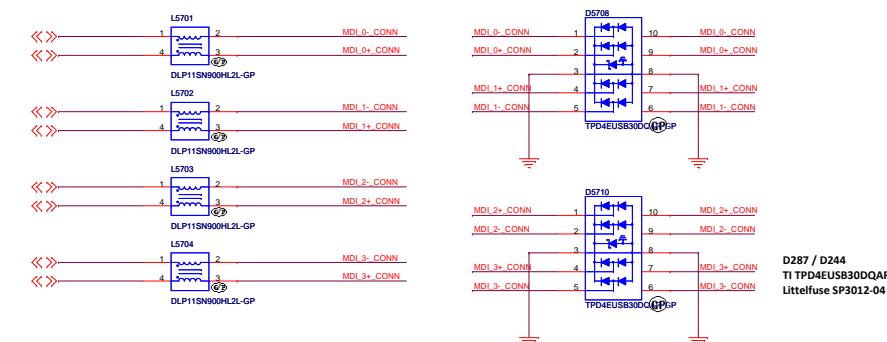
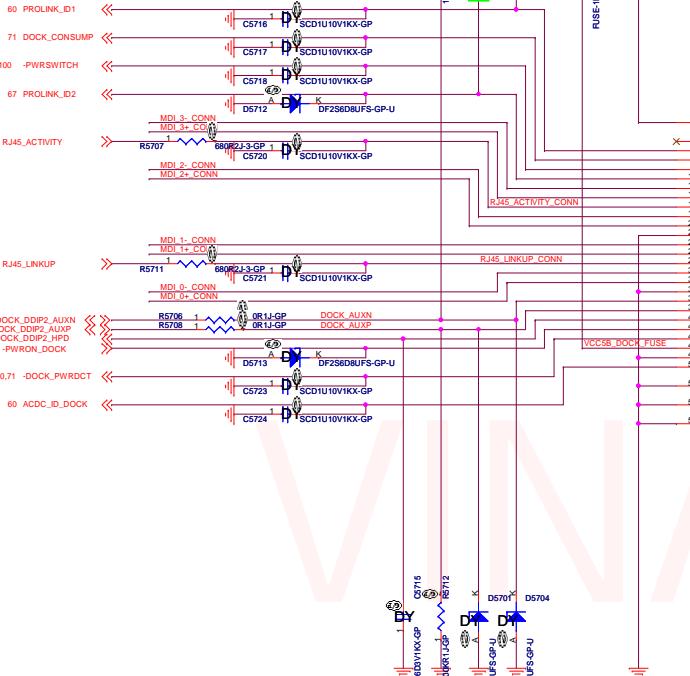


20150727_RV1_SIT_EC021
R5701:
Change to 63.2033C.1IL (20K 5% 1/20W 0201)

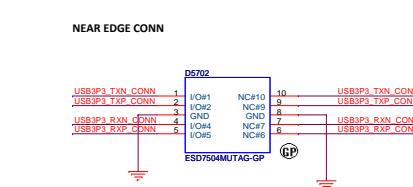
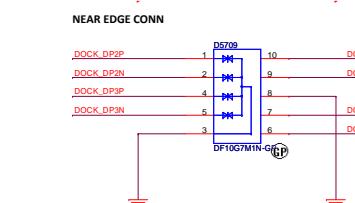
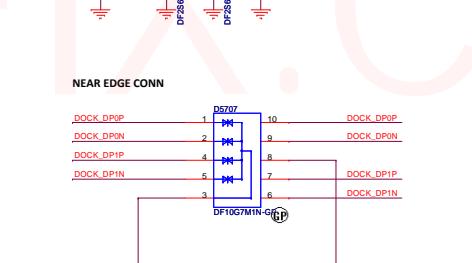
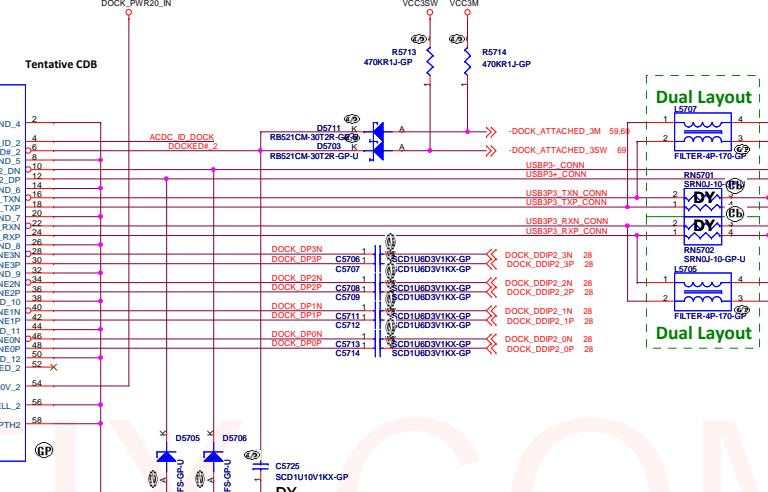
R5702 should be kept 1%

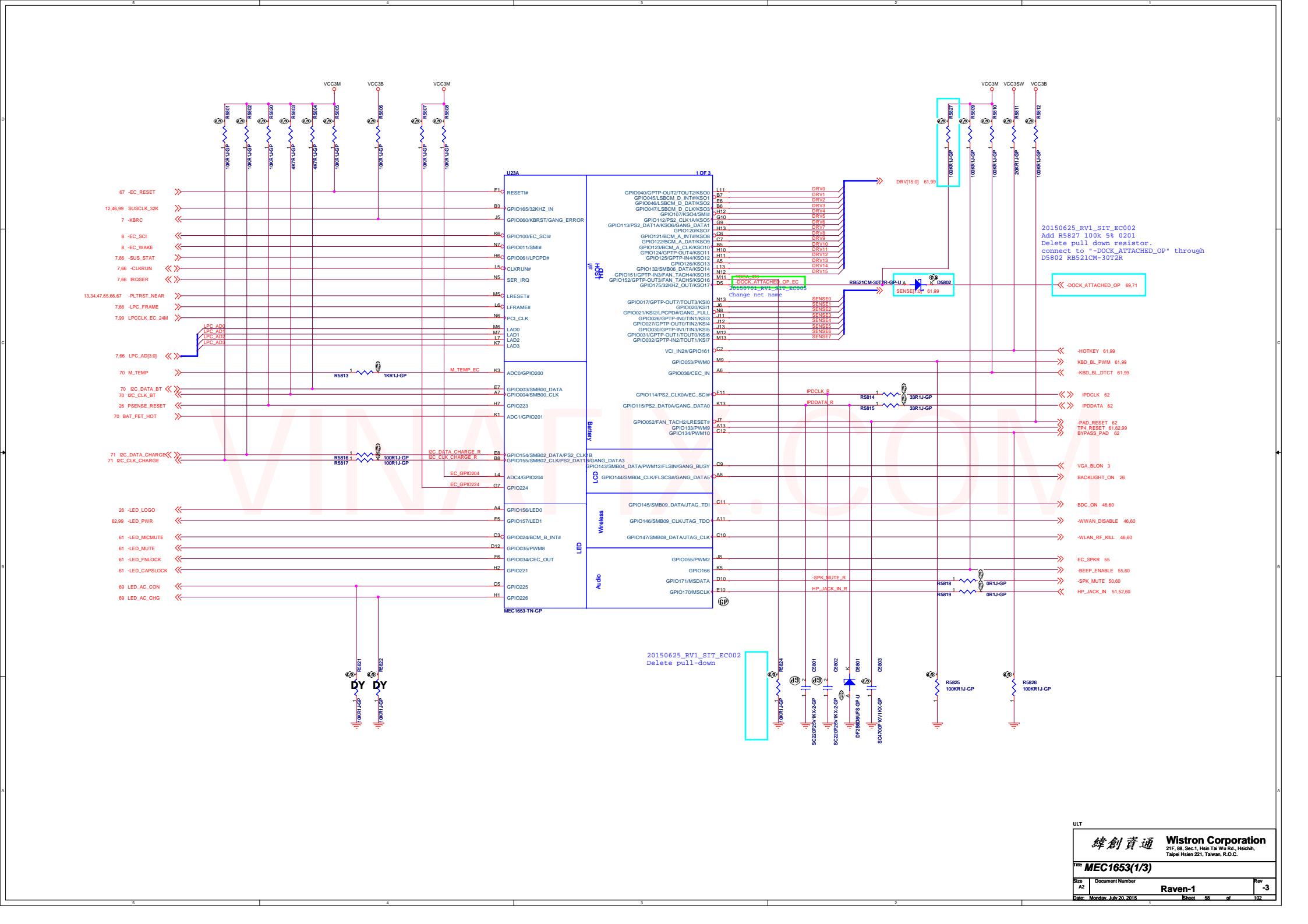
Design Target of max current on VCC5B_DOCK_FUSE

- 4A for pattern width
 - 1.5A for fuse selection



D287 / D244
TI TPD4EUSB30DQAF
Littelfuse SP3012-04





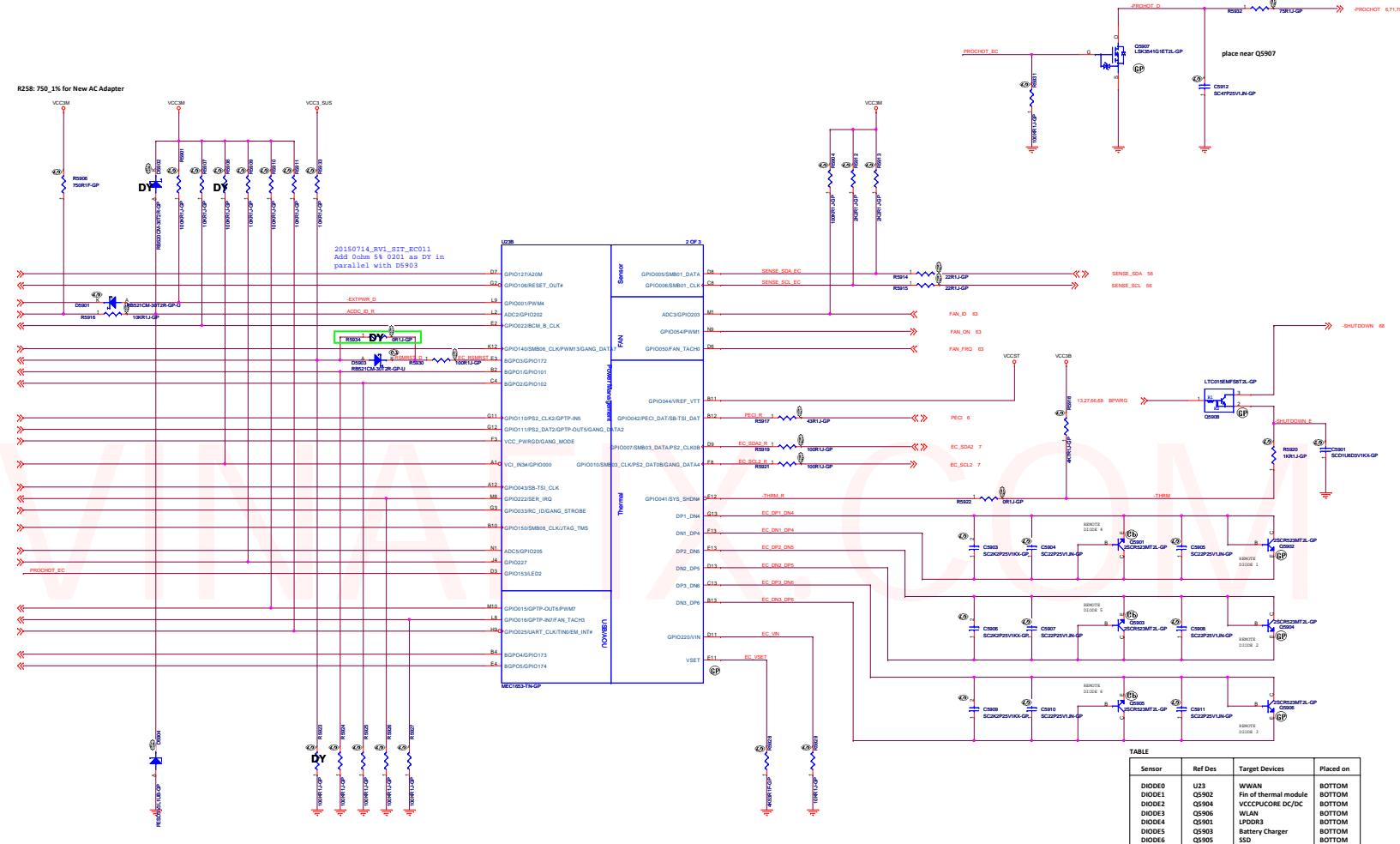
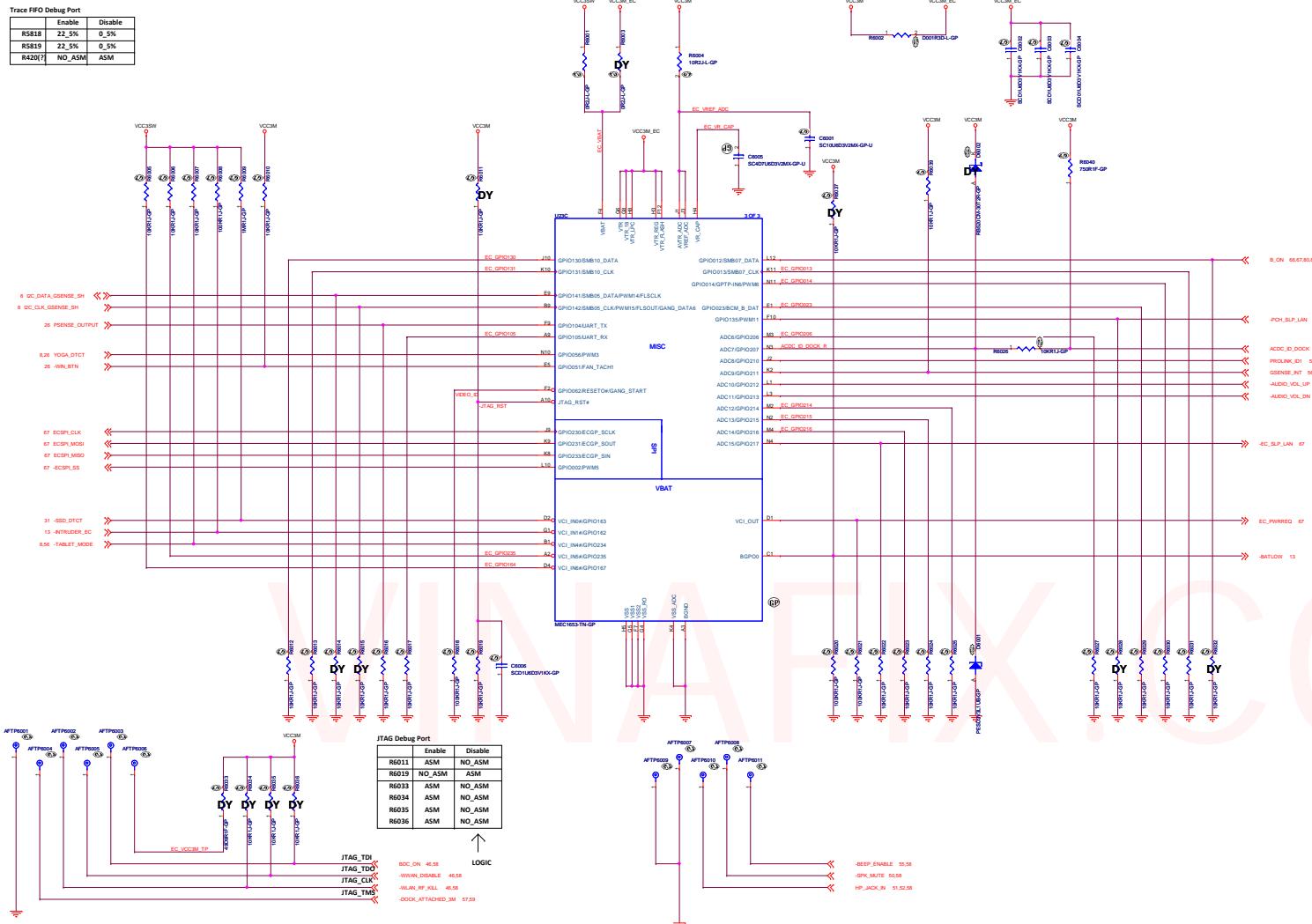
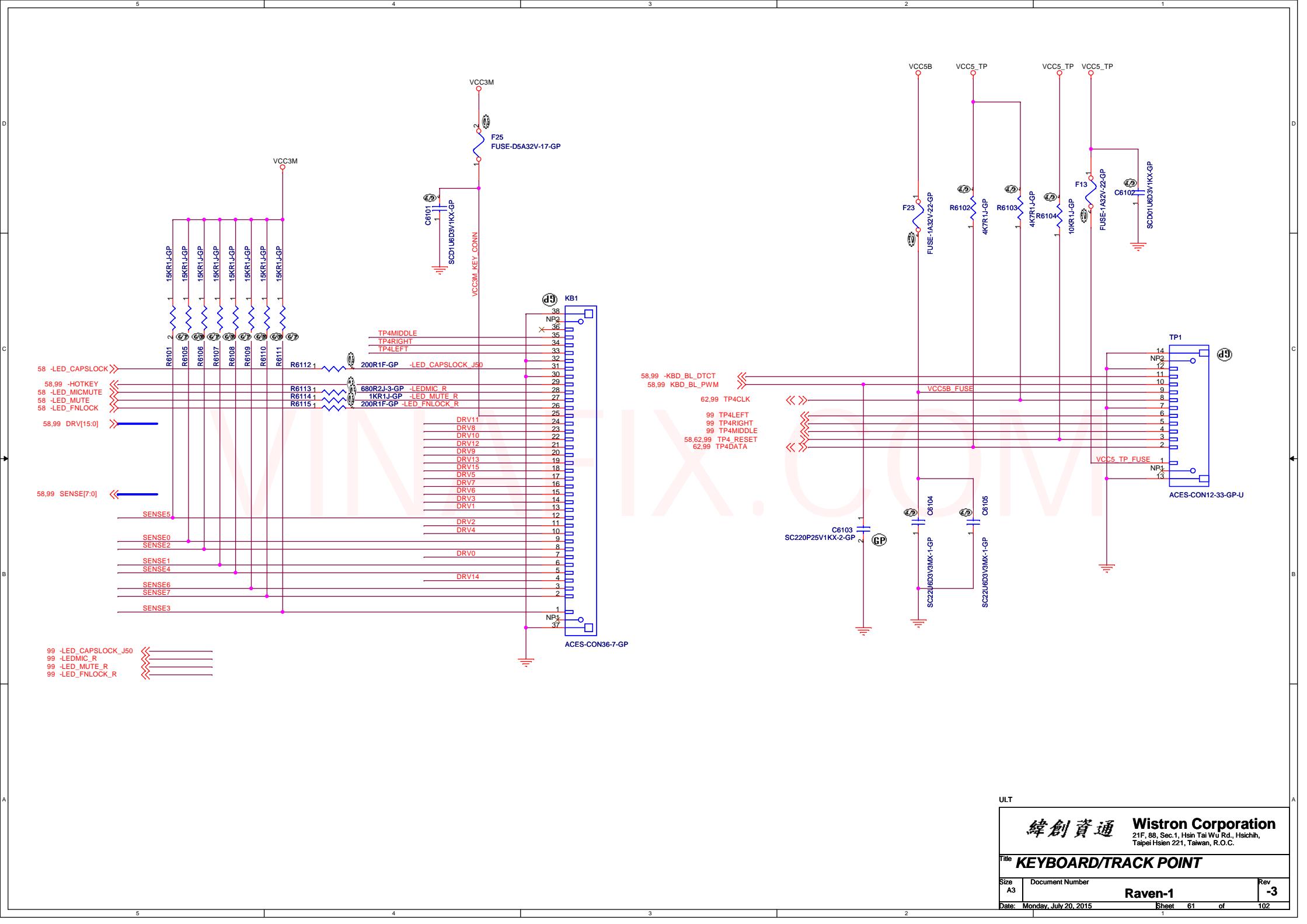
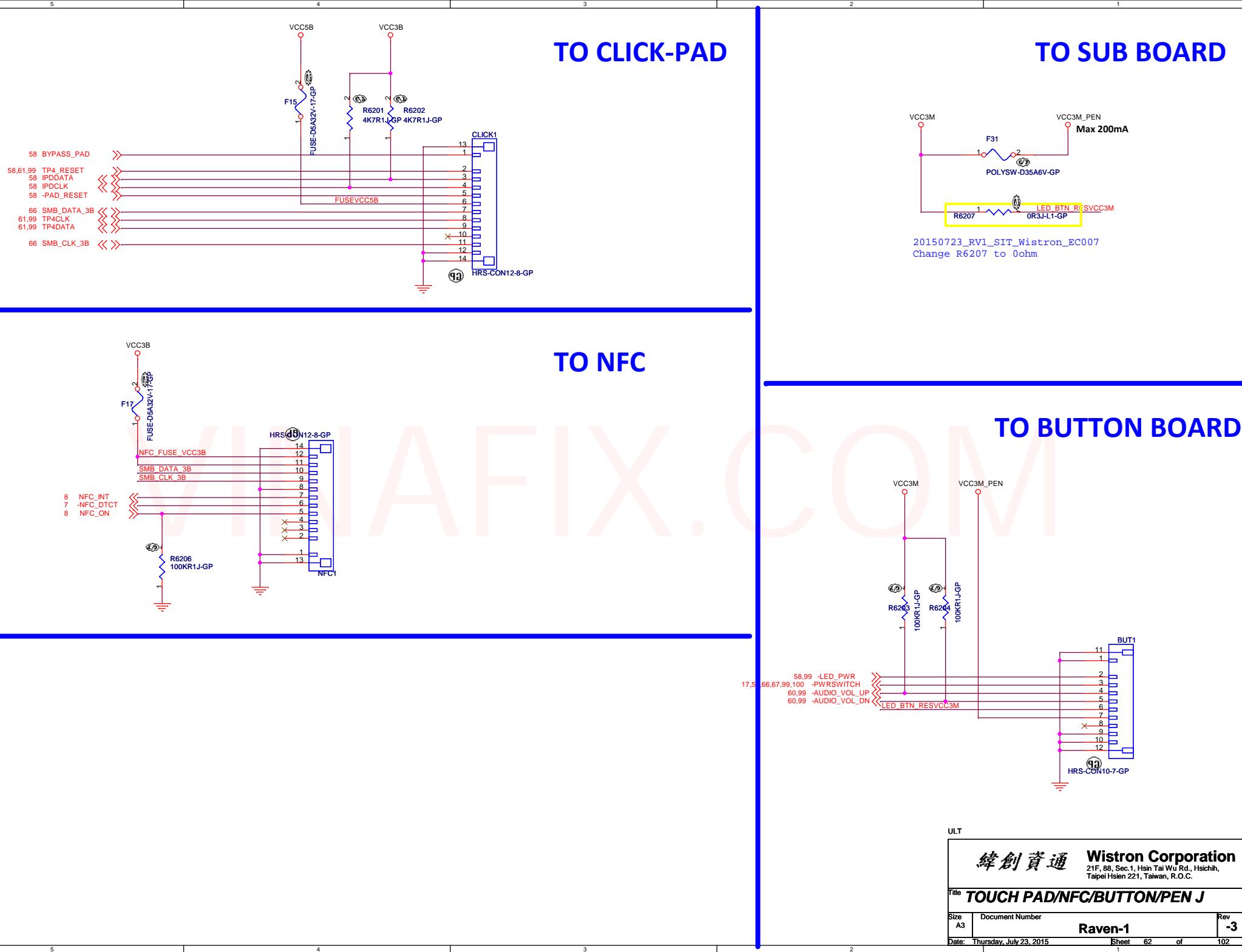


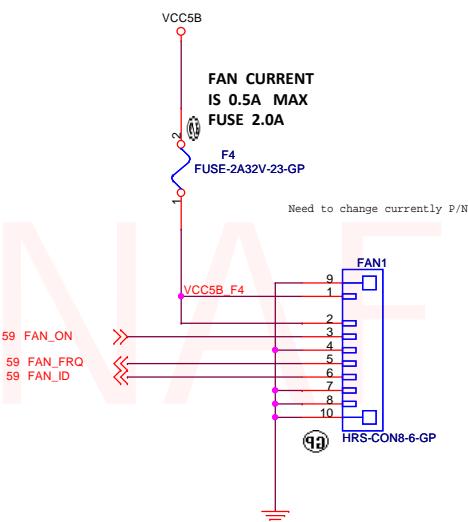
TABLE				
Sensor	Ref Des	Target Devices	Placed on	
DIODE9	U23	WWAN	BOTTOM	
DIODE1	Q5902	Fin of thermal module	BOTTOM	
DIODE2	Q5904	VCCPU/CORE DC/DC	BOTTOM	
DIODE3	Q5906	BT	BOTTOM	
DIODE4	Q5901	SSD	BOTTOM	
DIODE5	Q5903	Battery Charger	BOTTOM	
DIODE6	Q5905	SSD	BOTTOM	

Trace FIFO Debug Port		
	Enable	Disable
R5818	22_5%	0_5%
R5819	22_5%	0_5%
R420(?)	NO_ASM	ASM









PIN# NET NAME

PIN1	VCC5B_F4
PIN2	(OPEN)
PIN3	FAN_ON
PIN4	GND
PIN5	FAN_FRQ
PIN6	FAN_ID
PIN7	GND
PIN8	GND

FAN ID		Inside of Thermal Module
HIGH	Secondary Source	Open
LOW	Primary Source	Tie down to GND

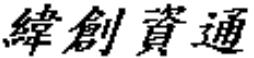
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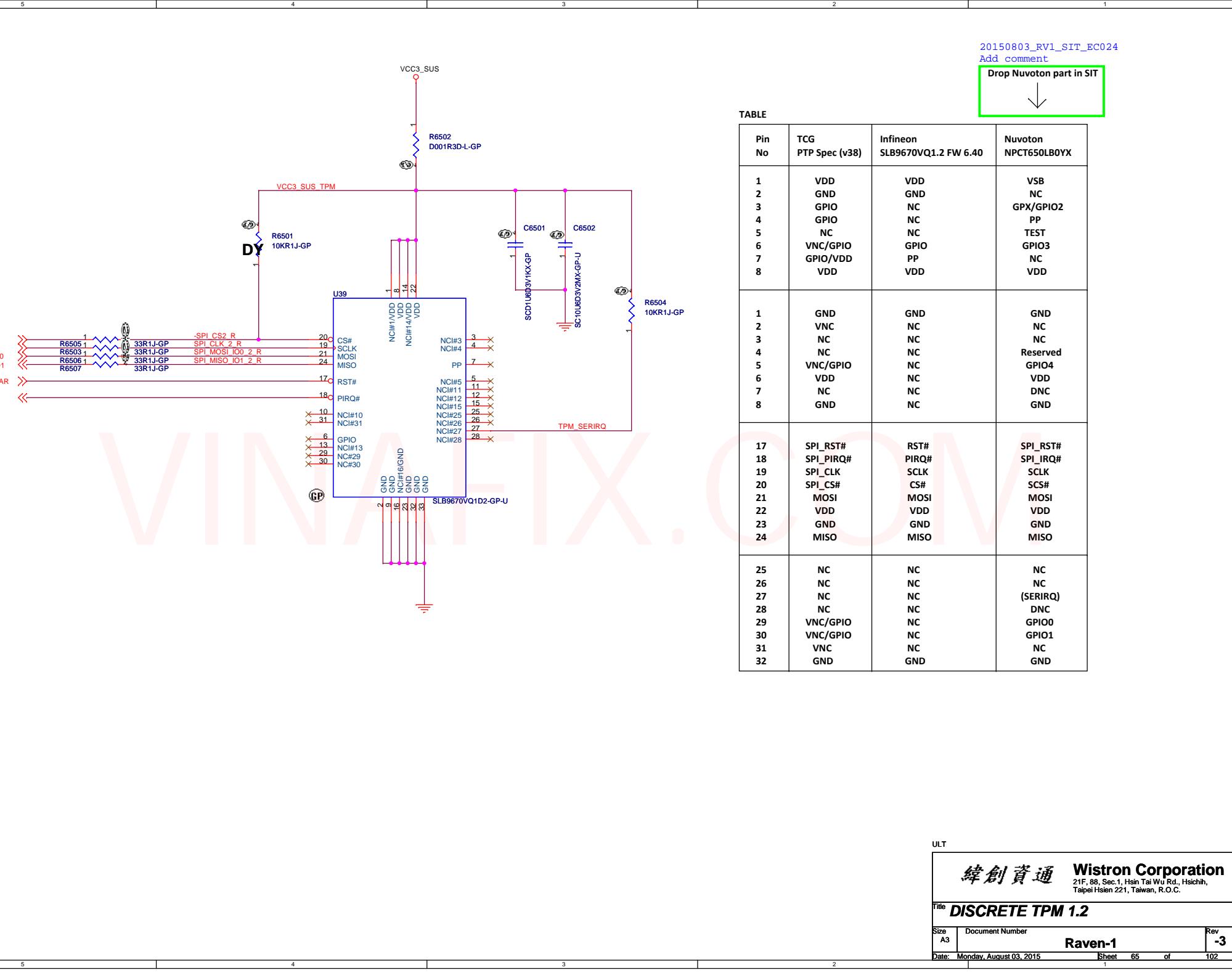
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title FAN CONNECTOR	
Size A3	Document Number
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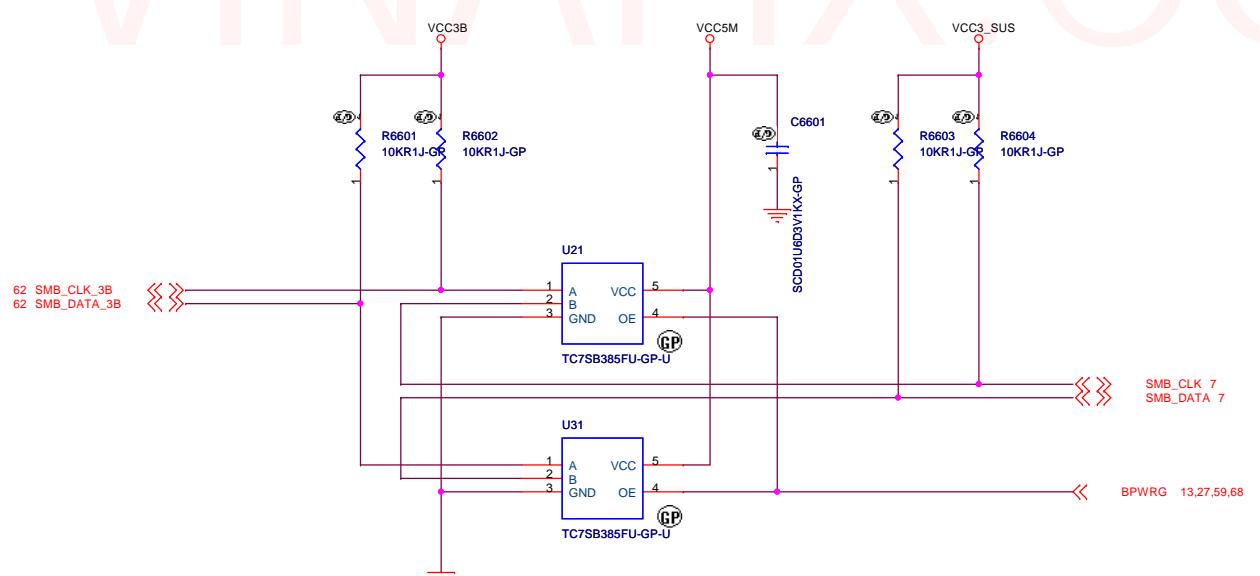
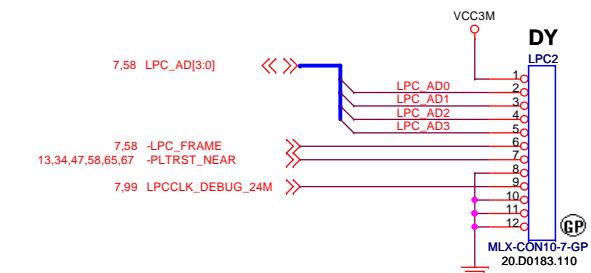
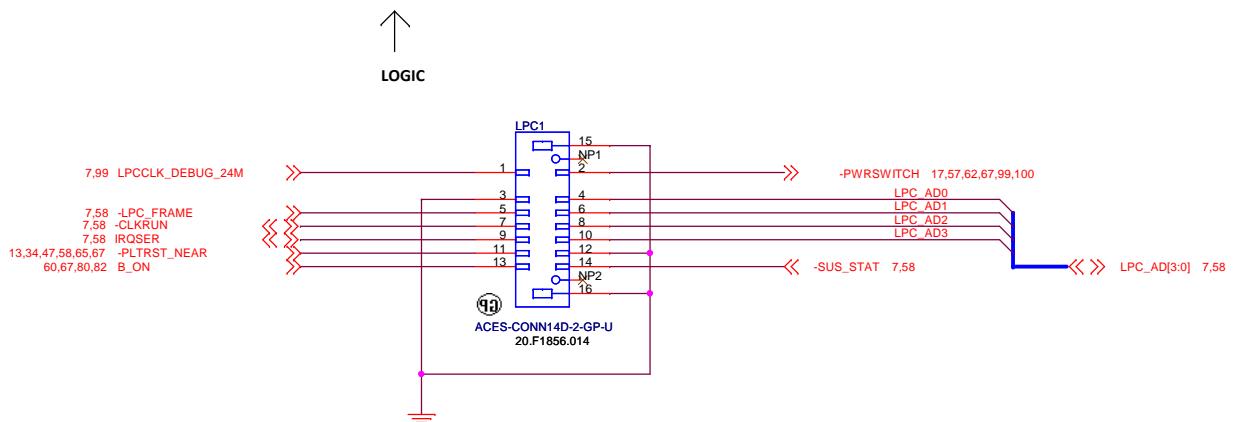
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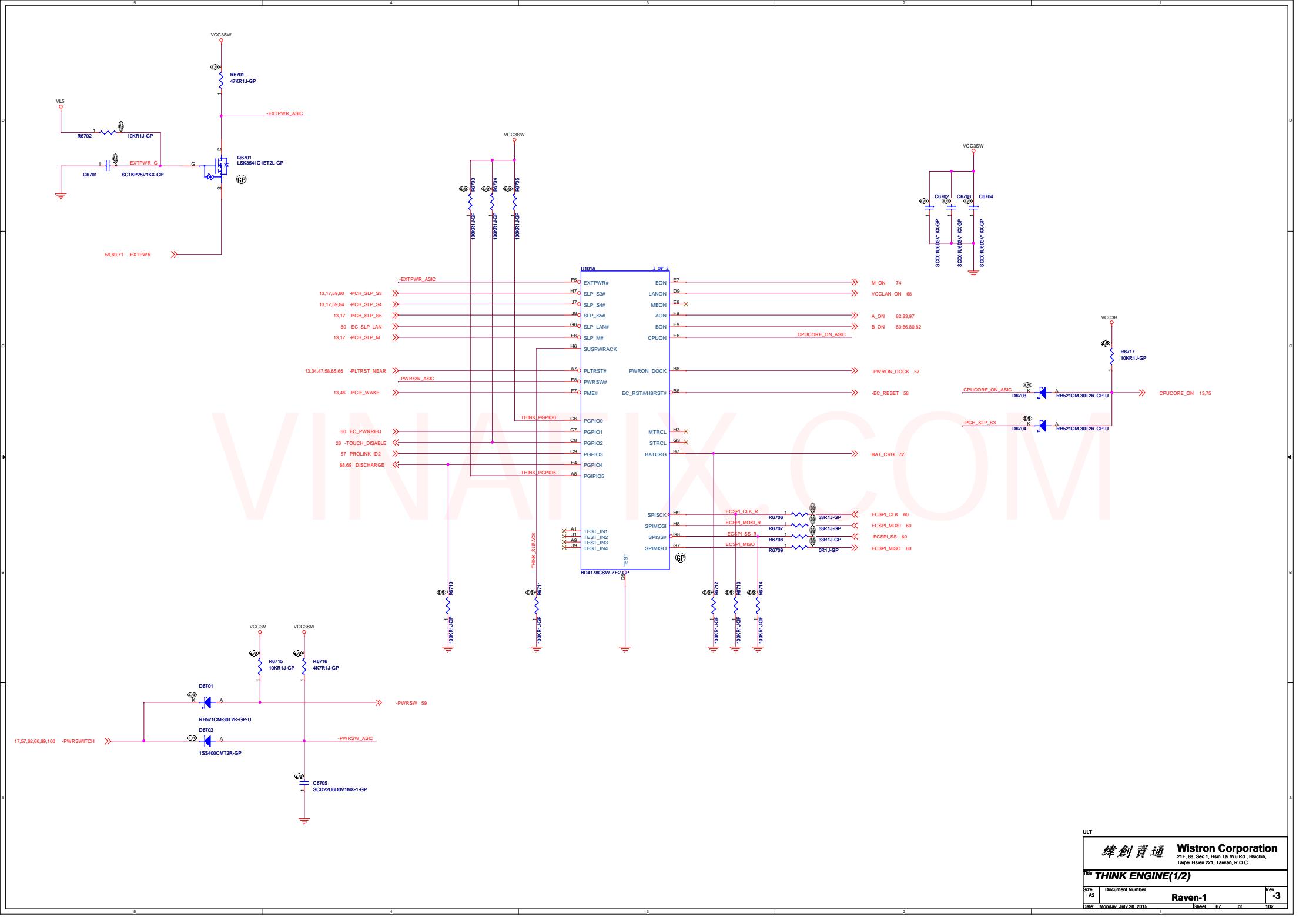


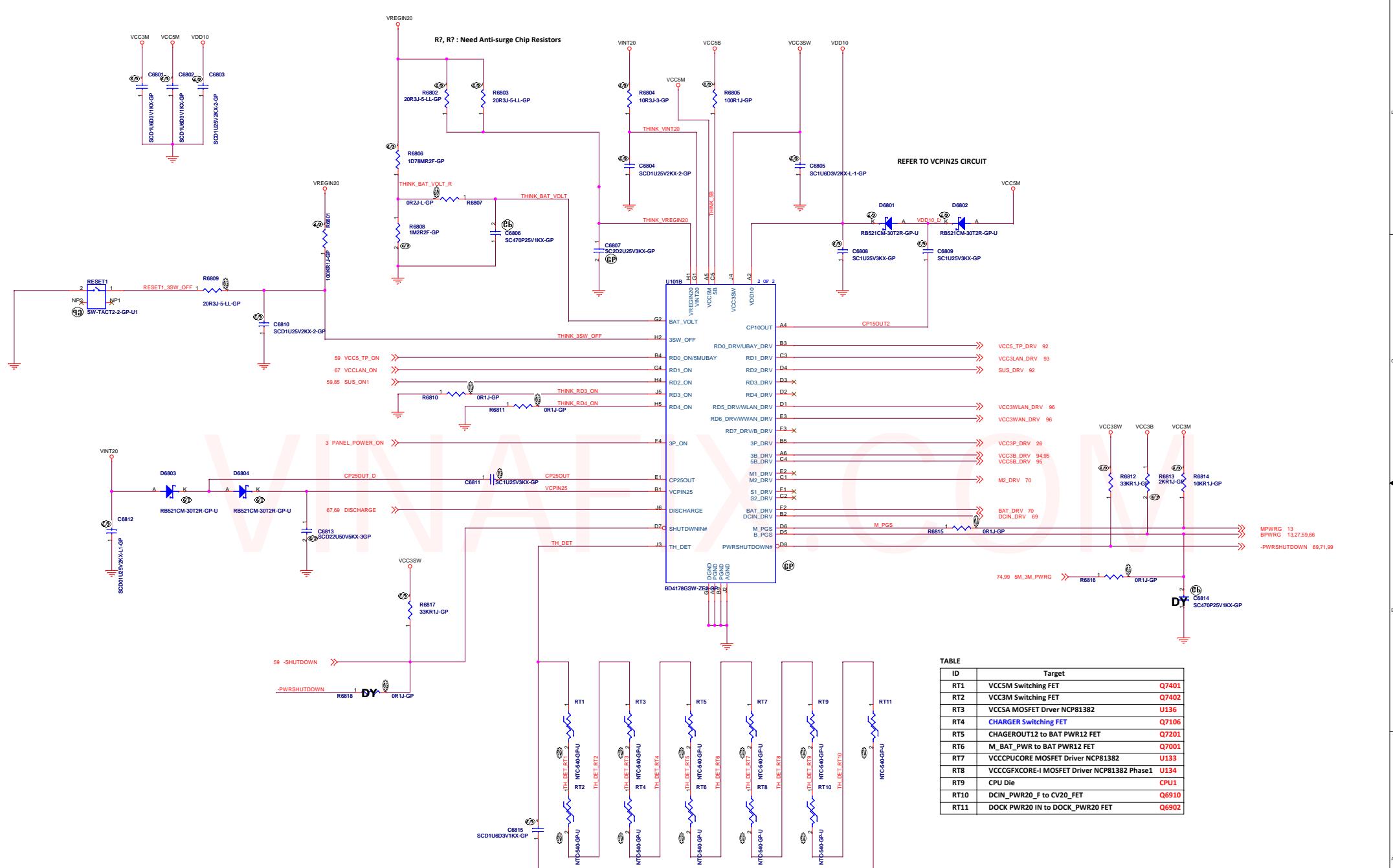
TABLE

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R?	ASM	NO_ASM

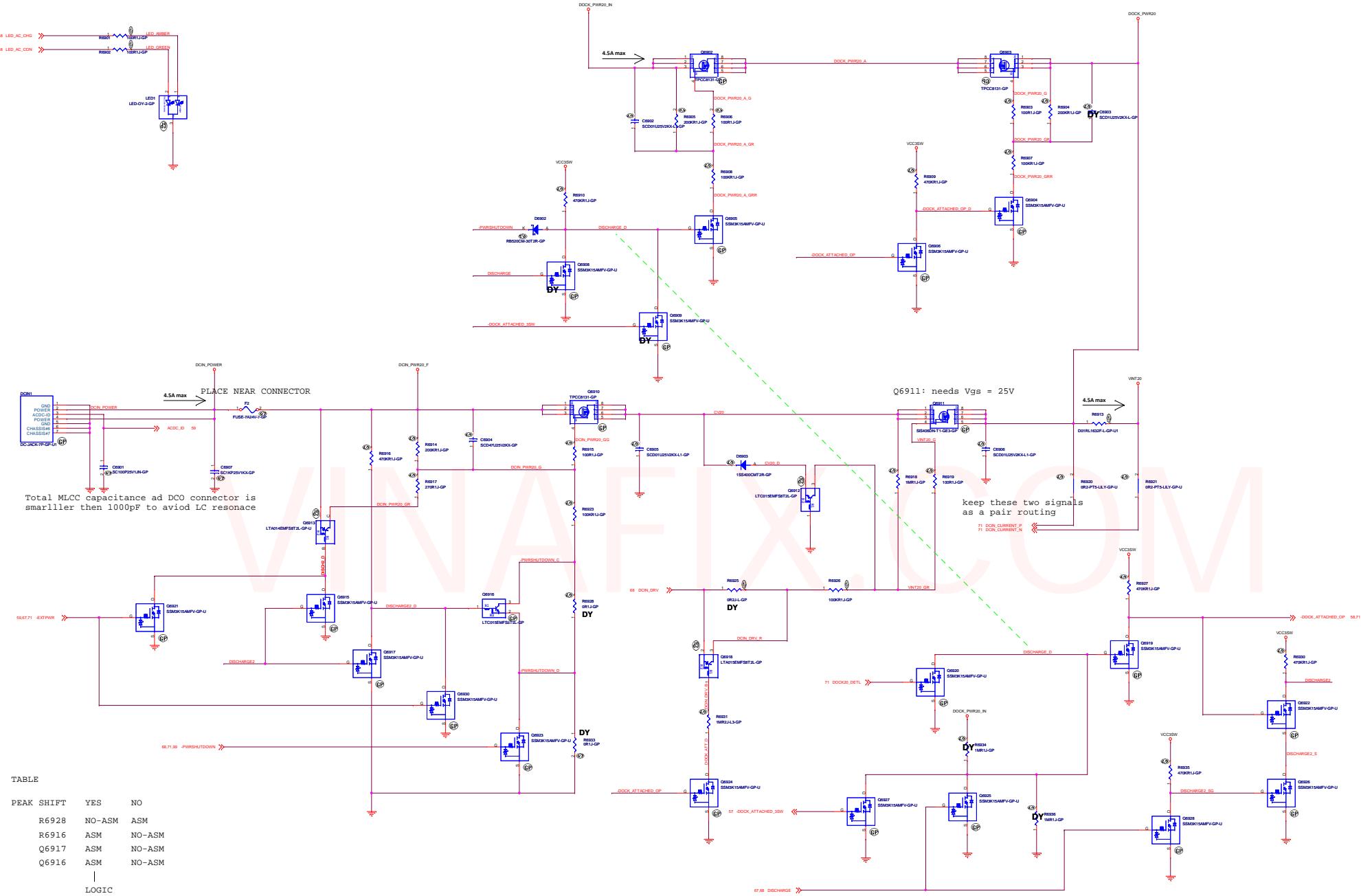
LPC for Debug Card Connector

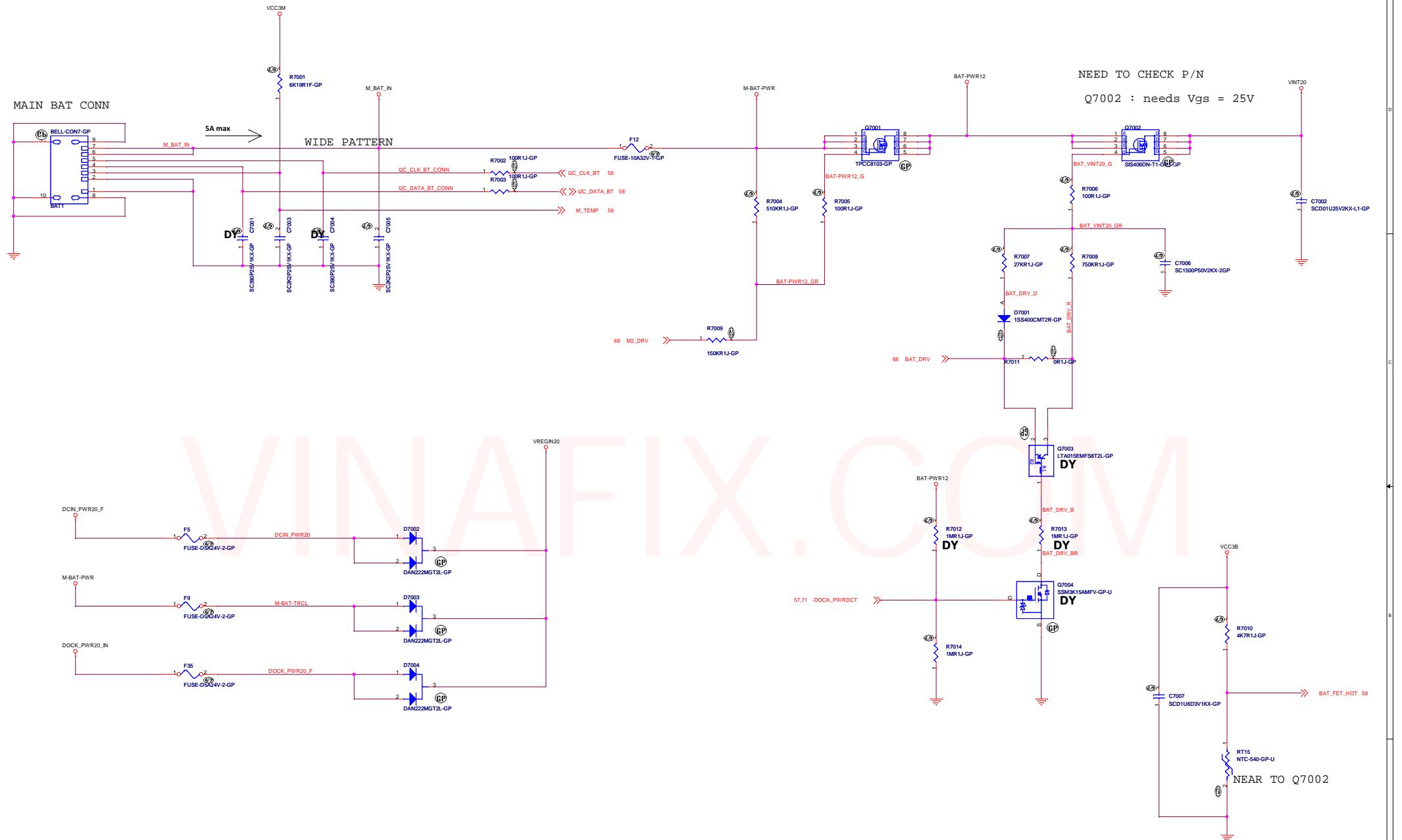


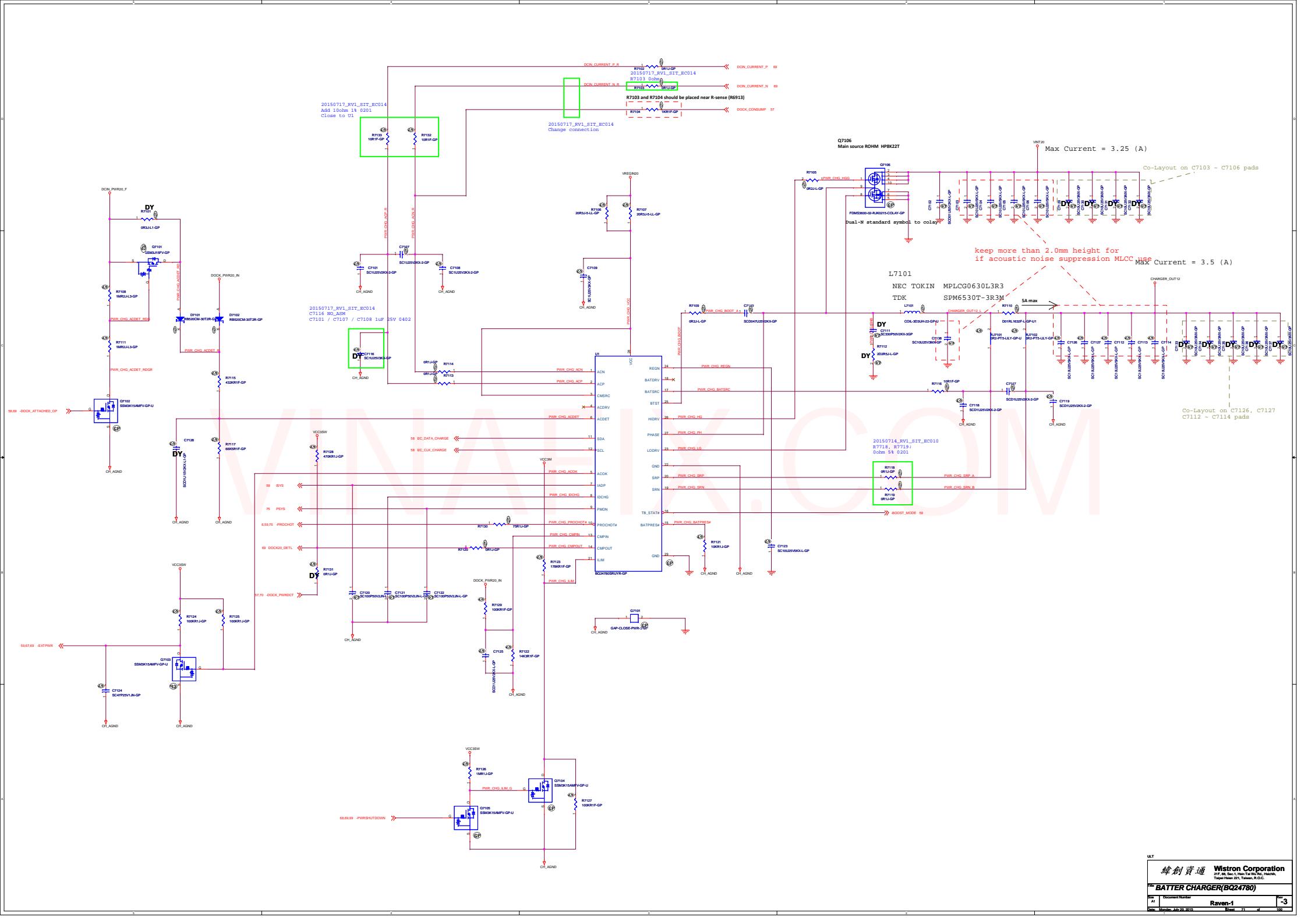


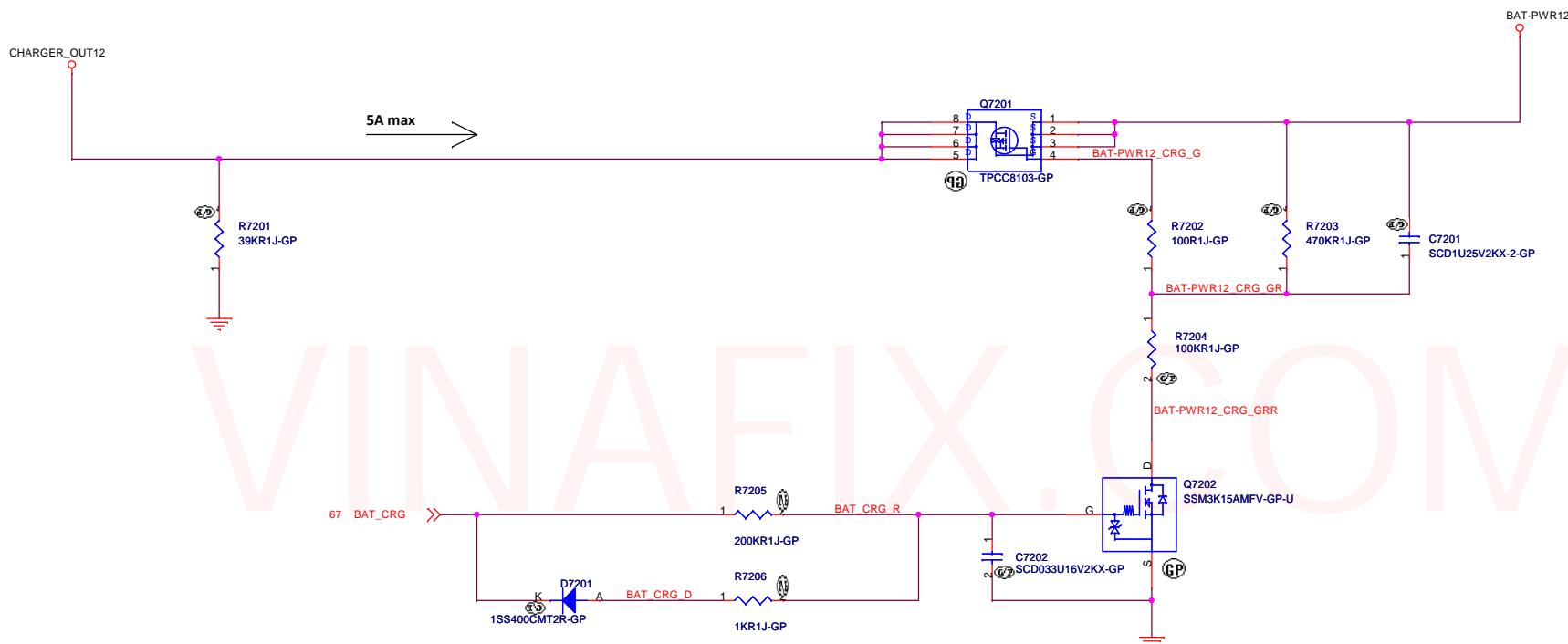


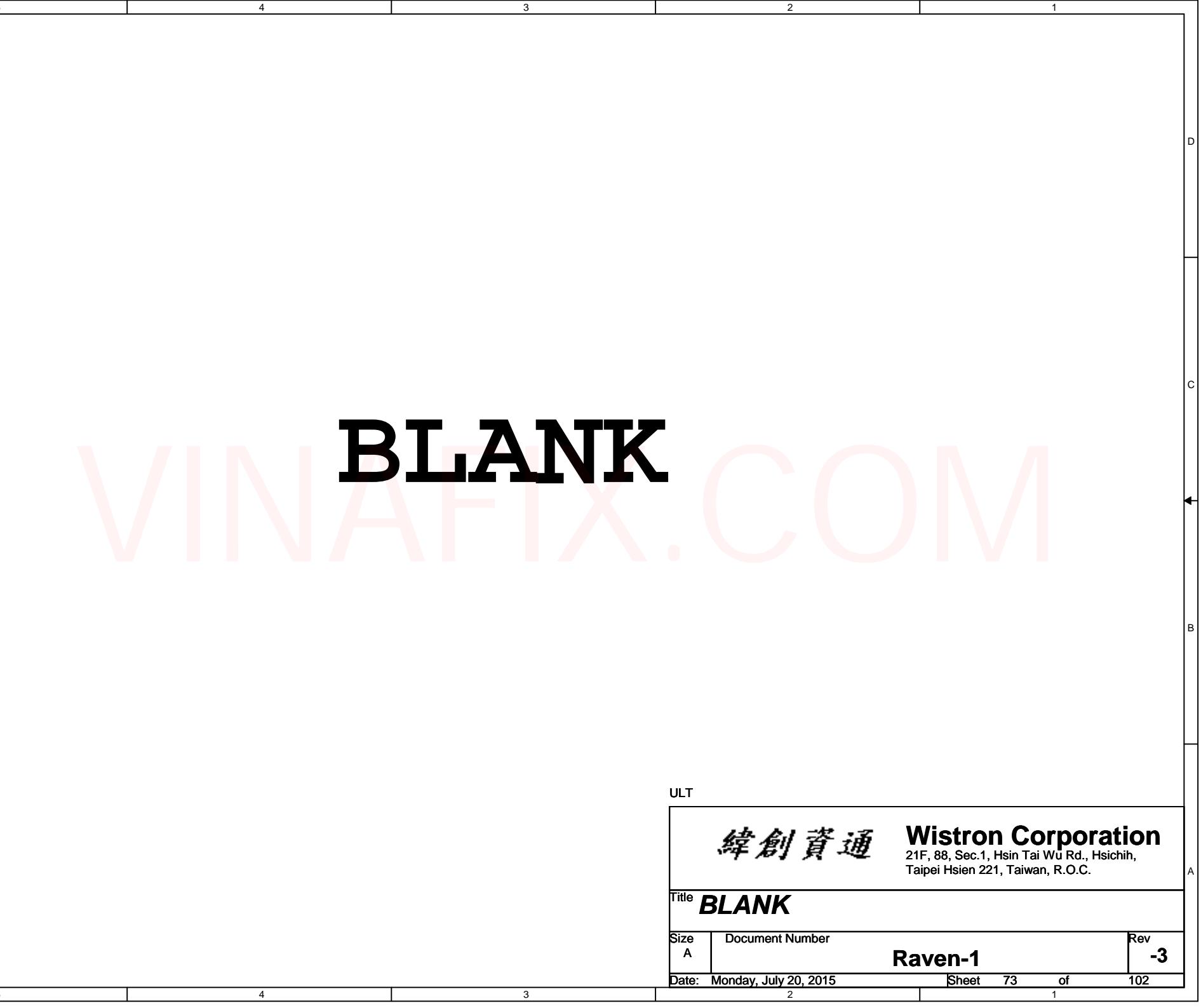
ID	Target
RT1	VCC5M Switching FET
RT2	VCC3M Switching FET
RT3	VCCSA MOSFET Driver NCP81382
RT4	CHARGER Switching FET
RT5	CHAGEROUT12 to BAT PWR12 FET
RT6	M_BAT_PWR to BAT PWR12 FET
RT7	VCCCPUCOM MOSFET Driver NCP81382
RT8	VCCCGFXCORE-I MOSFET Driver NCP81382 Phase1
RT9	CPU Die
RT10	DCIN_PWR20_F to CV20_FET
RT11	DOCK PWR20 IN to DOCK_PWR20 FET

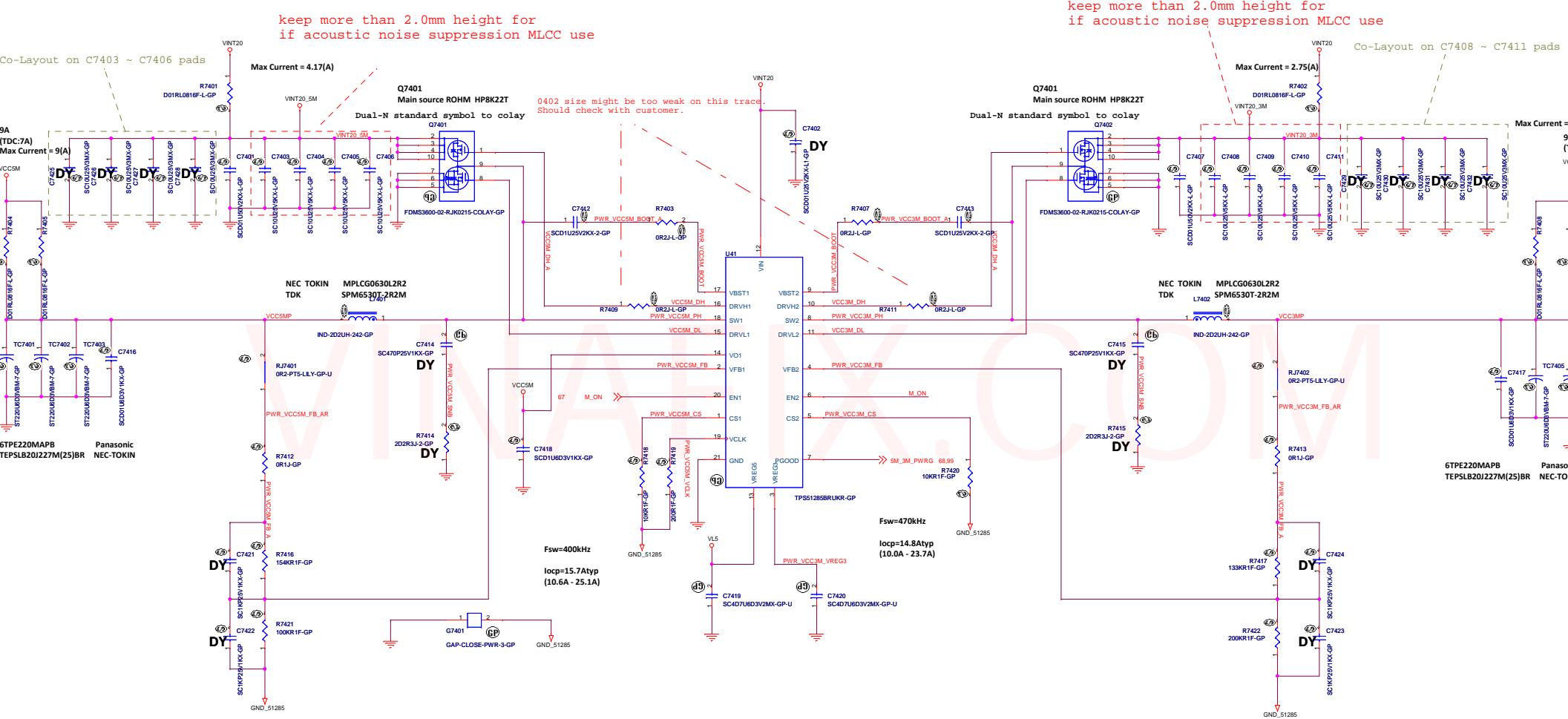


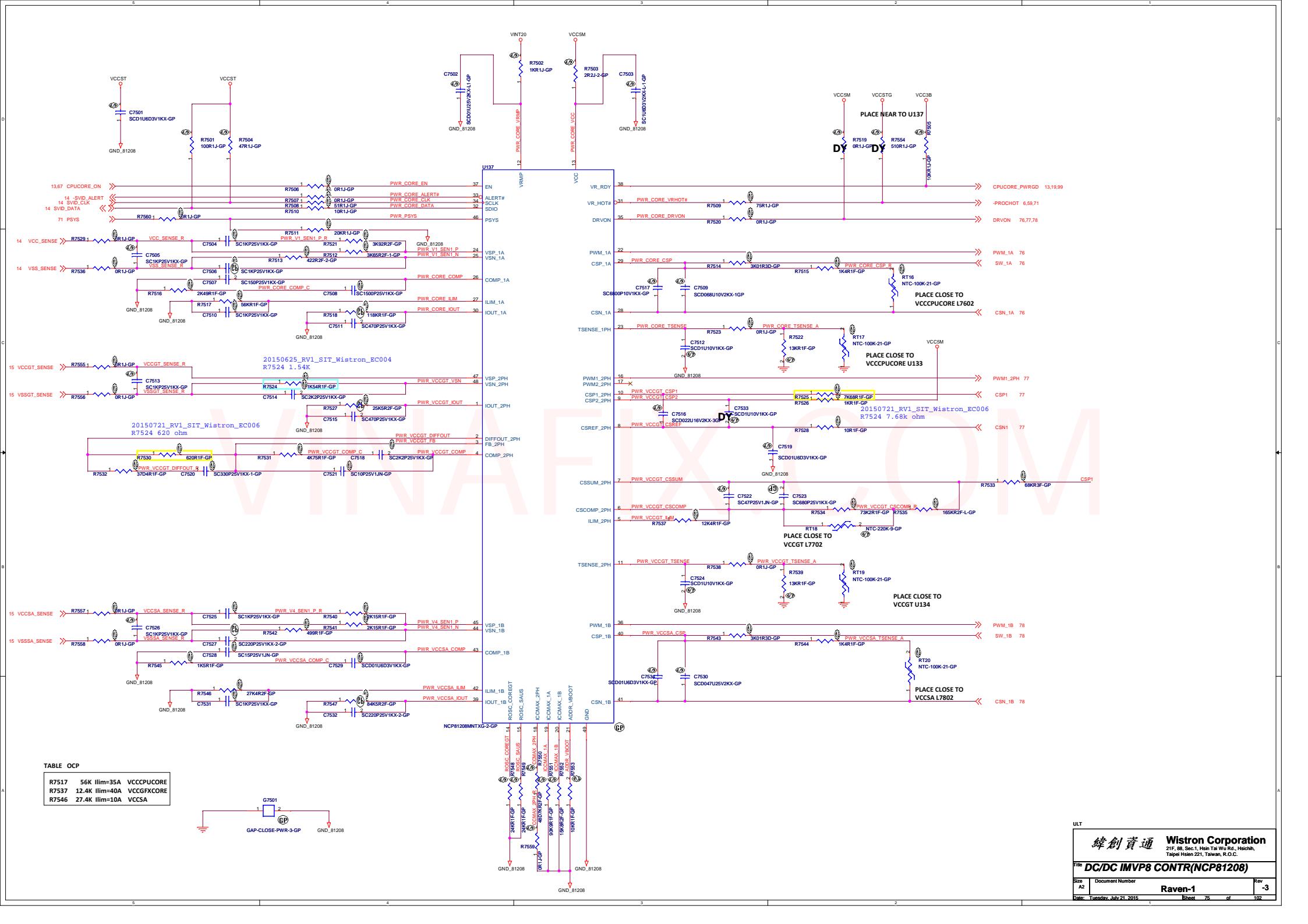






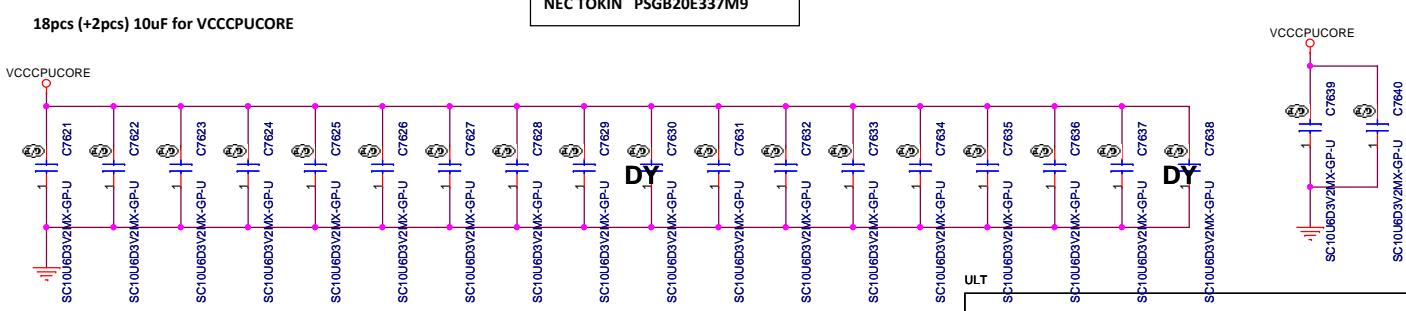
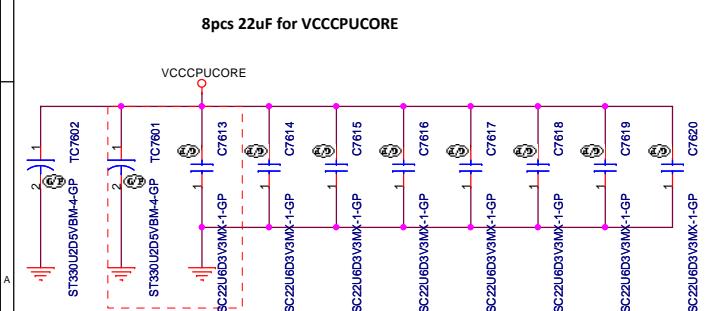
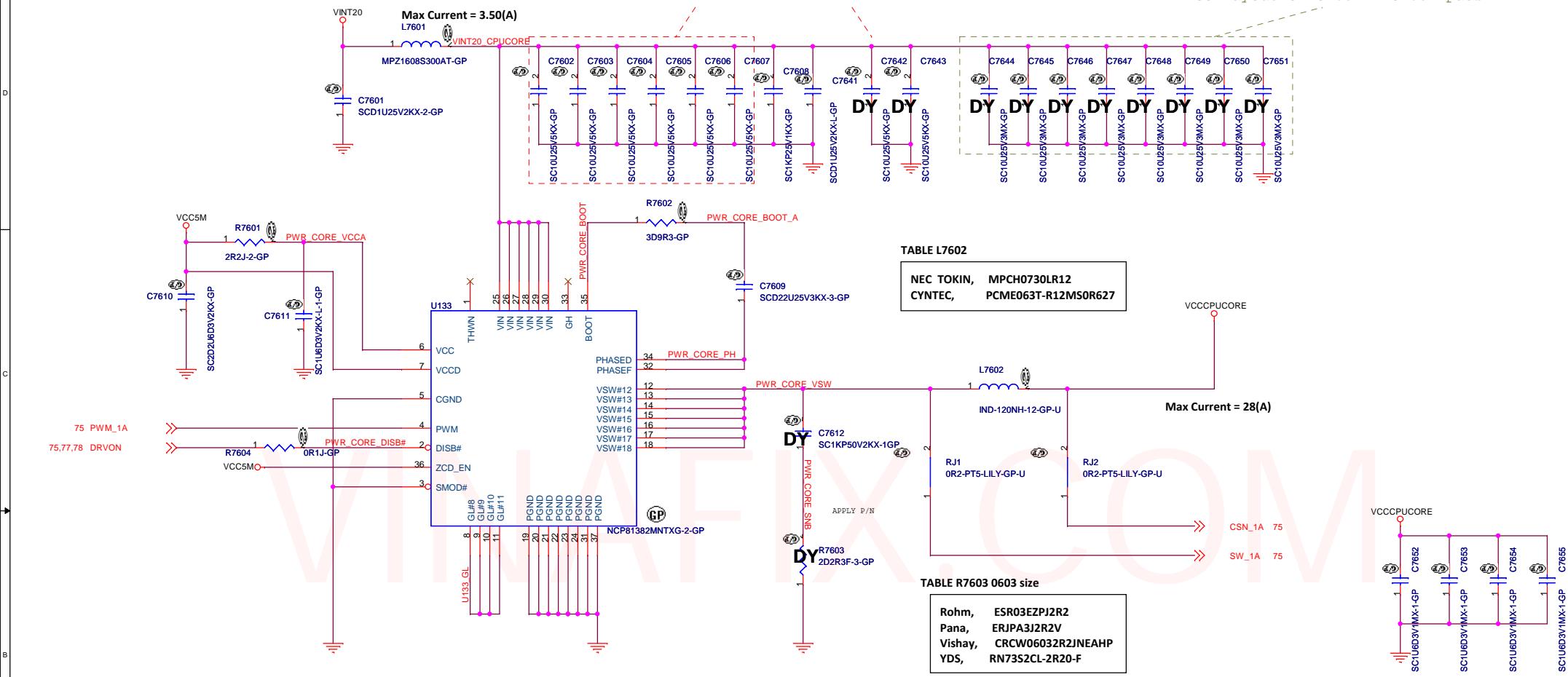






keep more than 2.0mm height for
if acoustic noise suppression MLCC use

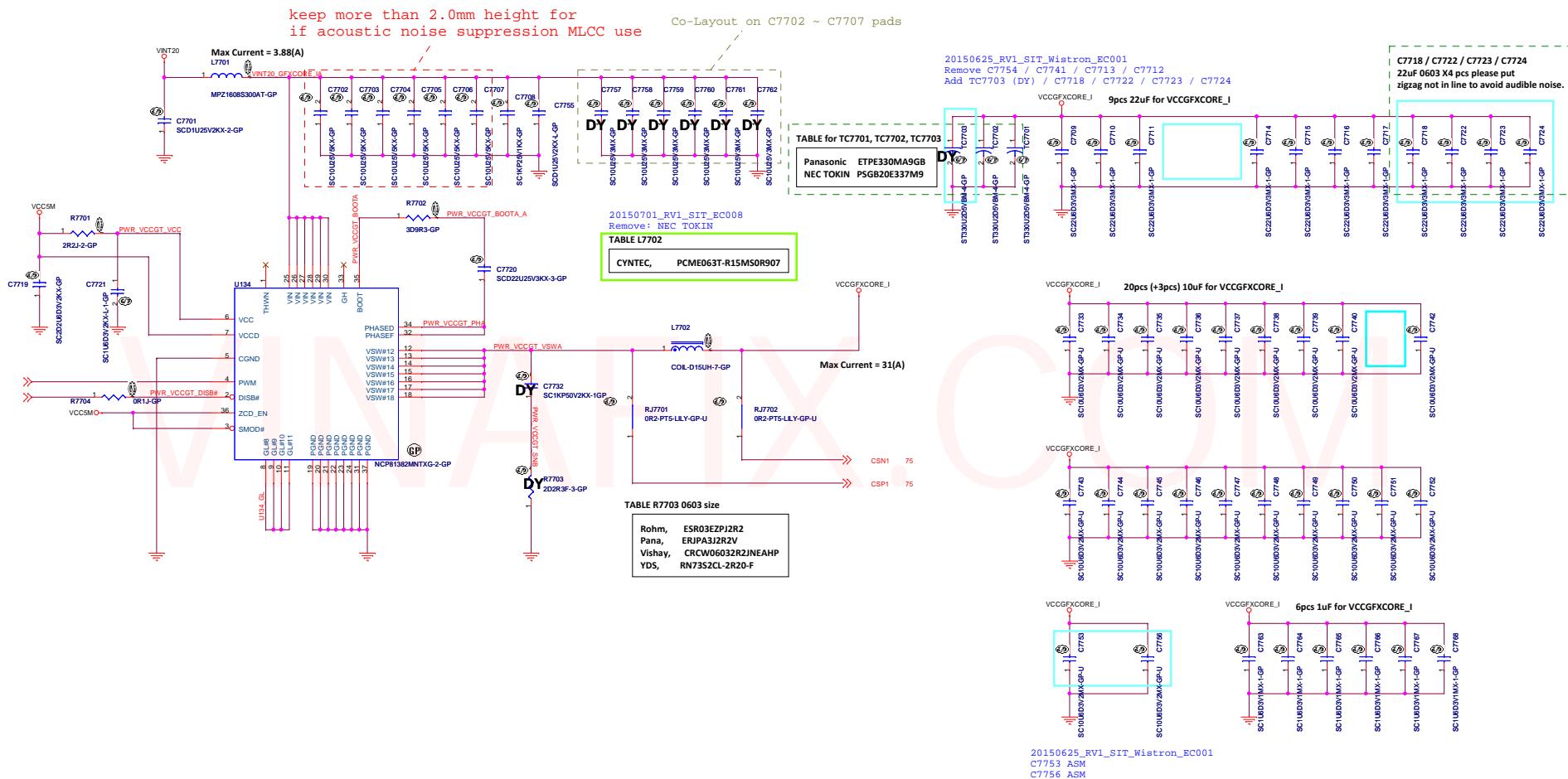
Co-Layout on C7602 ~ C7607 pads



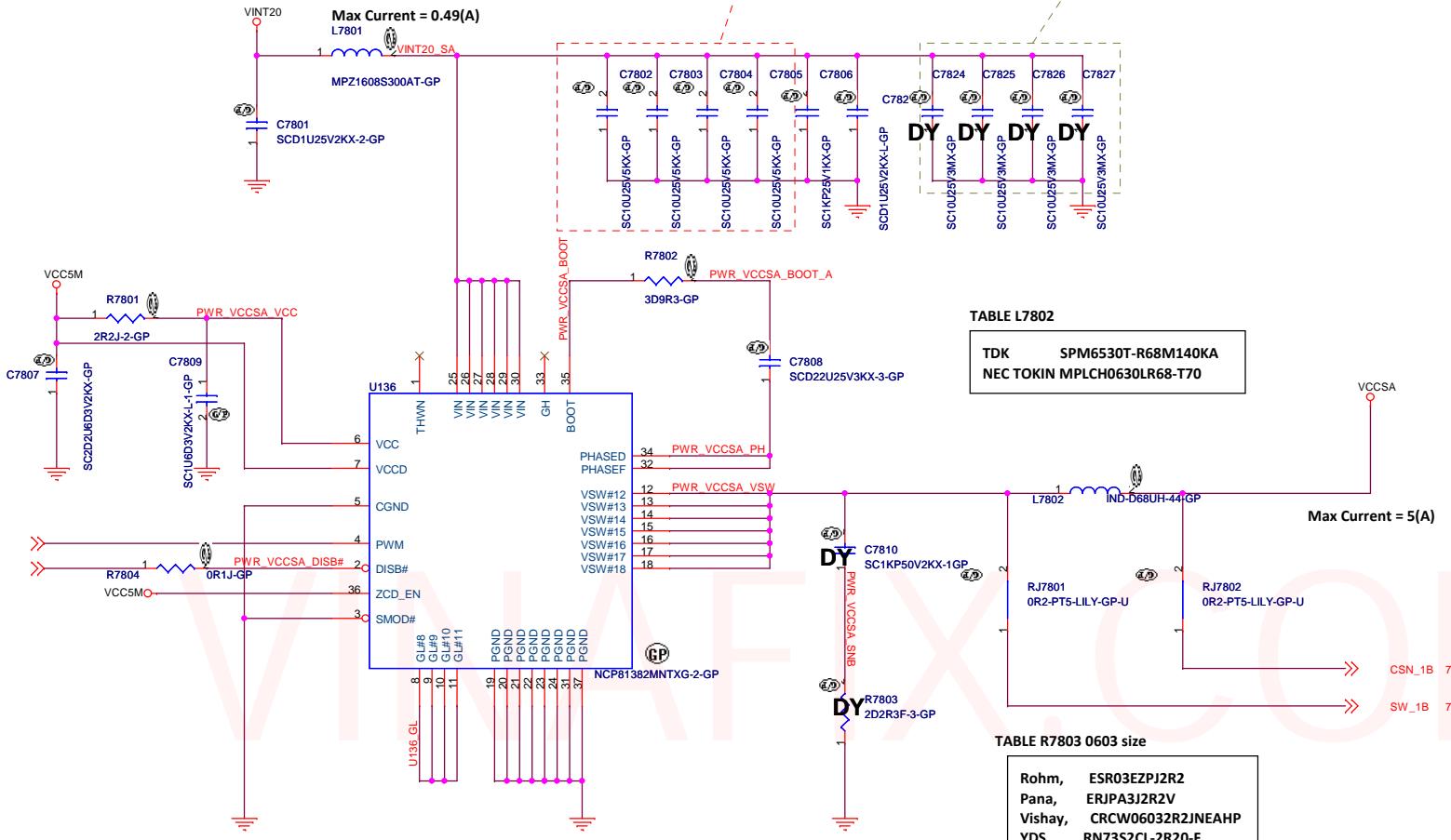
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Taipei Hsien 221, Taiwan, R.O.C.

Title **DC/DC VCCCPUCORE(NCP81382)**

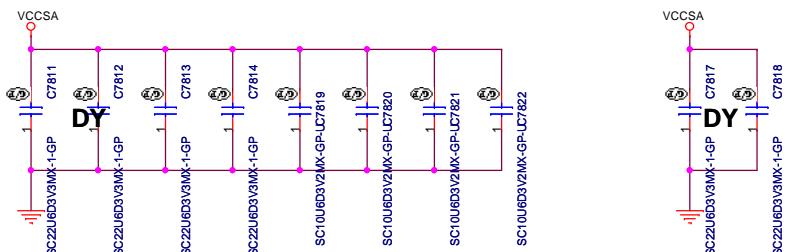
Size A3	Document Number	Rev -3
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keep more than 2.0mm height for Co-Layout on C7802 ~ C7805 pads
if acoustic noise suppression MLCC use



4pcs (+2pcs) 22uF and 4pcs 10uF for VCCSA



D

D

C

C

B

B

A

A

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Title **BLANK**

Size A Document Number

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-3

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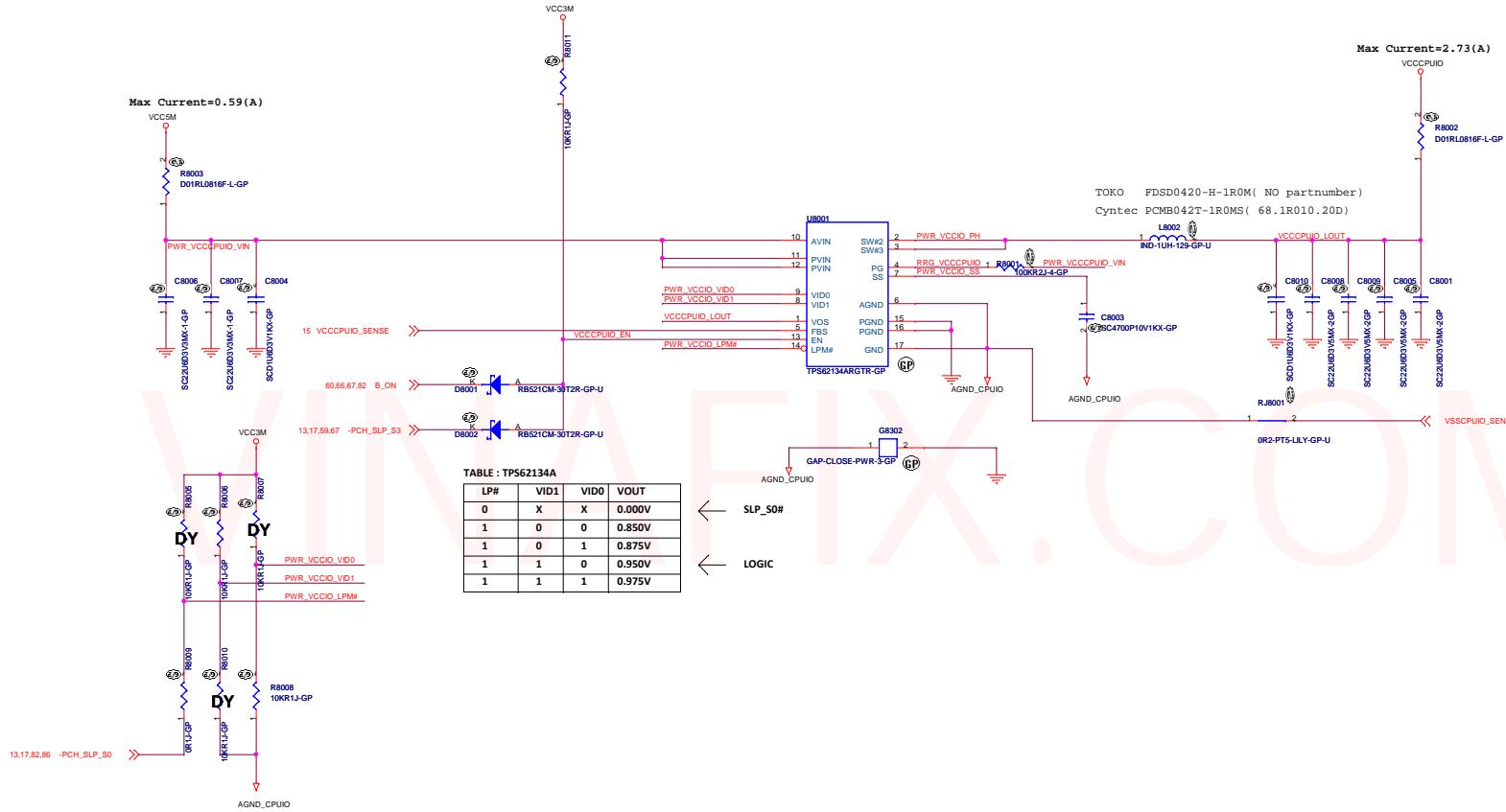
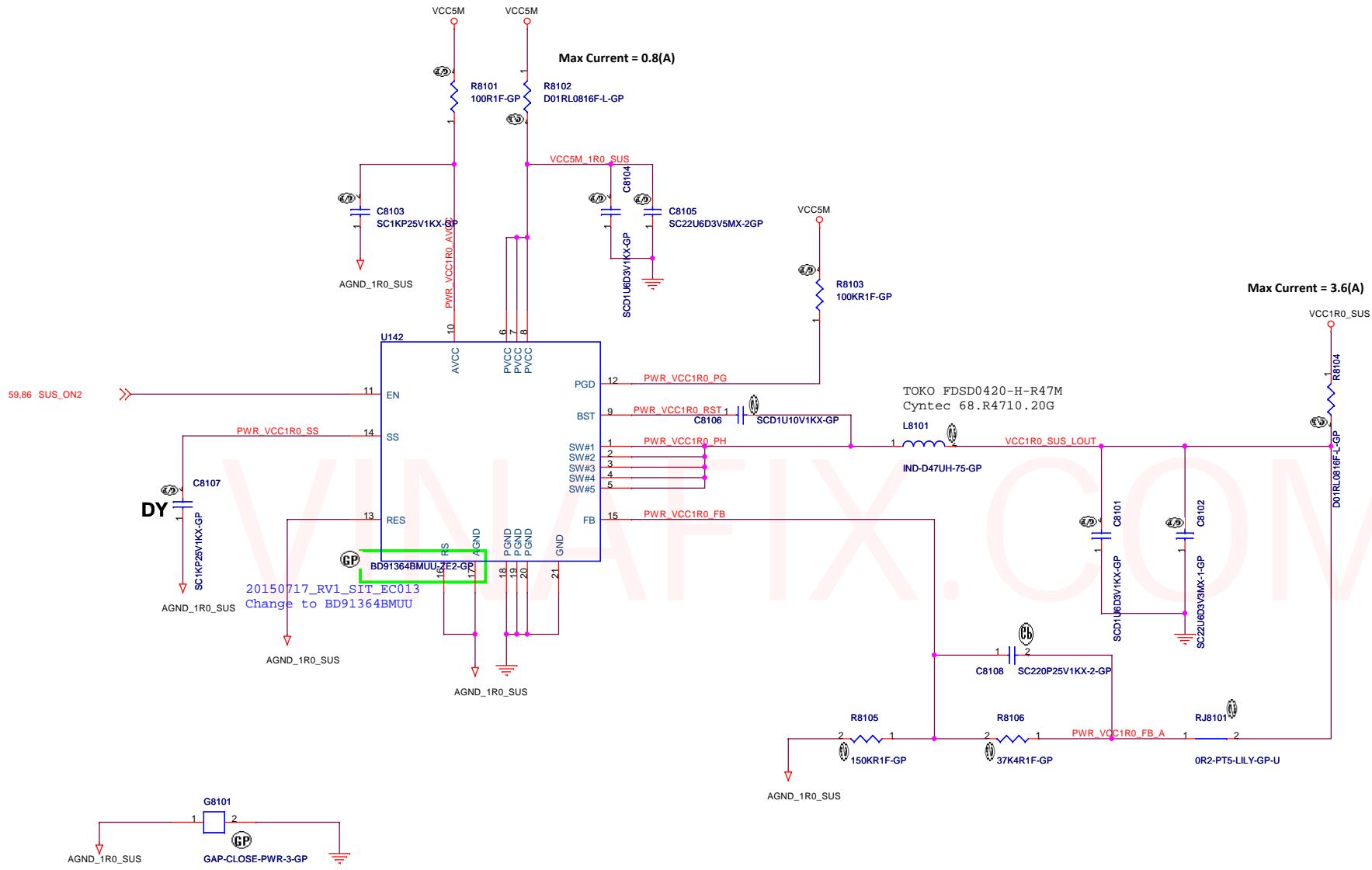
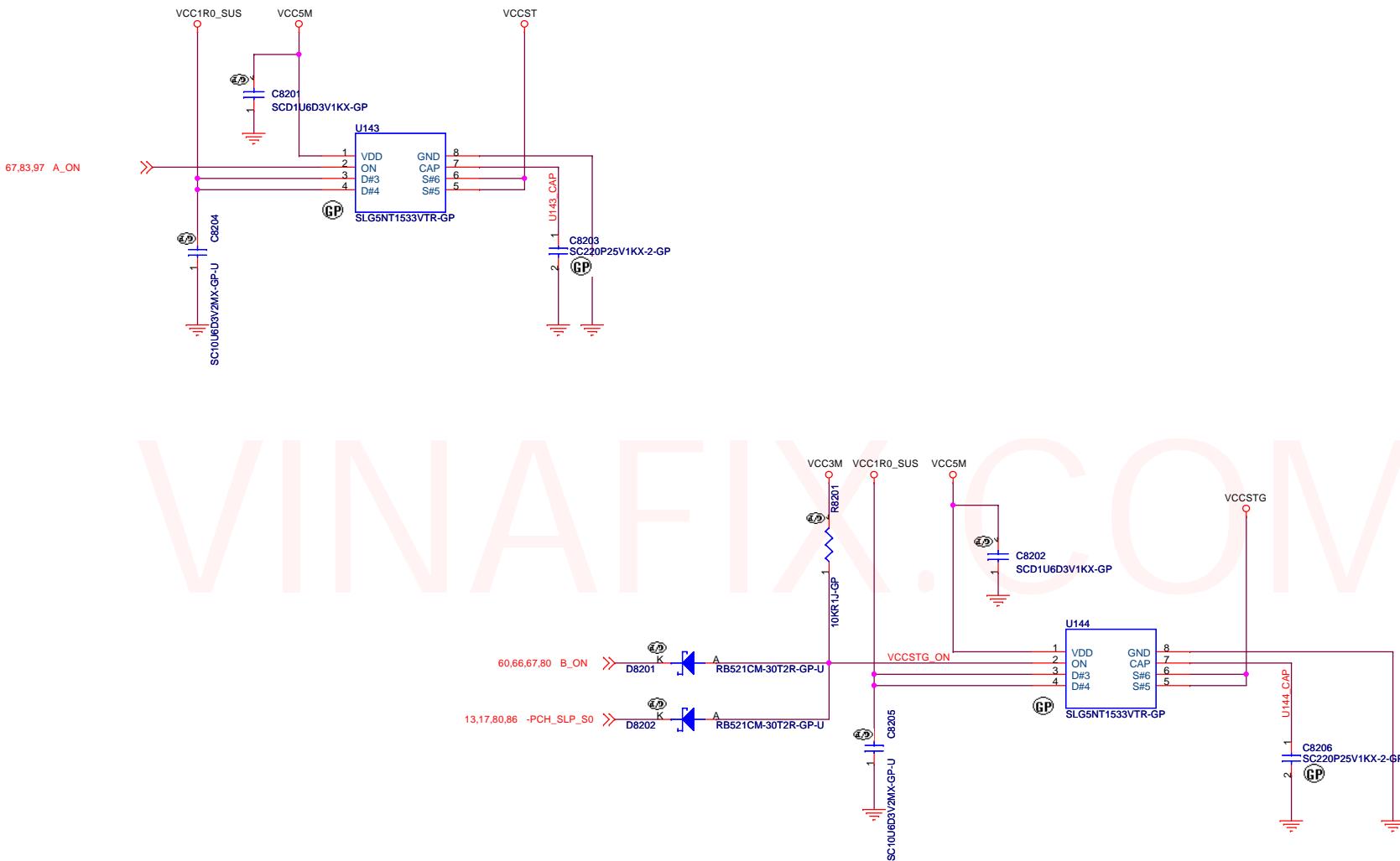


TABLE : TPS62134A			
LP#	VID1	VID0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V





JLT

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

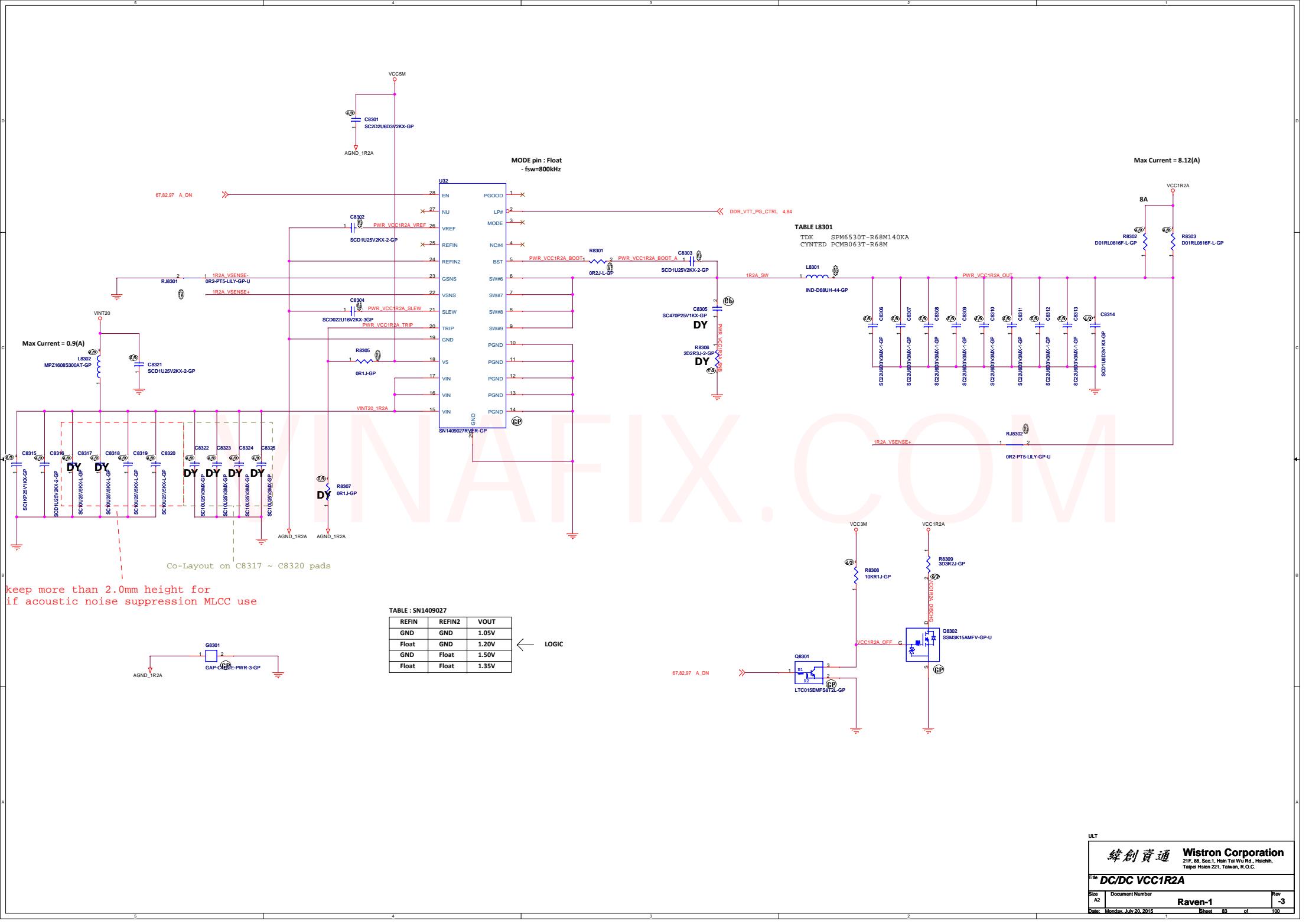
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title LOAD SW VCGST & VCGSTG

Size Document Number Rev

A3 Raven-1 -3

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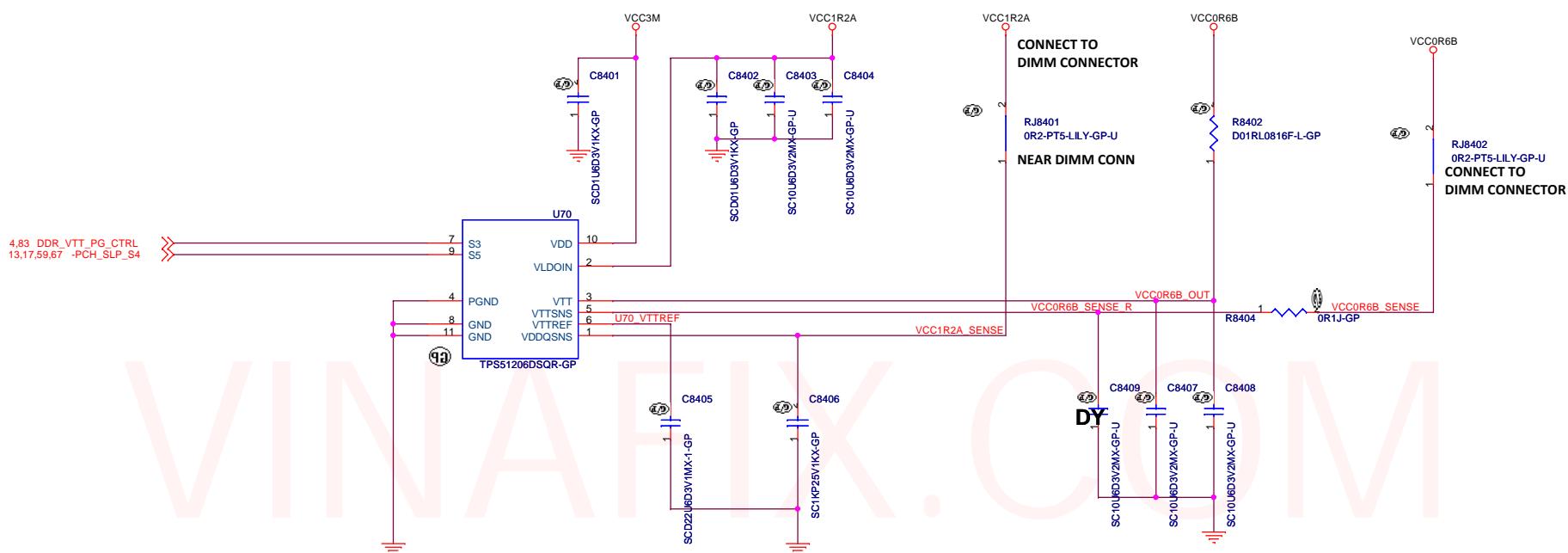
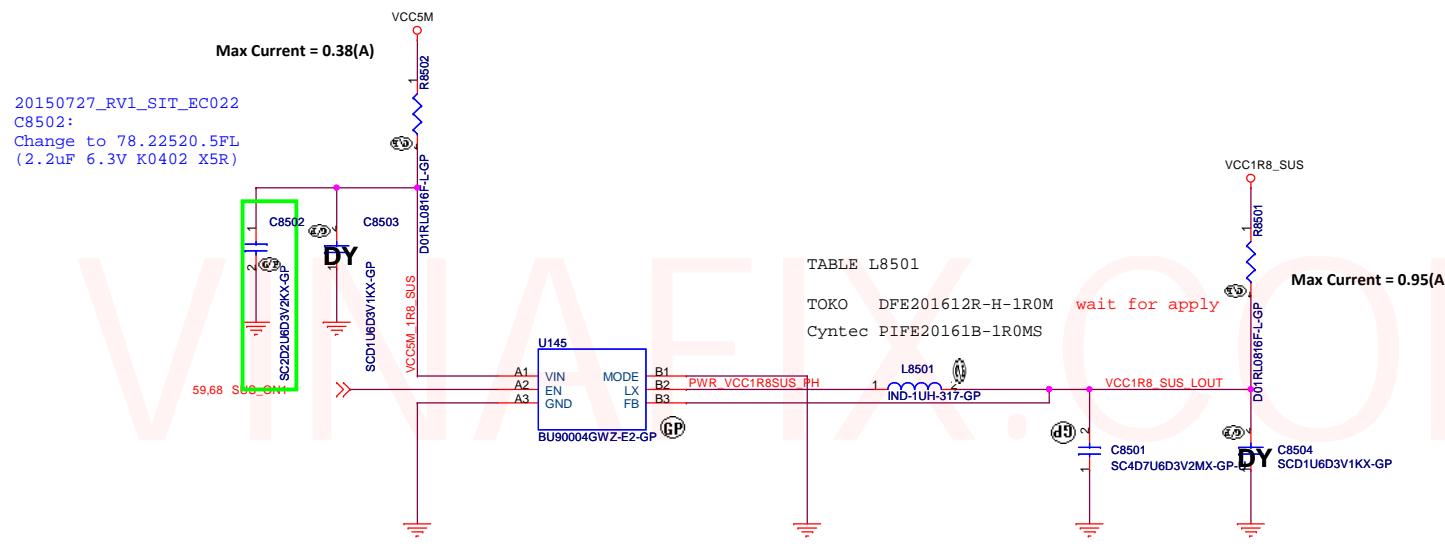


TABLE: TPS51206

S3	S5	VTT	VTRREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)

ULT



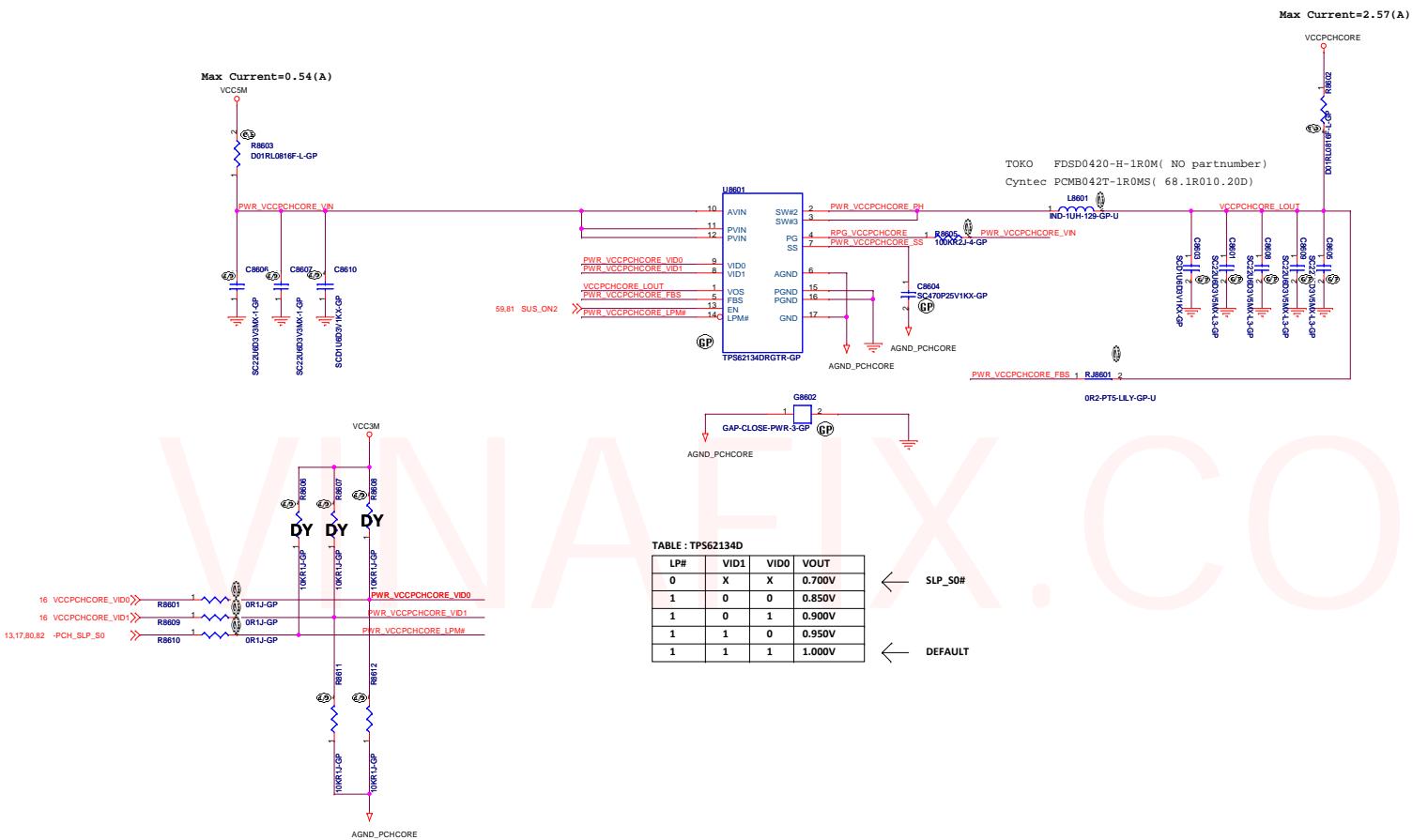


TABLE : TPS62134D

LP#	VID1	VID0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V

SL
DE

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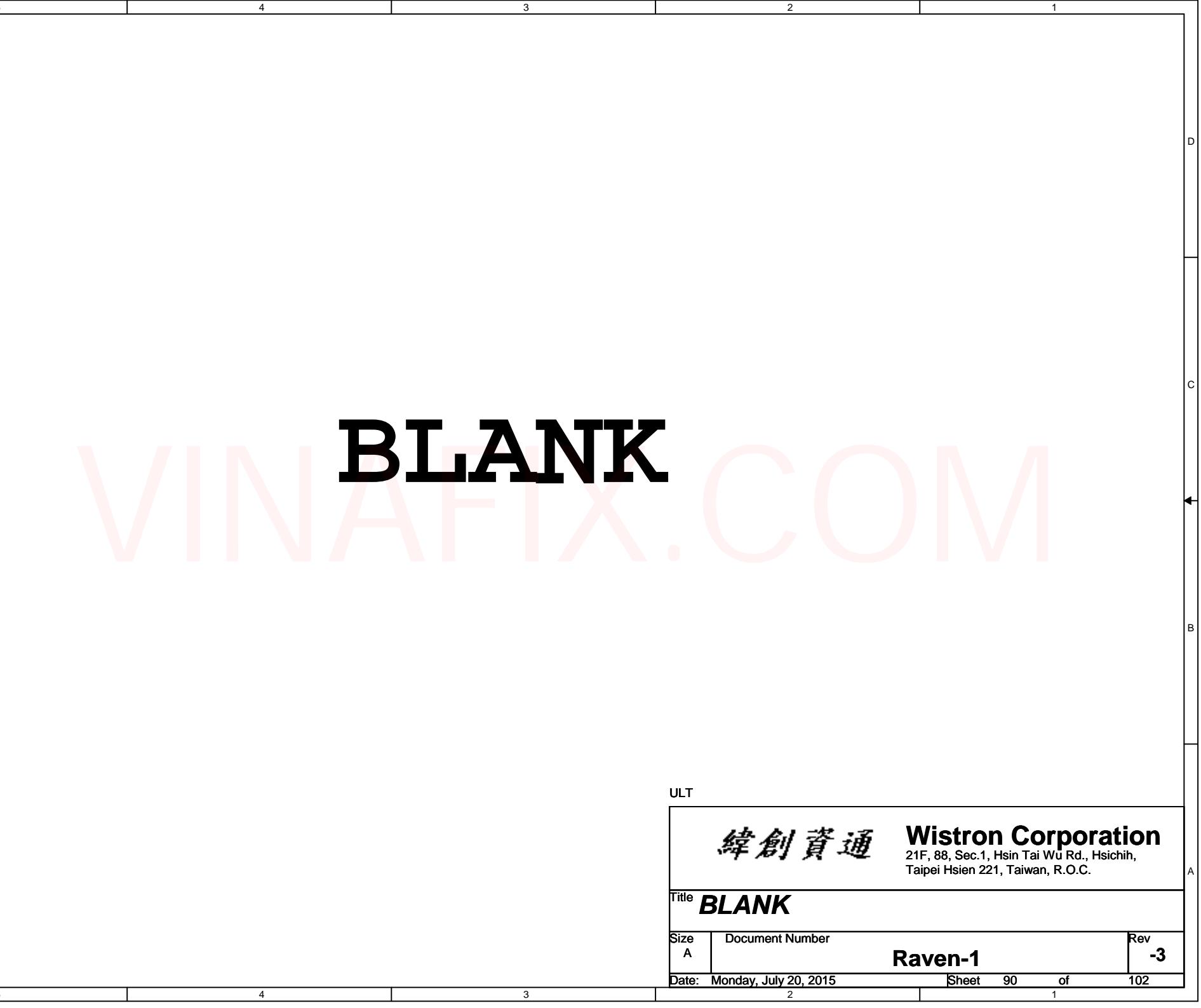
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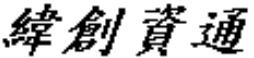


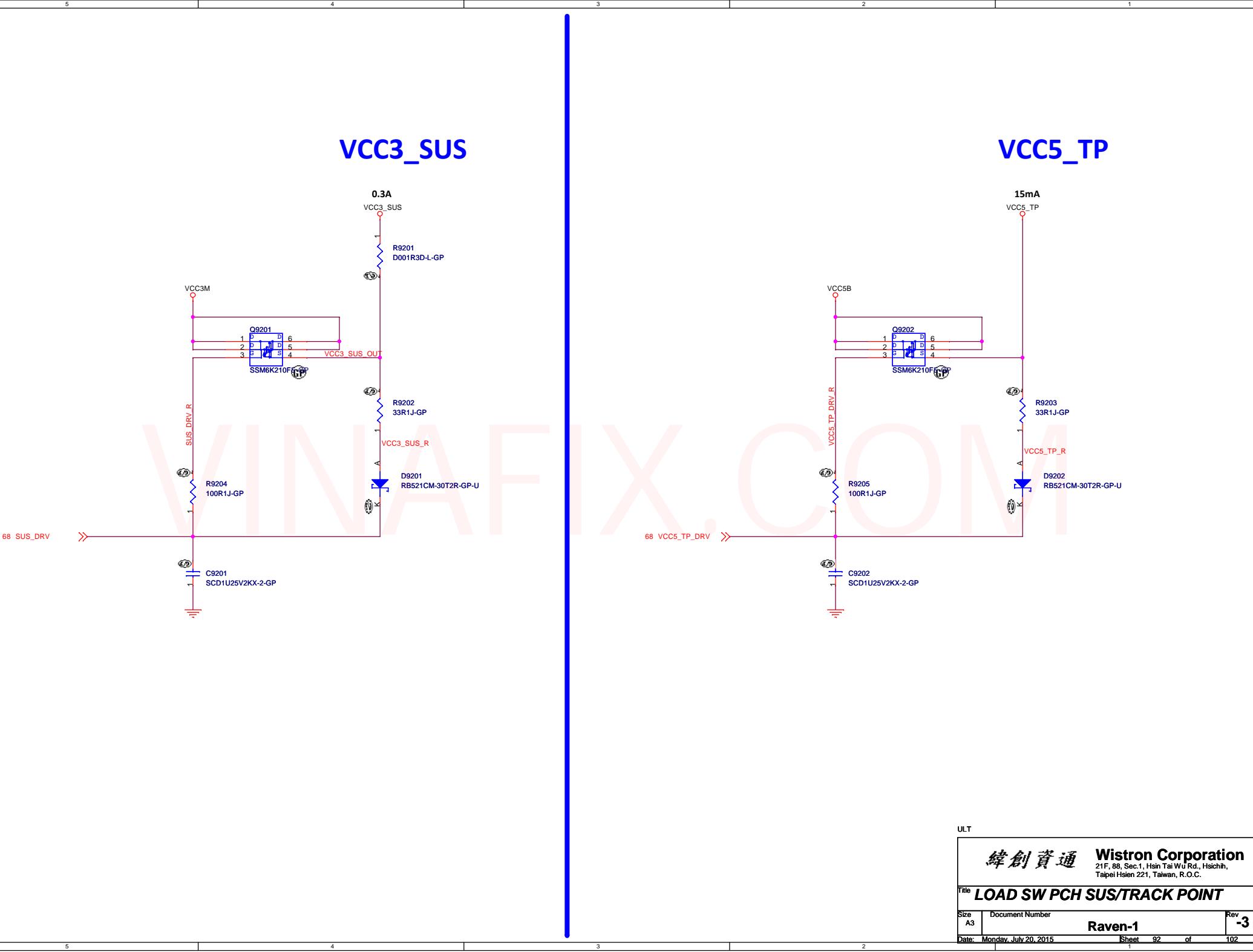
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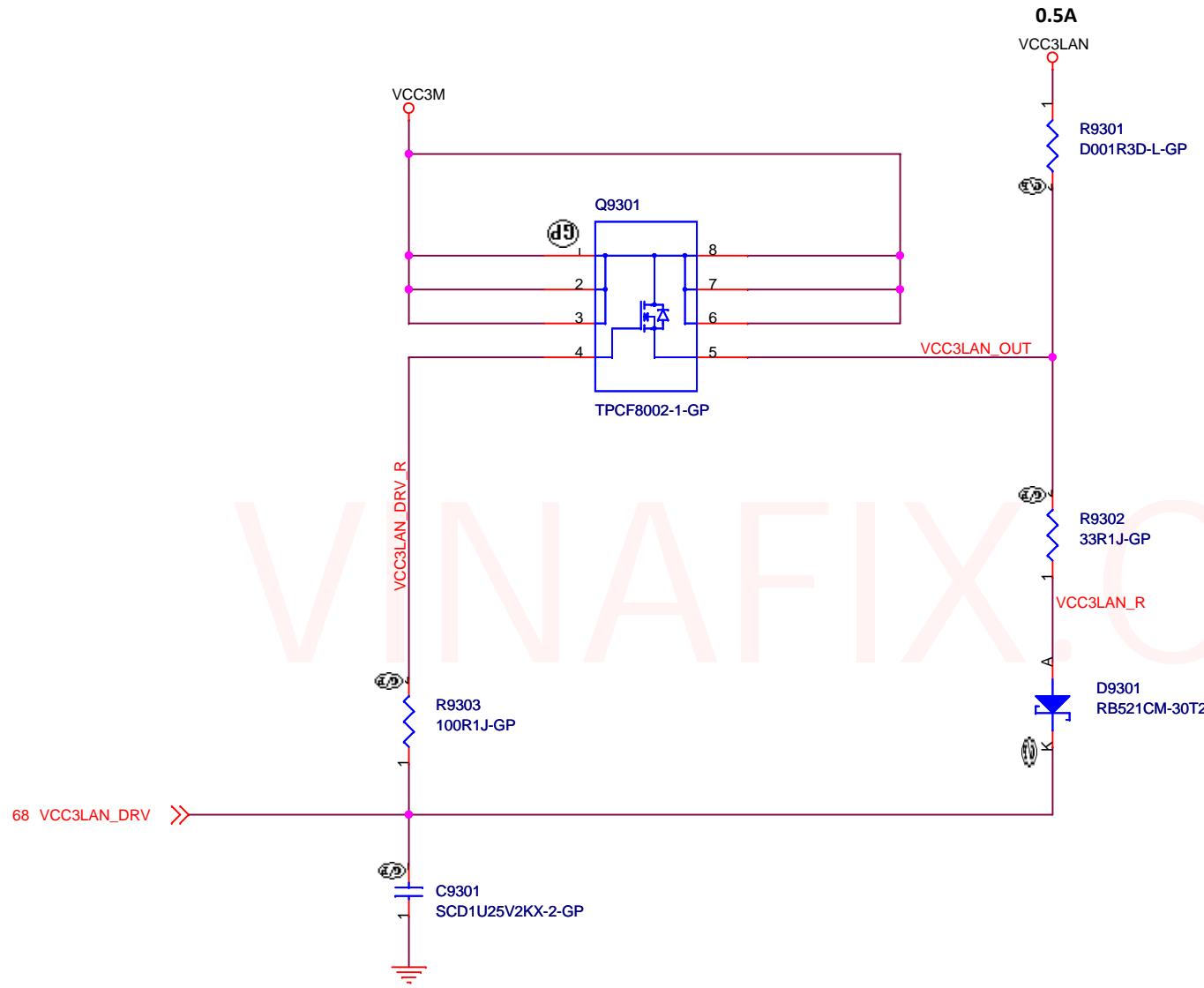
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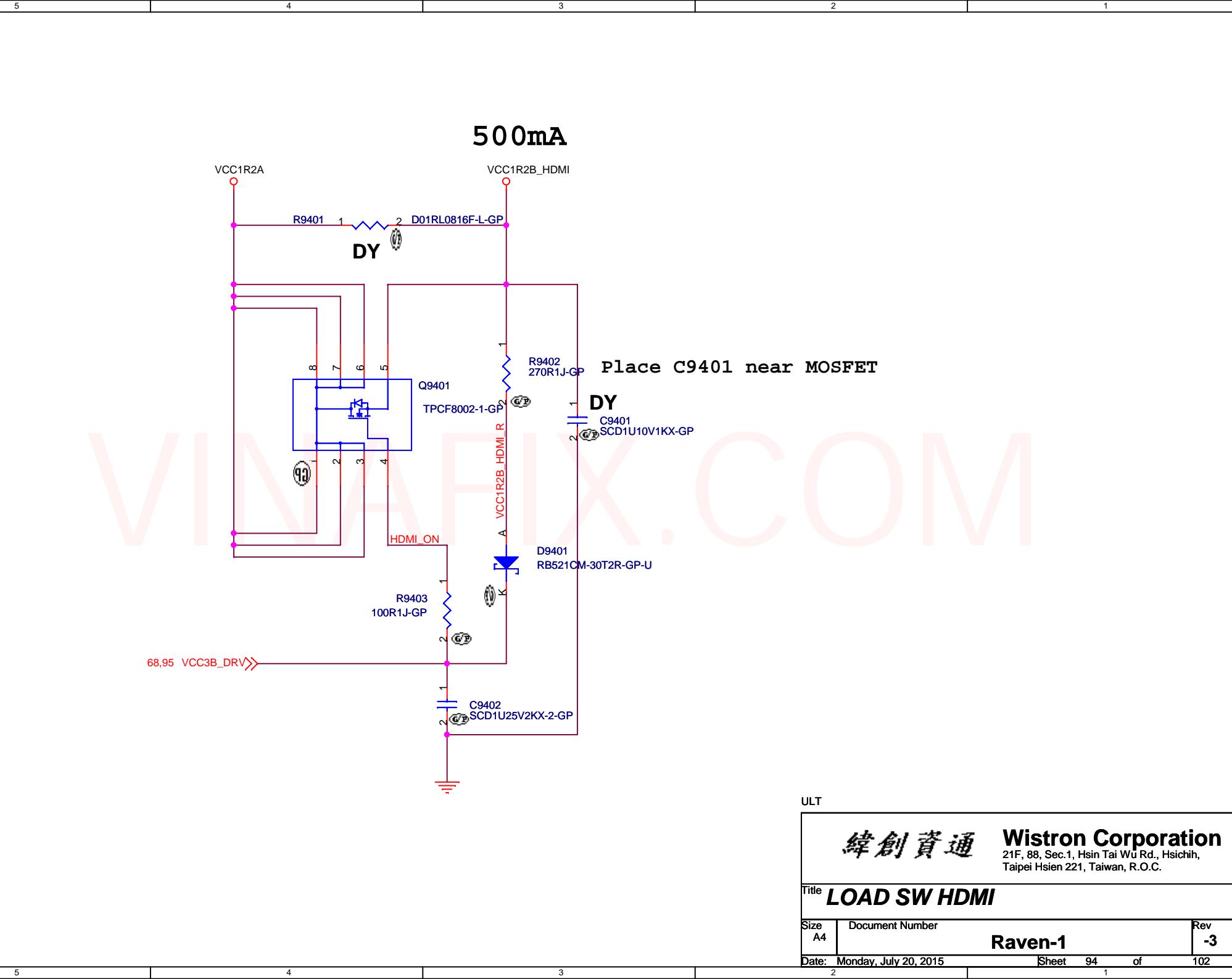
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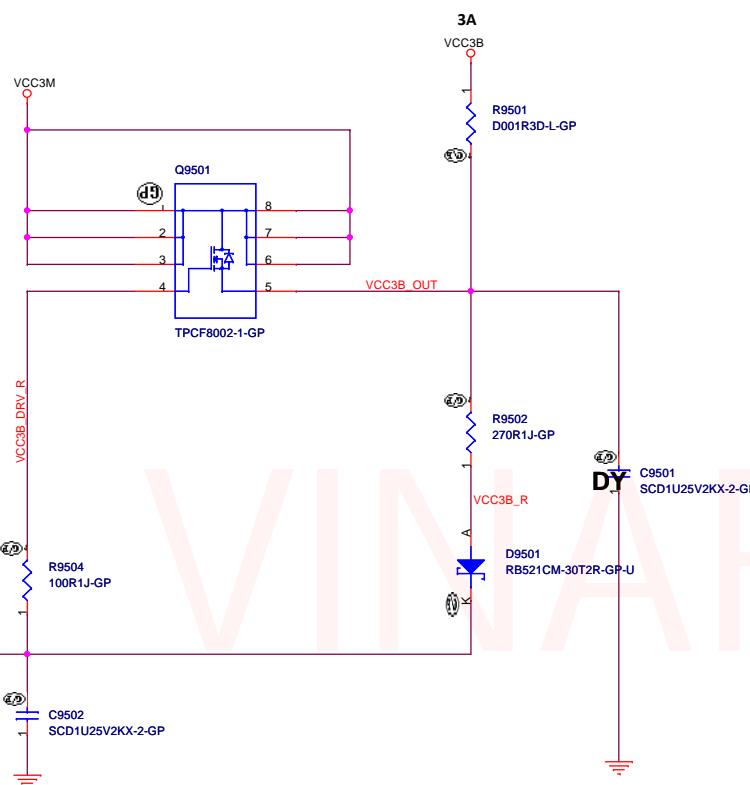
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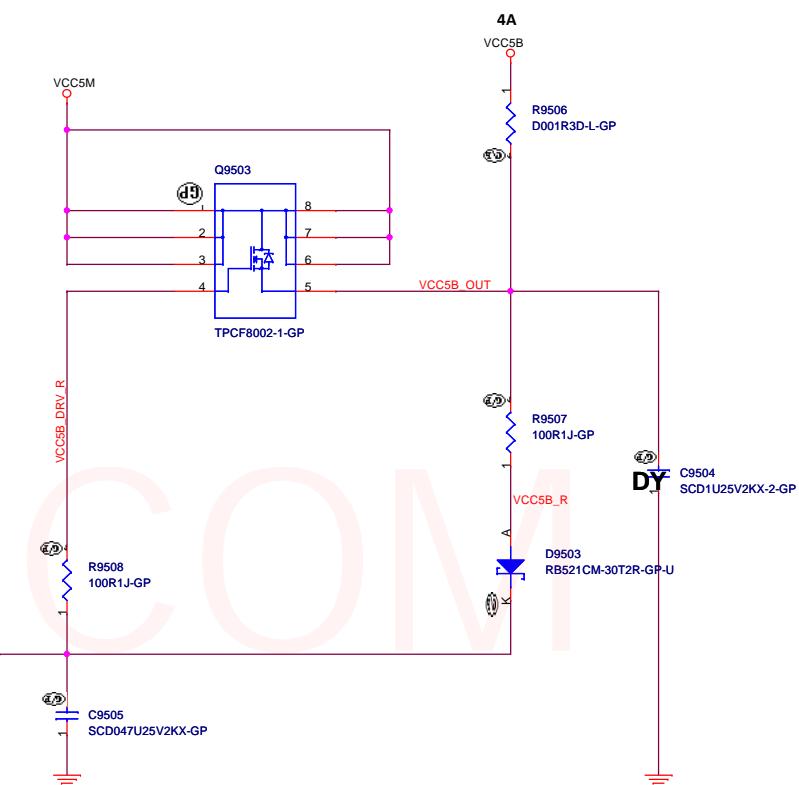
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Size A4	Document Number Raven-1
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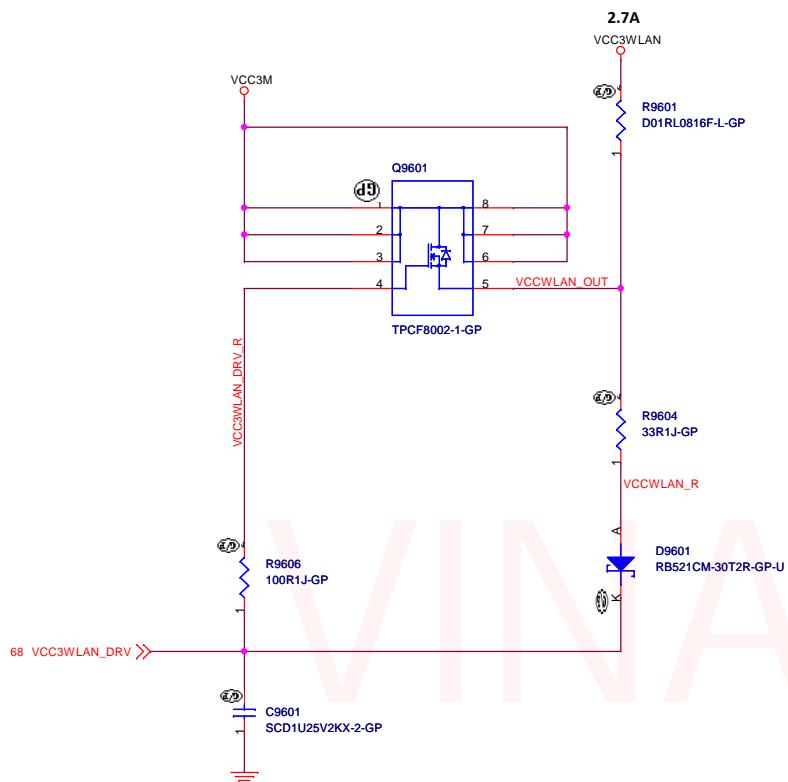
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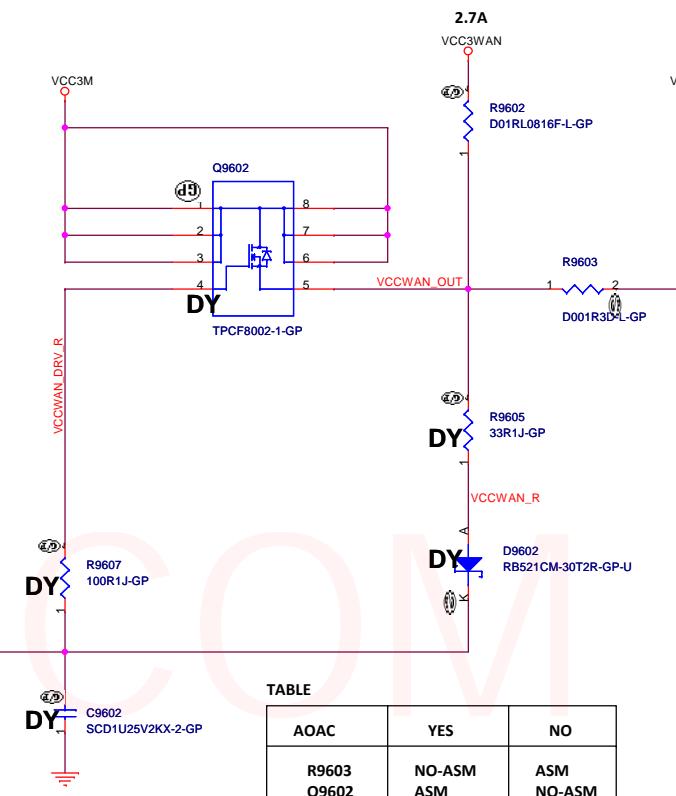
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LOAD SW B		
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WLAN



WWAN

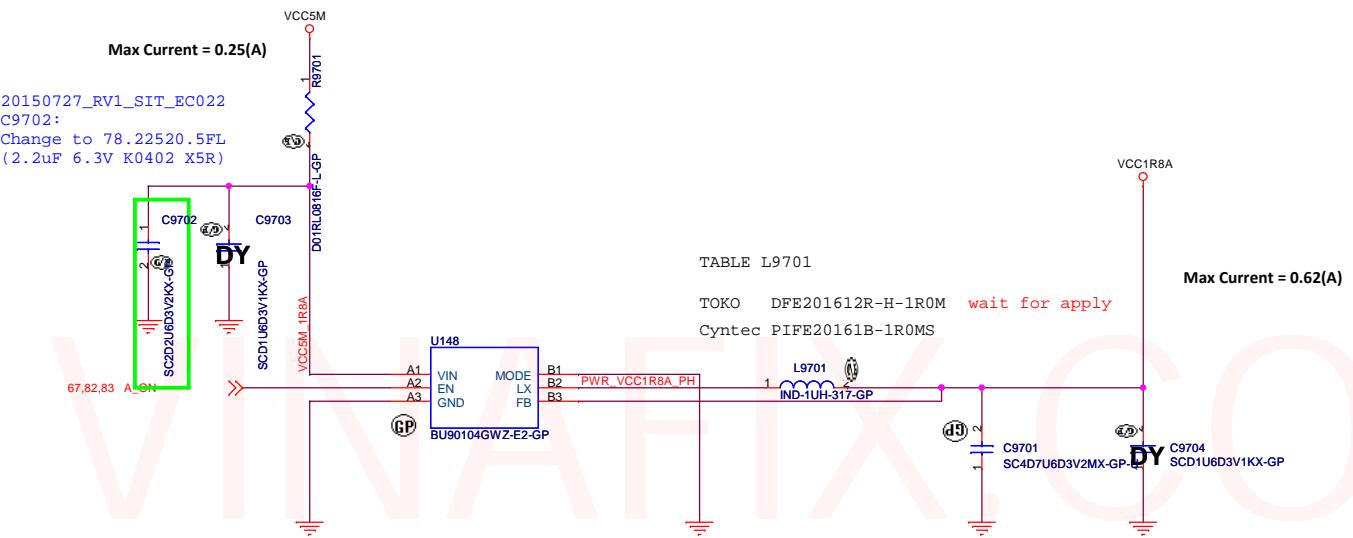


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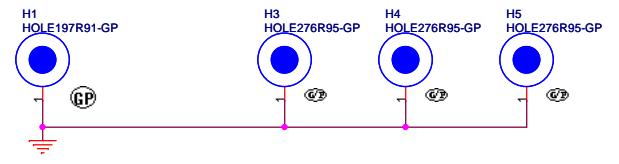
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Q9602	ASM	NO-ASM
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LOGIC
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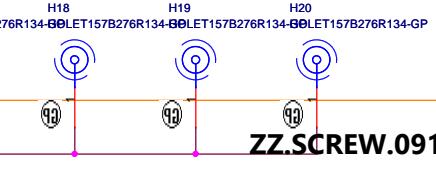
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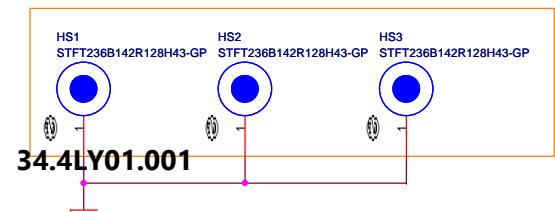


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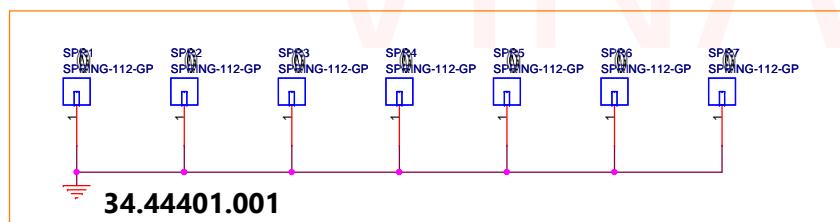
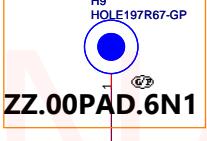
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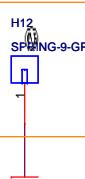
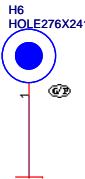


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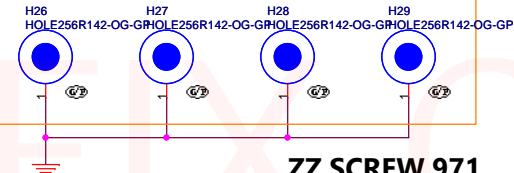
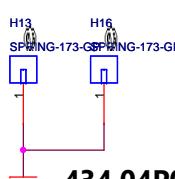
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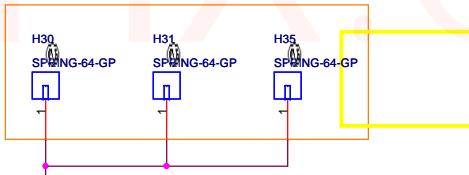
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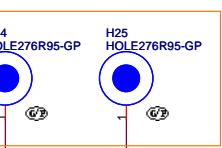


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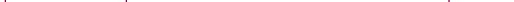


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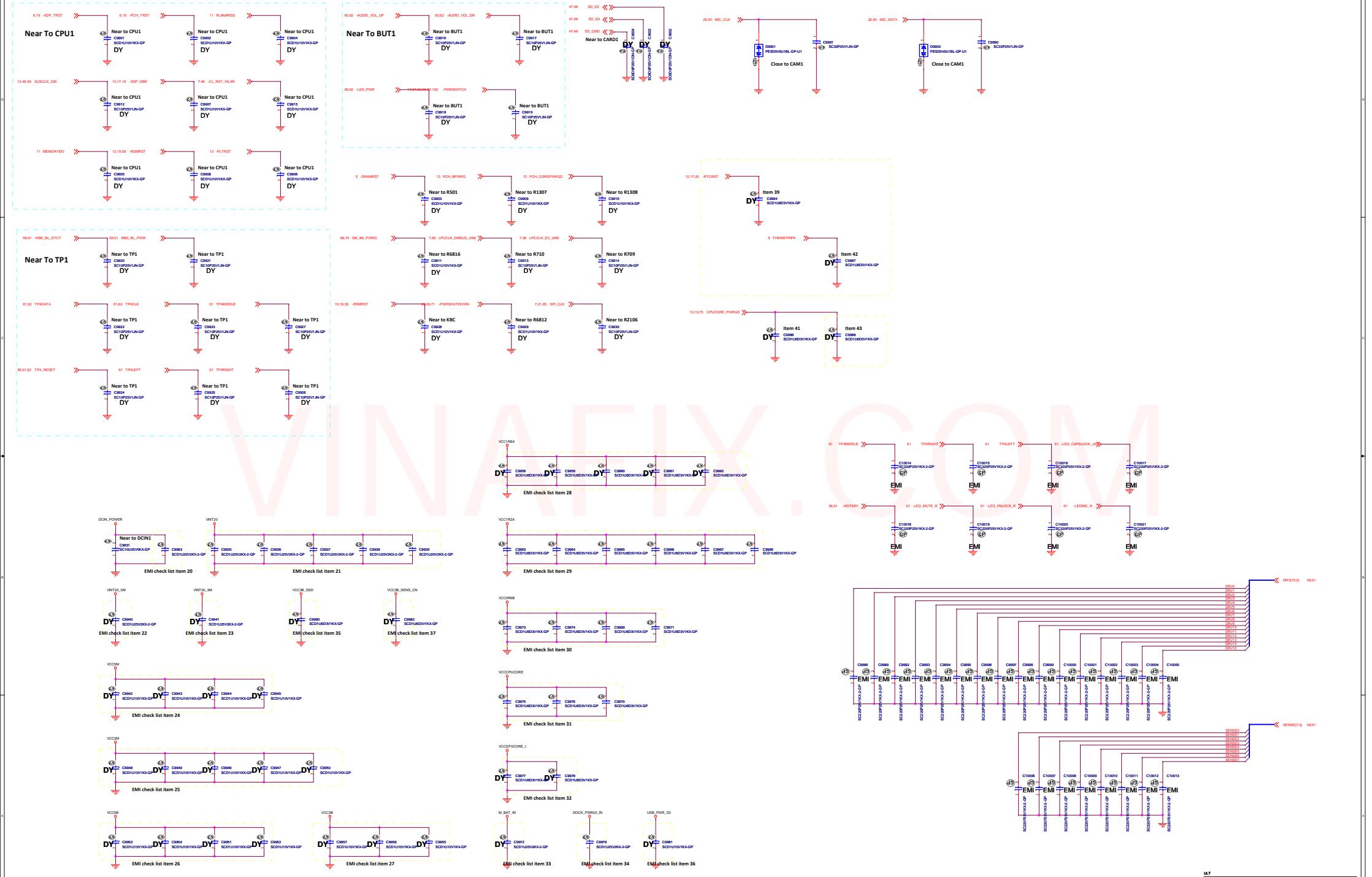
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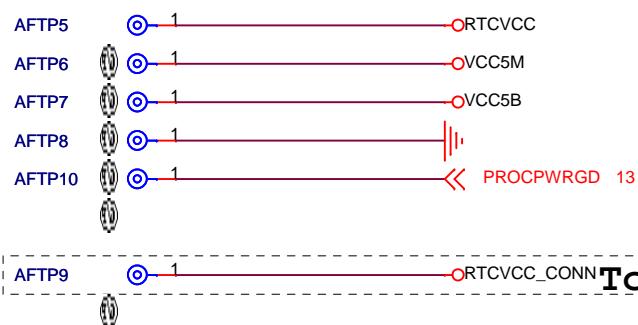


For Power Switch

Top side



Bottom side



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Title EMI DECOUPLING		
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