

# SISTEME DE ACHIZIȚIE DE DATE

## Eșantionarea semnalelor

### Introducere în teoria eșantionării

Odată cu dezvoltarea sistemelor digitale și a tehnologiilor de achiziție a datelor (care se bazează pe convertoare analog-digite și digital-analogice), funcțiile complexe liniare și neliniare implementate cu circuite analogice sunt implementate în mod alternativ cu sisteme care prelucrează eșantioane sub formă de date (sample data systems - SDS).

Dăsi mai costisitoare decât omoloagile analogice, SDS au avantajul flexibilității prin programare. În plus, mulți dintre algoritmi utilizati sunt rezultatul dezvoltărilor din domeniul teoriei procesării semnalelor. În unele cazuri, acești algoritmi sunt capabili de funcții care nu pot fi realizate prin tehnici analogice.

Odată cu utilizarea intensivă a SDS a apărut în mod proporțional și necesitatea de a înțelege bazele teoretice cerute de interfațarea acestor SDS cu lumea analogică.

În continuare sunt tratate câteva aspecte legate de fenomenul de aliasing și de teorema eșantionării.

Teorema eșantionării enunțată de C.E. Shannon în 1949 definește restricții asupra conținutului spectral al semnalelor funcție de timp. Teorema poate fi enunțată în modul cel mai simplu, după cum urmează:

Pentru a recupera cu exactitate funcția semnal  $f(t)$ , este necesar ca  $f(t)$  să fie eșantionată cu o rată mai mare decât de două ori frecvența maximă din compoziția sa spectrală.

Practic, pentru a eșantiona un semnal analogic cu frecvență maximă de 2kHz, trebuie folosită o rată de eșantionare de cel puțin 4kHz pentru a păstra și recupera cu exactitate forma de undă.

Consecințele eșantionării unui semnal la o rată inferioară frecvenței maxime din spectrul semnalului analogic determină apariția unui fenomen numit *aliasing*. Această concept constă în faptul că o componentă spectrală pierde identitatea unei alte frecvențe, atunci cind se produce recuperarea semnalului din eșantioane. În Figure 1(a) este un circuit ideal de eșantionare, cu perioada de eșantionare  $T$  ilustrată în (b), care eșantionează forma de undă  $f(t)$  din (c). Setul de date rezultat din eșantionare este ilustrat în (d) și poate fi definit ca un eșantion al punctelor funcției continue  $f(t)$ . În Figure 1(e), o altă componentă spectrală analogică,  $f'(t)$  poate fi identificată ca având același set de date de eșantionare ca funcția  $f(t)$  din (d). Datorită acestui fenomen, este dificil de determinat care dintre cele două componente spectrale este observată în realitate.

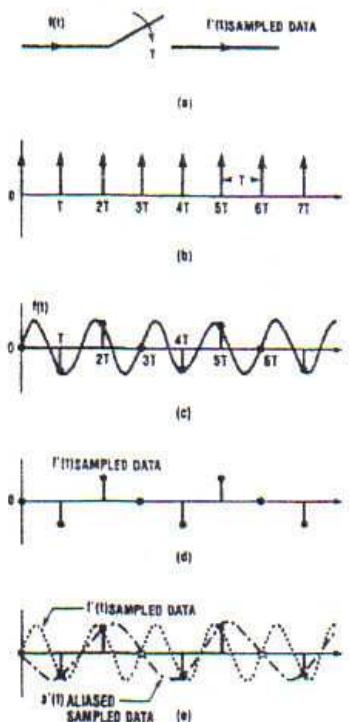


Figure 1 – În urma eșantionării, mai multe semnale pot conține același set de puncte (date). Semnalele sunt *alias* între ele.

La prima vedere poate fi spus că pot fi realizate proceduri de proiectare care să evite apariția fenomenului de *aliasing*, prin eșantionarea cu o rată mai mare decât dublul componentei spectrale de frecvență maximă a semnalului care este eșantionat. În realitate, cele mai multe semnale nu au un spectru limitat, ci conțin întregul spectru de componente: componente dorite,

dar și componente datorate zgomotului alb. Pentru a recupera această informație într-un mod precis, sistemul ar avea nevoie de o rată de eșantionare extrem de mare, nerealizabilă practic. Această dificultate poate fi depășită cu ușurință prin preconditionarea semnalului de intrare, adică prin limitarea spectrului său până la o frecvență stabilită (filtrare). Filtrul de preconditionare, denumit în mod uzual filtru *anti-aliasing*, garantează, spre exemplu în cazul filtrului trece jos, că SDS primește semnale analogice cu un conținut spectral care nu depășește frecvențele permise de filtru. Așa cum este ilustrat în Figure 2, mecanismul de eșantionare cu minimum dublul frecvenței maxime din spectrul semnalului de intrare devine facil.

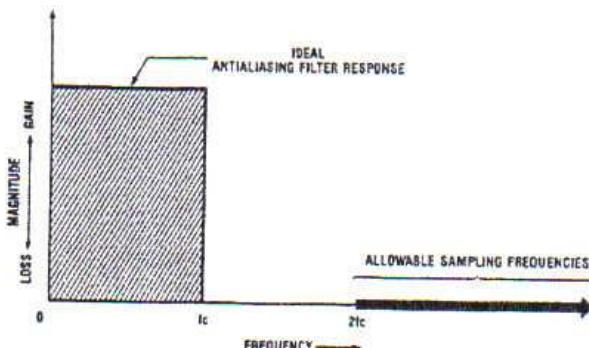


Figure 2 – În partea hașurată, este ilustrat răspunsul unui filtru trece jos ideal. Semnalele care trec prin acest filtru sunt limitate la frecvențe care nu sunt mai mari decât frecvența de tăiere,  $f_c$ . În conformitate cu teorema eșantionării, pentru a recupera semnalul de bandă limitată cu precizie, rata de eșantionare trebuie să fie mai mare decât  $2f_c$ .

Teorema eșantionării poate fi ilustrată grafic în cele două faze ale procesului: eșantionarea semnalului analogic de intrare (preconditionat) în Figure 3 și recuperarea semnalului analogic inițial din setul de date al semnalului digital în Figure 4.

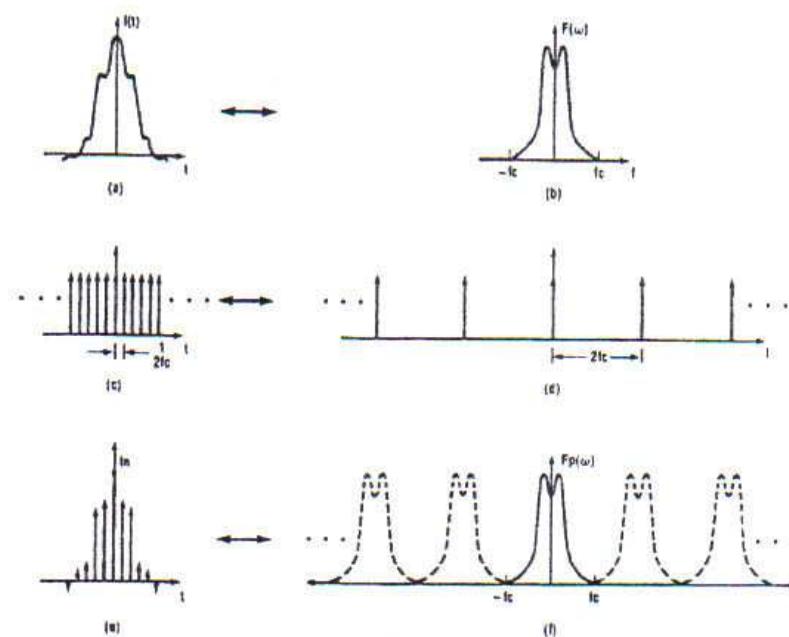


Figure 3 – Transformata Fourier a semnalului analogic eșantionat. În stânga sunt imaginile în domeniul timp, în dreapta, în domeniul frecvență, ale: (a), (b) – semnalul de intrare, (c),(d) – funcția de eșantionare, (e), (f) – semnalul eșantionat.

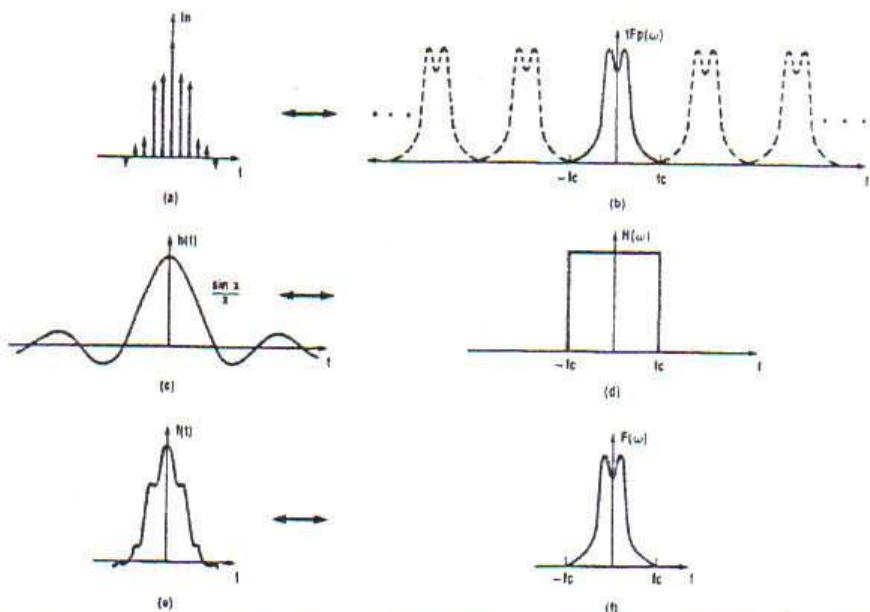


Figure 4 – Transformata Fourier a semnalului analogic recuperat din semnalului eșantionat. În stânga sunt imaginile în domeniul timp, în dreapta, în domeniul frecvență, ale: (a), (b) – semnalul eșantionat, (c),(d) – funcția de recuperare, (e), (f) – semnalul analogic recuperat.

Frecvența  $f_c$  din în Figure 4(d) reprezintă jumătatea ratei de eșantionare și este definită ca fiind frecvența Nyquist (după Harry Nyquist, de la Bell Laboratories). Această frecvență mai este numită frecvență de aliasing sau frecvență de suprapunere. Pentru a preveni apariția fenomenului de aliasing într-un SDS, frecvența de eșantionare ar trebui alesă astfel încât să fie mai mare decât dublul componentei spectrale superioare  $f_c$  a semnalului care este eșantionat.

În Figure 3(f) și în Figure 4(b) se observă că se regăsește spectrul original al semnalului analogic de intrare, precum și un număr infinit de imagini ale acestuia, care nu se suprapun. În Figure 5 este ilustrat fenomenul se suprapunere spectrală (aliasing), care apare atunci când eșantionarea se face cu o rată mai mică decât dublul frecvenței maxime din spectrul semnalului eșantionat. Ca urmare a subeșantionării, informația cuprinsă în semnalul inițial nu mai poate fi separată de imaginile multiplicate.

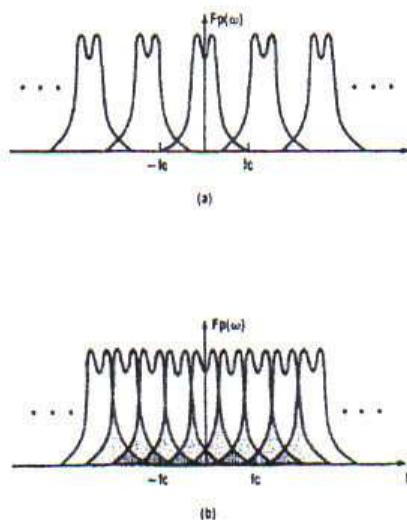
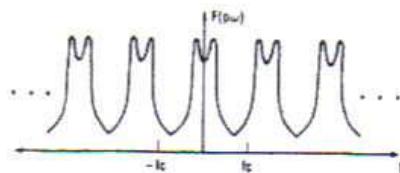
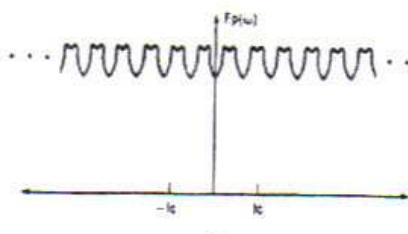


Figure 5 – Suprapunerea spectrală (aliasing), determinată de (a) subeșantionare sau (b) subeșantionare exagerată



(a)



(b)

Figure 6 – Anvelopa spectrală determinată de (a) subeşantionare sau (b) subeşantionare exagerată, care nu mai permite identificarea conţinutului spectral al semnalului analogic iniţial.

### Teorema eşantionării şi implicaţiile sale hardware

Deşi există numeroase tehnici sofisticate de implementare, este bine să subliniem faptul că ne vom opri în continuare la aspectele cele mai comune ale eşantionării.

În Figure 7 este prezentată schema bloc a unui SDS. Aşa cum este ilustrat în figură, înainte de orice procesare de semnal, semnalul analog de intrare trebuie precondiţionat, pentru a preveni apariţia fenomenului de aliasing, apoi digitizat în semnale logice care pot fi utilizate de orice bloc logic.



Figure 7 – Schema bloc generală a unui sistem de eşantionare a datelor (SDS) cu un singur canal.

Funcţiile antialiasing şi de digitizare sunt realizate de un filtru de intrare şi de un convertor analog-digital, respectiv. Odată semnalul digitizat, el poate fi alterat sau procesat, iar după finalizarea procesării, poate fi reconstruit înapoi într-un semnal continuu analogic, prin intermediul unui convertor digital-analogic, urmat de un filtru de netezire.

Nu am făcut precizări cu privire la blocul S/H prezentat în Figure 7. În general, convertorul analog-digital poate opera ca unitate de sine stătătoare. Cu toate acestea, în multe procese de viteză ridicată, viteza convertorului nu este suficientă și necesită asistență unui circuit de eşantionare și memorare (sample and hold – S/H).

### Consideraţii privind filtrul antialiasing de intrare

Aşa cum a fost prezentat mai sus, filtrul antialiasing ar trebui să limiteze banda de frecvenţe a semnalului de intrare la frecvenţe care nu depăşesc frecvenţa Nyquist. În realitate, cu toate acestea, filtrele nu sunt ideale, și au caracteristici tipice de atenuare și fază aşa cum sunt ilustrate în Figure 8.

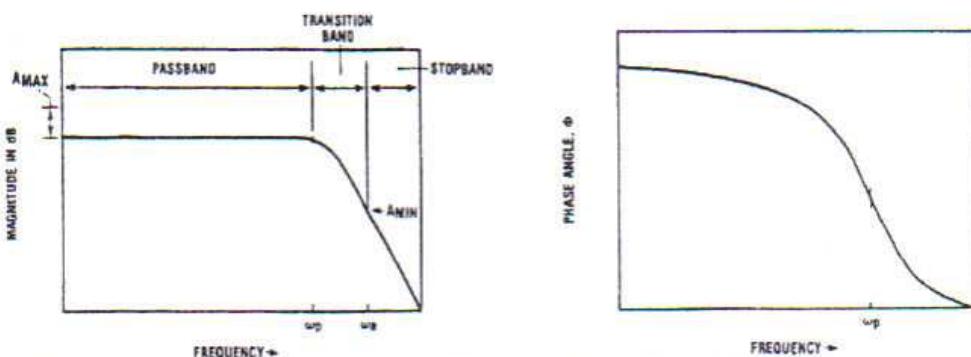


Figure 8 – Caracteristica tipică a unui filtru - atenuare și fază în funcție de frecvență.

Limitarea completă a spectrului semnalului de intrare nu este practic posibilă. În SDS, limitarea spectrului este realizată prin atenuarea acelor frecvenţe mai mari decât frecvenţa Nyquist până la un nivel care este nedetectabil de către convertorul analog-digital. Acum acest nivel este de regulă mai mic decât nivelul de zgomot de quantizare (în valoare efectivă) al convertorului utilizat.

De exemplu, pentru un convertor AD pe 8 bit, cu 2,56V referință, nivelul de zgomot de cuantizare (în valoare efectivă) al convertorului este de -59dB. Pentru filtrul Butterworth a cărui caracteristică este ilustrată în Figure 9, acest nivel poate fi satisfăcut de orice ordin n. Cu cât ordinul filtrului este mai ridicat, cu atât panta caracteristicii atenuare este mai abruptă, iar filtrul se apropie de ideal.

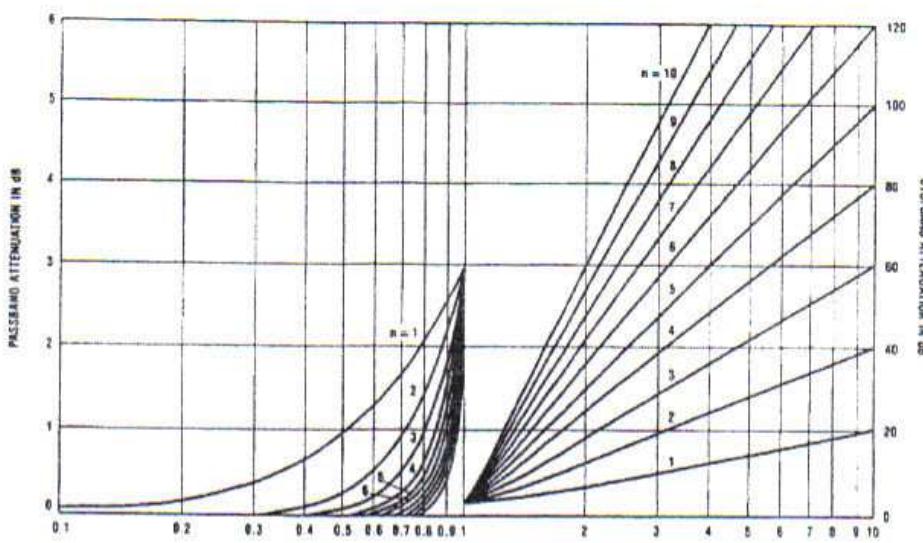


Figure 9 – Caracteristica atenuare în funcție de frecvență pentru un filtru Butterworth de grad n.

Convertorul AD nu va primi frecvențele mai mari decât frecvența de tăiere a filtrului fa din Figure 8, deci frecvența de de eșantionare a semnalului analogic de intrare poate fi aleasă mai mare decât 2fa. Portiunea de frecvențe cel mai puțin distorsionate este cea dintre 0 și fp. Frecvențele din banda de tranziție sunt distorsionate într-o măsură destul de mare, deși obiectivul filtrului a fost acela de limitare a frecvențelor utile la frecvența de tăiere fp. Datorită răspunsului non-ideal al filtrului, adevarata frecvență Nyquist apare la fa.

Din cele enunțate, rezultă că proiectarea filtrului antialiasing este foarte simplă. Nu trebuie scăpat din vedere faptul că toate formele de undă sunt compuse din sume și diferențe de componente spectrale diferite, ca urmare dacă răspunsul unui filtru trece bandă nu este plat pentru spectrul de frecvențe dorit, semnalul recuperat va fi o insumare aproximativă/cronată a tuturor componentelor spectrale alterate prin atenuări diferite în banda de trecere a filtrului.

În plus, proiectarea filtrului antialiasing nu trebuie să piardă din vedere efectul de întârziere. Așa cum este ilustrat în Figure 8, timpul de întârziere corespunde unei deplasări specifice de fază la o anumită frecvență. În mod similar cu considerațiile legate de aplativare caracteristicii de atenuare în banda de trecere, dacă deplasarea de fază a filtrului nu este exact proporțională cu frecvența, semnalul de ieșire va fi o formă de undă în care suma tuturor componentelor spectrale a fost alterată de modificări ale fazelor. În contrast față de panta caracteristicii de atenuare, cu cât ordinul filtrului Butterworth este mai ridicat, cu atât întârzierea devine mai non-ideală (crește), ceea ce duce la un semnal de ieșire distorsionat.

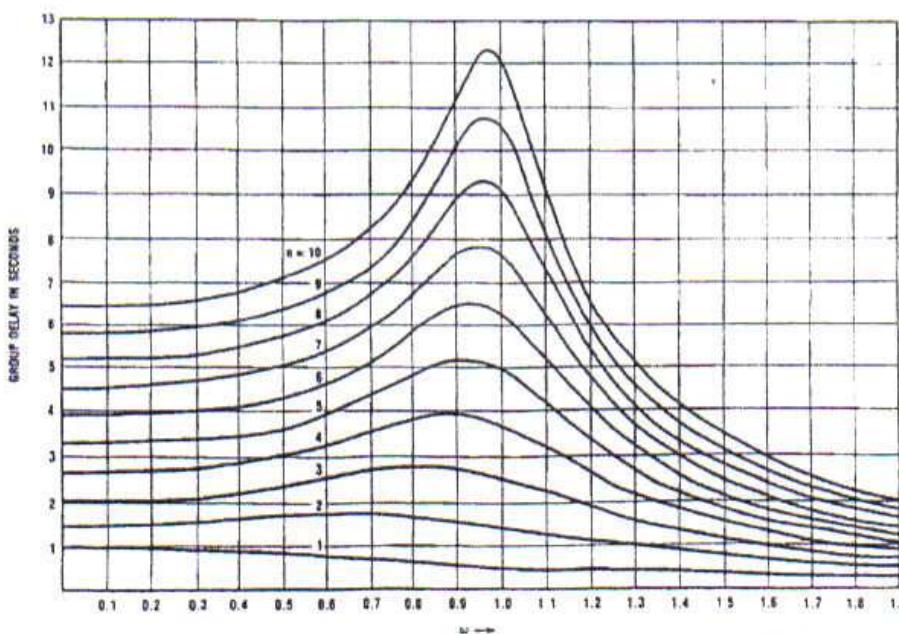


Figure 10 – Caracteristica întârziere de grup în funcție de frecvență pentru un filtru Butterworth de grad n.

Un fenomen suplimentar este cel legat de efectul eșantionării. În urma eșantionării unui semnal, se produce multiplicarea semnalului cu un tren de impulsuri unitate. Forma de undă care rezultă are un spectru care este conoluția dintre spectrul semnalului inițial și spectrul trenului de impulsuri unitate, așa cum este reprezentat în Figure 11. Datorită filtrării și efectului de întârziere a funcției  $\sin(x)/x$ , combinate cu efectele filtrării antialiasing non-ideale, o parte din suma și diferența componentelor spectrale ar putea apărea în interiorul spectrului semnalului inițial, ceea ce produce erori de aliasing.

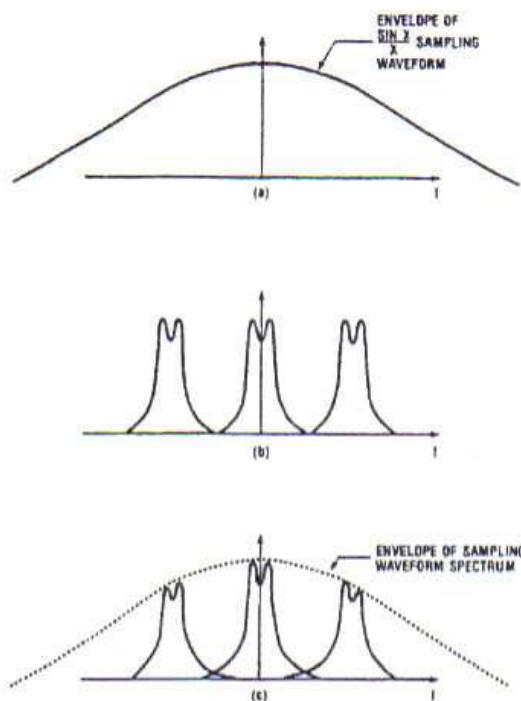


Figure 11 – Semnalul (c) al semnalului eșantionat rezultă prin conoluția între (a) și (b)

Un filtru antialiasing cât mai apropiat de ideal este cu atât mai complex și dificil de realizat. În orice caz, nu pot fi înălțurate complet fenomenele de atenuare diferită în banda de trecere și de distorsionare și alias a semnalului de intrare. În final, proiectarea trebuie să implice un compromis între complexitatea filtrului, viteza de eșantionare, deci și banda de lucru a sistemului.

## Concepțe de bază privind filtrarea

Un filtru este un dispozitiv utilizat pentru separarea semnalelor pe baza frecvenței lor și este de obicei realizat din componente de circuit pasive, reactive și/sau active. Există cinci tipuri de filtre utilizate pentru trecerea sau oprirea semnalelor, definite după cum urmează:

1. **Filtrul trece jos (low-pass filter)** permite trecerea frecvențelor din banda de trecere (passband), determinată de frecvența 0 (curent continuu) și o frecvență de tăiere. În banda de trecere există o valoare maximă a variației atenuării (ripple). Frecvențele de dincolo de  $f_c$  pot fi atenuate puternic, însă dincolo de o frecvență  $f_s$ , o anumită atenuare minimă trebuie să fie garantată, în banda de oprire (stopband). Regiunea de tranziție sau banda de trecere (transition band) este definită de frecvențele dintre  $f_c$  și  $f_s$ .

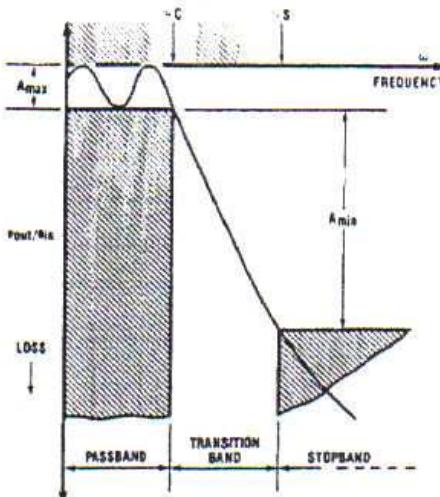


Figure 12 – Răspunsul unui filtru trece jos

2. **Filtrul trece sus (high-pass filter)**

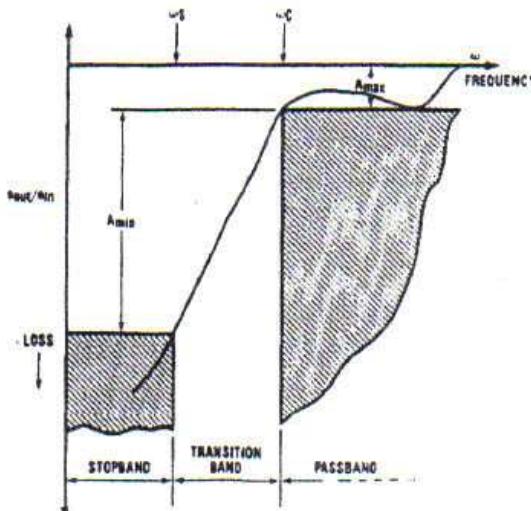


Figure 13 – Răspunsul unui filtru trece sus

3. **Filtrul trece bandă (band pass filter)**

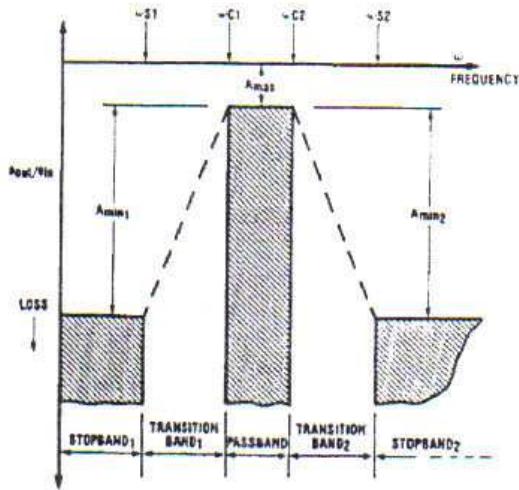


Figure 14 – Răspunsul unui filtru trece bandă

#### 4. Filtrul oprește bandă (band reject filter)

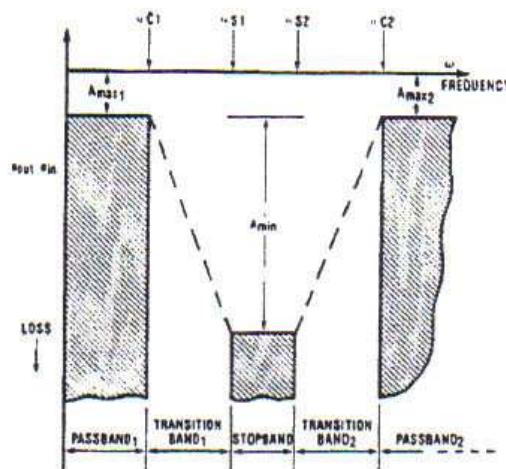


Figure 15 – Răspunsul unui filtru opește bandă

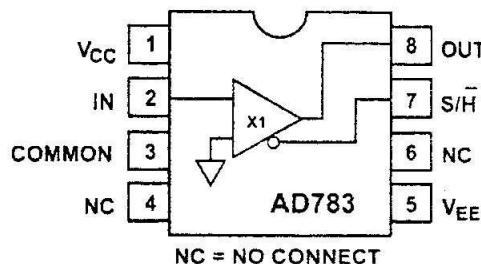
4. Filtrul **trece tot (all pass)**, sau filtru schimbător de fază, permite tuturor frecvențelor să treacă, fără a introduce o atenuare semnificativă. Filtrul introduce o deplasare de fază predictibilă, pentru toate frecvențele, fără a o restricționa doar la o anumită bandă de frecvențe.

## AD783\*

### FEATURES

- Acquisition Time to 0.01%: 250 ns Typical
- Low Power Dissipation: 95 mW
- Low Droop Rate: 0.02  $\mu$ V/ $\mu$ s
- Fully Specified and Tested Hold Mode Distortion
- Total Harmonic Distortion: -85 dB
- Aperture Jitter: 50 ps Maximum
- Internal Hold Capacitor
- Self-Correcting Architecture
- 8-Pin Mini Cerdip and SOIC Packages

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION

The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 offers a typical acquisition time of 250 ns to 0.01%. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 100 kHz. The AD783 is configured as a unity gain amplifier and uses a patented self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 retains the held value with a droop rate of 0.02  $\mu$ V/ $\mu$ s. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The J grade device is specified for operation from 0°C to +70°C and the A grade from -40°C to +85°C. The J and A grades are available in 8-pin cerdip and SOIC packages. The military temperature range version is specified for operation from -55°C to +125°C and is available in an 8-pin cerdip package. For details refer to the *Analog Devices Military Products Databook* or AD783/883B data sheet.

### PRODUCT HIGHLIGHTS

1. Fast acquisition time (250 ns), low aperture jitter (20 ps) and fully specified hold mode distortion make the AD783 an ideal SHA for sampling systems.
2. Low droop (0.02  $\mu$ V/ $\mu$ s) and internally compensated hold mode error result in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD783 an ideal choice for a variety of high performance applications.
4. The AD783 requires no external components or adjustments.
5. The AD783 is an excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.

\*Protected by U.S. Patent Number 4,962,325.

REV. A

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# AD783—SPECIFICATIONS

## DC SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with V<sub>CC</sub> = +5 V ± 5%, V<sub>EE</sub> = -5 V ± 5%, C<sub>L</sub> = pF, unless otherwise noted)

Parameter		AD783J/A			
	Min	Typ	Max	Units	
SAMPLING CHARACTERISTICS					
Acquisition Time					
5 V Step to 0.01%		250	375	ns	
5 V Step to 0.1%		200	350	ns	
Small Signal Bandwidth		15		MHz	
Full Power Bandwidth		2		MHz	
HOLD CHARACTERISTICS					
Effective Aperture Delay (+25°C)	-30	15	30	ns	
Aperture Jitter (+25°C)		20	50	ps	
Hold Settling (to 1 mV, +25°C)		150	200	ns	
Droop Rate		0.02	1	µV/µs	
Feedthrough (+25°C) (V <sub>IN</sub> = ±2.5 V, 500 kHz)		-80		dB	
ACCURACY CHARACTERISTICS <sup>1</sup>					
Hold Mode Offset	-5	0	+5	mV	
Hold Mode Offset Drift		10		µV/°C	
Sample Mode Offset		50	200	mV	
Nonlinearity		±0.005		% FS	
Gain Error		±0.03	±0.1	% FS	
OUTPUT CHARACTERISTICS					
Output Drive Current	-5		+5	mA	
Output Resistance, DC		0.3	0.6	Ω	
Total Output Noise (DC to 5 MHz)		150		µV rms	
Sampled DC Uncertainty		85		µV rms	
Hold Mode Noise (DC to 5 MHz)		125		µV rms	
Short Circuit Current					
Source			20	mA	
Sink			13	mA	
INPUT CHARACTERISTICS					
Input Voltage Range	-2.5		+2.5	V	
Bias Current		100	250	nA	
Input Impedance		10		MΩ	
Input Capacitance		2		pF	
DIGITAL CHARACTERISTICS					
Input Voltage Low			0.8	V	
Input Voltage High	2.0			V	
Input Current High (V <sub>IN</sub> = 5 V)		2	10	µA	
POWER SUPPLY CHARACTERISTICS					
Operating Voltage Range	±4.75	±5	±5.25	V	
Supply Current		9.5	17	mA	
+PSRR (+5 V ± 5%)	45	65		dB	
-PSRR (-5 V ± 5%)	45	65		dB	
Power Consumption		95	175	mW	
TEMPERATURE RANGE					
Specified Performance (J)	0		+70	°C	
(A)	-40		+85	°C	

### NOTES

<sup>1</sup>Specified and tested over an input range of ±2.5 V.

Specifications subject to change without notice

## HOLD MODE AC SPECIFICATIONS ( $T_{MIN}$ to $T_{MAX}$ with $V_{CC} = +5 V \pm 5\%$ , $V_{EE} = -5 V \pm 5\%$ , $C_L = 50 pF$ , unless otherwise noted)

Parameter		Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION $f_{IN} = 100$ kHz $f_{IN} = 500$ kHz			-85 -72	-80	dB dB
SIGNAL-TO-NOISE AND DISTORTION $f_{IN} = 100$ kHz $f_{IN} = 500$ kHz			77 70		dB dB
INTERMODULATION DISTORTION ( $F_1 = 99$ kHz, $F_2 = 100$ kHz) Second Order Products Third Order Products				-80 -85	dB dB

## NOTES

<sup>1</sup> $f_{IN}$  amplitude = 0 dB and  $f_{SAMPLE}$  = 300 kHz unless otherwise indicated.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

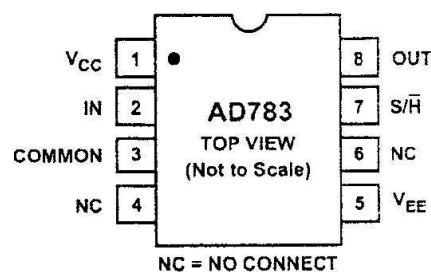
Spec	With Respect to	Min	Max	Units
$V_{CC}$	COM	-0.5	+6.5	V
$V_{EE}$	COM	-6.5	+0.5	V
Analog Input	COM	-6.5	+6.5	V
Digital Input	COM	-0.5	+6.5	V
Output Short Circuit to Ground, $V_{CC}$ , or $V_{EE}$		Indefinite		
Maximum Junction Temperature		-65	+175	°C
Storage			+150	°C
Lead Temperature (10 sec max)			+300	°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD783 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION



## ORDERING GUIDE

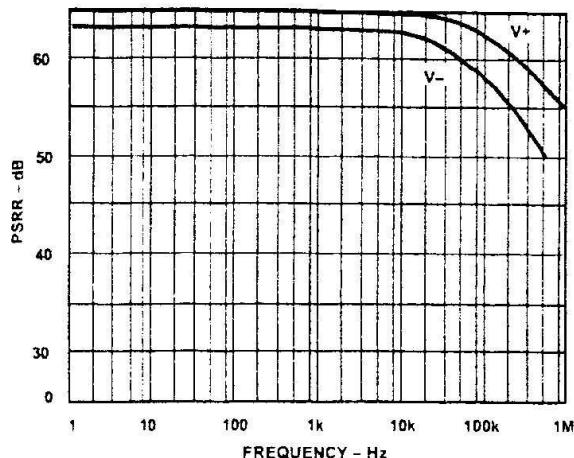
Model <sup>1</sup>	Temperature Range	Description	Package Options <sup>2</sup>
AD783JQ	0°C to +70°C	8-Pin Cerdip	Q-8
AD783AQ	-40°C to +85°C	8-Pin Cerdip	Q-8
AD783JR	0°C to +70°C	8-Pin SOIC	R-8
AD783AR	-40°C to +85°C	8-Pin SOIC	R-8

## NOTES

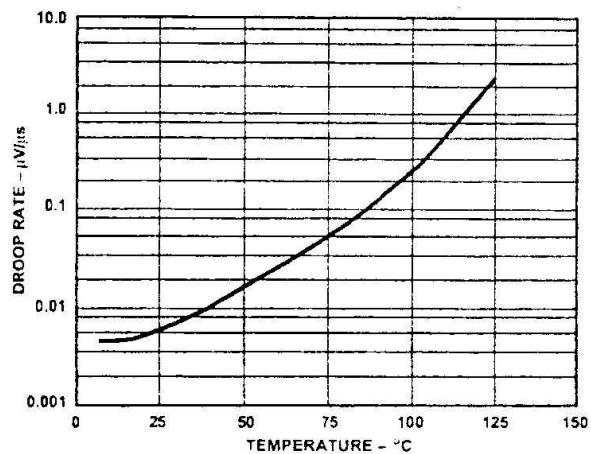
<sup>1</sup>For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD783/883B data sheet.

<sup>2</sup>Q = Cerdip, R = SOIC.

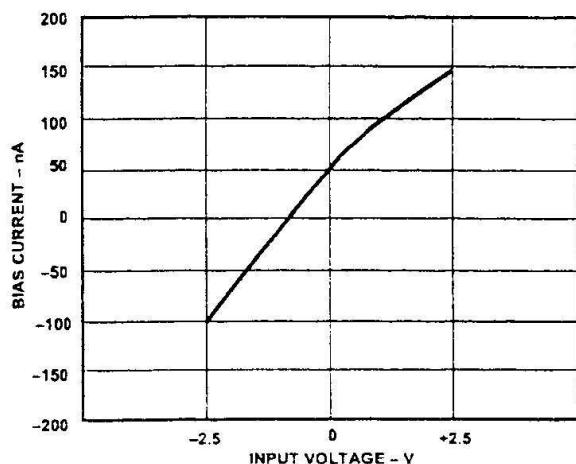
# AD783-Typical Characteristics



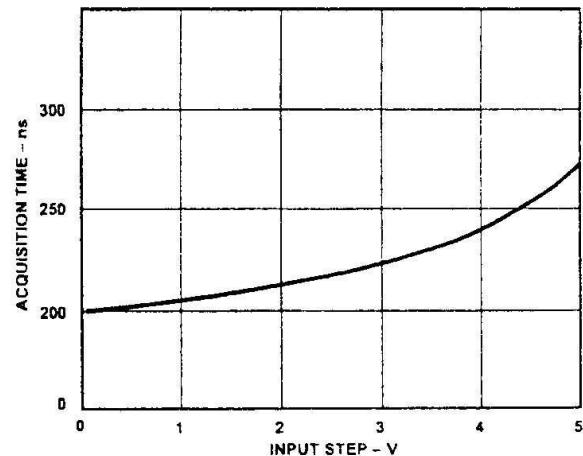
Power Supply Rejection Ratio vs. Frequency



Droop Rate vs. Temperature,  $V_{IN} = 0\text{ V}$



Bias Current vs. Input Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

**DEFINITIONS OF SPECIFICATIONS**

**Acquisition Time**—The length of time that the SHA must remain in the sample mode in order to acquire a full-scale input step to a given level of accuracy.

**Small Signal Bandwidth**—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p-p sine wave.

**Full Power Bandwidth**—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 5 V p-p sine wave.

**Effective Aperture Delay**—The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

**Aperture Jitter**—The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

**Hold Settling Time**—The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

**Droop Rate**—The drift in output voltage while in the hold mode.

**Feedthrough**—The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

**Hold Mode Offset**—The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

**Sample Mode Offset**—The difference between the input and output signals when the SHA is in the sample mode.

**Nonlinearity**—The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of -2.5 V and +2.5 V.

**Gain Error**—Deviation from a gain of +1 on the transfer function of input vs. held output.

**Power Supply Rejection Ratio**—A measure of change in the held output voltage for a specified change in the positive or negative supply.

**Sampled DC Uncertainty**—The internal rms SHA noise that is sampled onto the hold capacitor.

**Hold Mode Noise**—The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

**Total Output Noise**—The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

**Output Drive Current**—The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

**Signal-To-Noise and Distortion (S/N+D) Ratio**—S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

**Total Harmonic Distortion (THD)**—THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed in decibels.

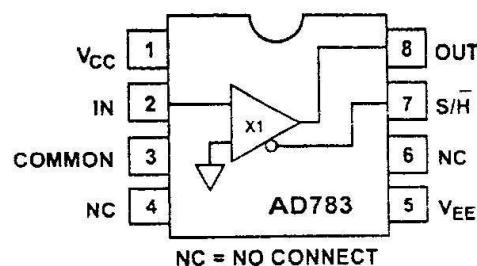
**Intermodulation Distortion (IMD)**—With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any device with nonlinearities will create distortion products, of order  $(m+n)$ , at sum and difference frequency of  $m f_a \pm n f_b$ , where  $m, n = 0, 1, 2, 3, \dots$ . Intermodulation terms are those for which  $m$  or  $n$  is not equal to zero. For example, the second order terms are  $(f_a+f_b)$  and  $(f_a-f_b)$ , and the third order terms are  $(2f_a+f_b)$ ,  $(2f_a-f_b)$ ,  $(f_a+2f_b)$  and  $(f_a-2f_b)$ . The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is -0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

**FUNCTIONAL DESCRIPTION**

The AD783 is a complete, high speed sample-and-hold amplifier that provides high speed sampling to 12-bit accuracy in 250 ns.

The AD783 is completely self-contained, including an on-chip hold capacitor, and requires no external components or adjustments to perform the sampling function. Both input and output are treated as a single-ended signal, referred to common.

The AD783 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD783.



Functional Block Diagram

# AD783

## DYNAMIC PERFORMANCE

The AD783 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD783 to be used with high speed, high resolution A-to-D converters like the AD671 and AD7586. The AD783's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the AD783 can acquire a 5 V step in less than 250 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

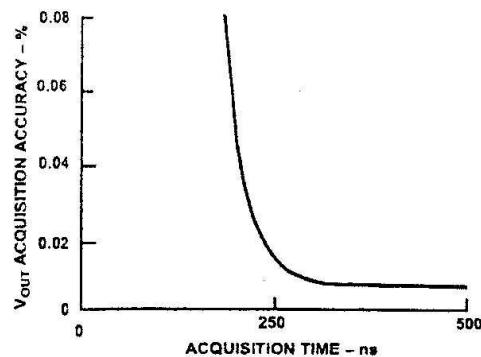


Figure 1. *V<sub>out</sub> Settling vs. Acquisition Time*

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD783 is 150 ns. The settling time of the AD783 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

## HOLD MODE OFFSET

The dc accuracy of the AD783 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of -2.5 V to +2.5 V, the AD783 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 2. As indicated by the AD783 specifications, the hold mode offset is very stable over temperature.

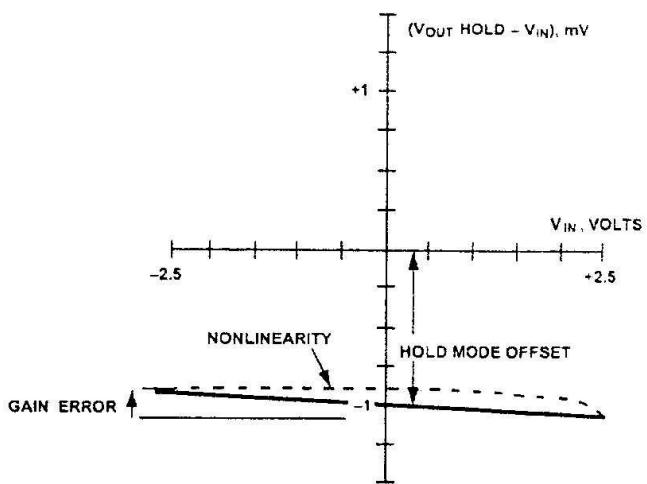


Figure 2. *Hold Mode Offset, Gain Error and Nonlinearity*

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

## SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD783 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1  $\mu$ F capacitors should be connected from  $V_{CC}$  and  $V_{EE}$  to common.

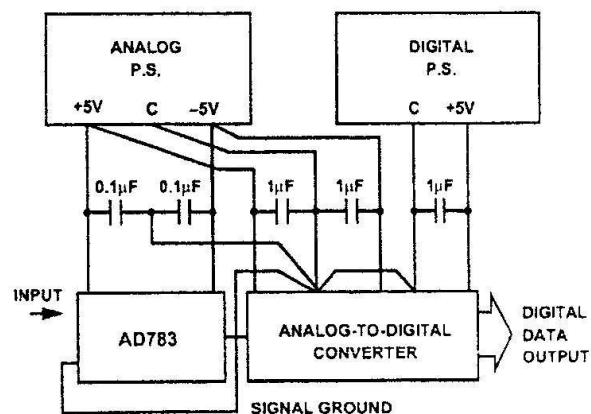


Figure 3. *Basic Grounding and Decoupling Diagram*

The AD783 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD783 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 3 illustrates the recommended decoupling and grounding practice.

### NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD783 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 4.

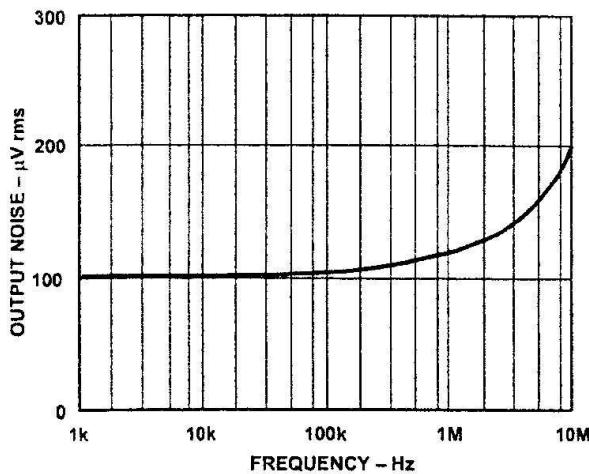


Figure 4. RMS Noise vs. Input Bandwidth of ADC

### DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD783 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over  $5\text{ k}\Omega$ ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD783 is required. The AD711 (precision BiFET op amp) is recommended for these applications.

### HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 5.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 6 and 7 were made using a 14-bit A/D converter with  $V_{IN} = 5\text{ V p-p}$  and a sample frequency of 100 kSPS.

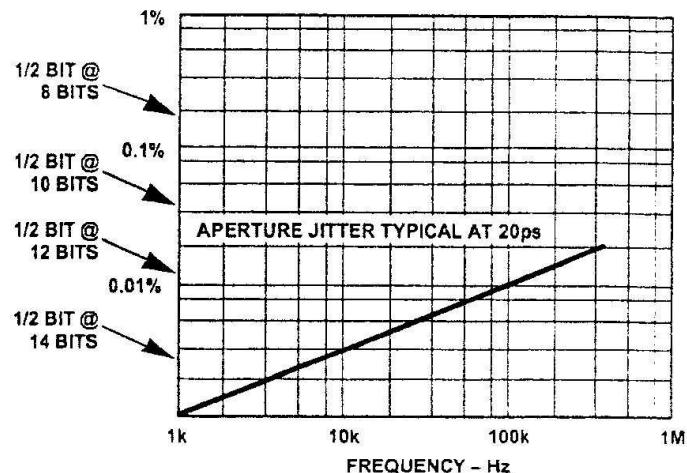


Figure 5. Error Magnitude vs. Frequency

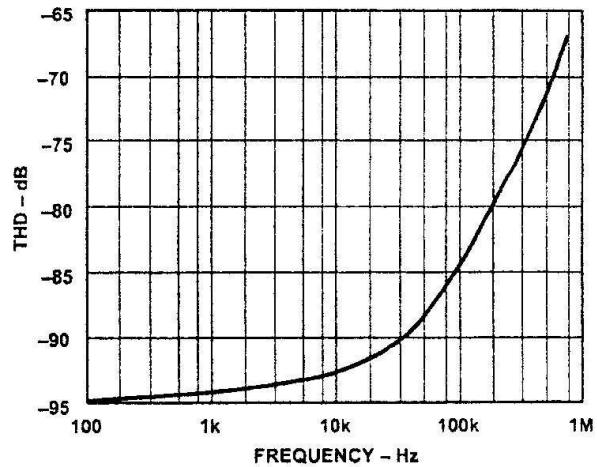


Figure 6. Total Harmonic Distortion vs. Frequency

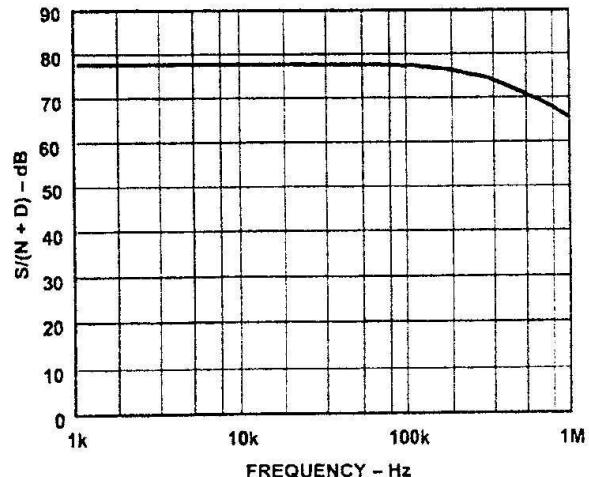


Figure 7. Signal/(Noise and Distortion) vs. Frequency

# AD783

## AD783 TO AD670 INTERFACE

The 15 MHz small signal bandwidth of the AD783 makes it a good choice for undersampling applications. Figure 8 shows the interface between the AD783 and the AD670 ADC, where the AD783 samples the incoming IF signal. For this particular application, the IF carrier was 10.7 MHz and the information signal was a 5 kHz FSK-modulated tone. The sample-and-hold signal is applied to the 8-bit AD670 ADC and then digitally processed for analysis.

The CLKIN signal is connected directly to the S/H pin of the AD783 and must comply with the acquisition and settling requirements of the SHA. A delayed version of CLKIN is applied to the R/W input of the AD670 in order to accommodate the hold-mode settling requirements of the AD783. The 10  $\mu$ s conversion speed of the AD670 combined with the 150 ns hold-mode settling time of the AD783 result in a total system throughput of 10.15  $\mu$ s.

By keeping the 10.7 MHz IF input to the AD783 at a low amplitude, 255 mV p-p, the resultant distortion and jitter-induced noise result in approximately 45 dB of dynamic range. The AD670 can be conveniently configured such that its full-scale input range is 255 mV in order to retain the full 8-bit dynamic range of the converter. The maximum sample rate of the AD670 is 10  $\mu$ s; therefore, to comply with the Nyquist criteria the maximum information bandwidth is 50 kHz.

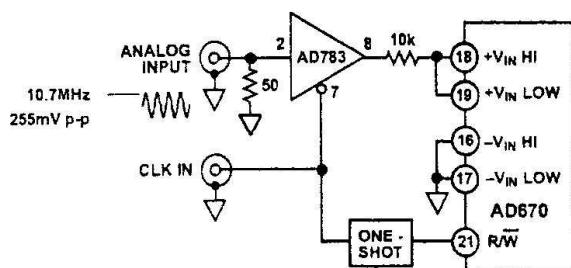


Figure 8. AD783 to AD670 Interface

## AD783 to AD671 (12-Bit, 500 ns ADC) Interface

The AD783 to AD671 Interface requires an op amp, a dual flip-flop, and a monostable multivibrator or "one-shot." The op amp amplifies the  $\pm 2.5$  V output of the AD783 to the full-scale input of the AD671. Appropriate op amps include the AD841 and AD845 (see the AD671 data sheet for additional information). The flip-flops and one-shot are used to generate the AD671 ENCODE pulse and the appropriately timed AD783 S/H pulse.

A master sampling clock is tied to the clock input of flip-flop1 and the input of the one-shot. The D1 input of flip-flop1 should be tied high and the one-shot should be configured to generate a pulse on a rising edge of the sampling clock. The rising edge of the sampling clock causes the Q1 output of the flip-flop to go low placing the AD783 into hold mode. Simultaneously, a low going pulse is generated at the one-shot output. The length of this pulse would usually be made long enough to allow the output of the AD783 to settle (hold-mode settling time), but because of the error-correcting ability of the AD671, the length of this pulse may be reduced to approximately 200 ns.

The low going one-shot output is connected to the clock input of flip-flop2. The D2 input of flip-flop2 is tied high. The rising edge of the low going pulse toggles the Q2 output of flip-flop2 to a high state. This output, which is tied to the ENCODE input of the AD671, initiates a conversion of the buffered output signal of the AD783. The AD671 issues the signal DAV when the conversion is complete. The DAV signal is tied to the asynchronous CLR1 and CLR2 inputs of both flip-flops. When DAV goes low, the Q1 output goes high returning the AD783 to the sample or acquisition mode. The Q2 output (ENCODE) returns low until it is again triggered by the rising edge of the one-shot output.

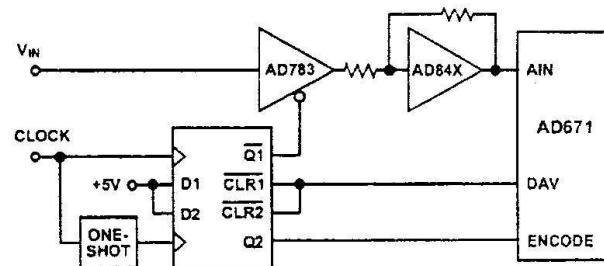
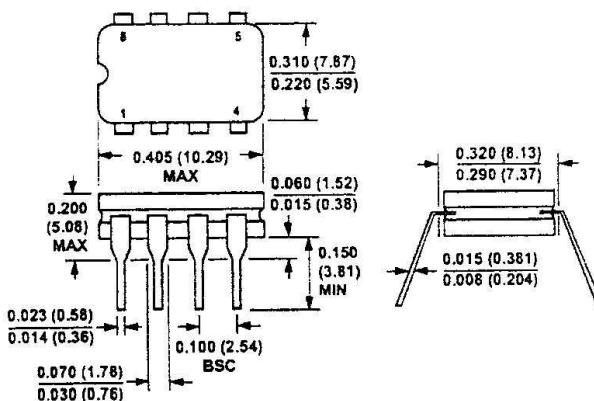


Figure 9. AD783 to AD671 Interface

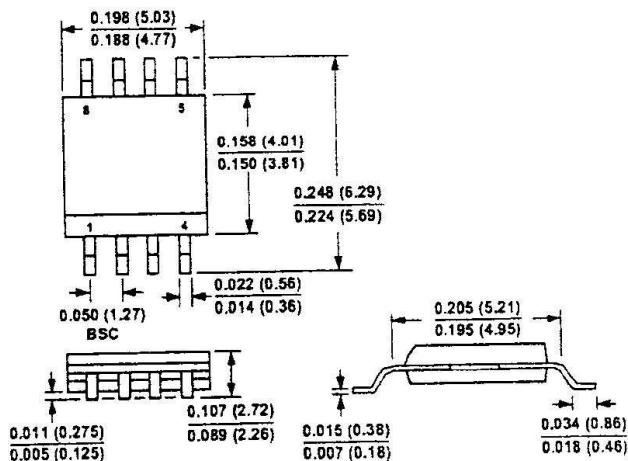
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Pin Cerdip (Q-8) Package



### 8-Pin SOIC (R-8) Package



PRINTED IN U.S.A.



# AAF-1

## 2 to 8 Channel Low-Pass Filter Card Series For PC/AT and Stand-Alone Data Acquisition Systems

### Features

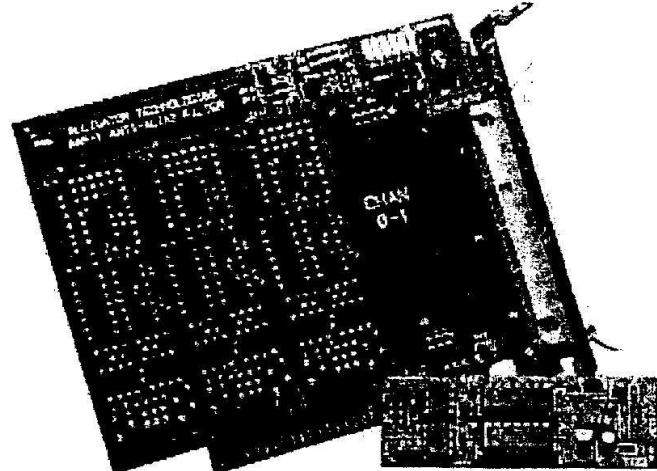
- 2, 4, 6, or 8 differential-input low-pass filter channels per card
- Variable cutoff frequency ranges between 0.1 Hz and 200kHz
- Choice of 8-pole Cauer, Bessel, Butterworth, high-speed Cauer, and linear phase delay filters
- $\pm 500$  Volt protected inputs
- $\pm 200V$  common-mode input
- CMMR 86dB typ.

The AAF-1 is a multi-channel low-pass filter board designed for use in front of 12-bit A/D converters. It protects and filters 2, 4, 6, or 8 differential analog channels. Each 2-channel pair is available with any one of 8-pole Cauer, Bessel, Butterworth, high-speed Cauer, or high-speed linear phase filters. The Cauer filter provides rapid attenuation of unwanted high frequencies (120 dB/octave), while only minimally affecting frequencies in the passband (less than 0.15 dB ripple).

The cutoff frequency of the AAF-1 is set by an on-board potentiometer, which sets the same cutoff frequency for all filters on the board. Optionally, the cutoff frequency can be controlled with an external clock source for tracking filter applications, very low cutoff frequencies, or other special purposes.

### Applications

The AAF-1 is ideally suited for removing unwanted higher frequency signals that can erroneously appear as lower frequencies below half the A/D sampling rate. This phenomenon, known as aliasing, cannot be removed with post-acquisition processing such as digital filters. The AAF-1 also is ideal for eliminating noise and interference introduced before the electrical signals from the sensors are digitized by the A/D board.



Filter Type	Strength/Weakness	Application
Cauer	Good passband flatness and low noise with sharpest cutoff	For frequency-domain applications requiring a sharp cutoff; also useful in the time domain
	Non-uniform group delay	
Bessel	Uniform group delay; lowest wideband noise	For time-domain applications requiring minimum distortion of rapid slope changes
	Drooping amplitude response in the frequency domain; gentler cutoff frequency	
Butterworth	Best passband flatness and very low noise	For frequency-domain applications requiring minimum noise or maximum passband flatness
	Non-uniform group delay (but more uniform than Cauer filters) and gentler cutoff slope	
High-Speed Cauer	Similar to Cauer with lower noise as well as higher cutoff frequency and higher stopband rejection	Similar applications to Cauer, but with a need for a cutoff higher than 50 kHz or a higher stopband rejection
	Non-uniform group delay (more uniform than Cauer)	
High-Speed Linear Phase	Highest maximum cutoff frequency; sharper cutoff than Bessel	For highest-speed applications, especially in the time domain
	Reduced I/O voltage limits $\pm 3V$ typ, $\pm 4.5V$ max for high-speed linear phase	

### Filter Characteristics

	Cutoff Frequency	Passband Gain (to 85% of fc)	Stopband Rejection	Attenuation Slope	Total Wideband Noise	Phase Match
Bessel	0.1 Hz - 33 kHz standard* (150:1) 0.1 Hz - 67 kHz modified (75:1)	**	84dB Typ.	45dB/octave Typ.	60 $\mu$ VRMS Typ.	1.2° Typ.
Butterworth	0.1 Hz - 50 kHz standard (100:1) 0.1 Hz - 100 kHz modified (50:1)	0dB + 0.15 - 0.5dB	90dB Typ.	48dB/octave Typ.	80 $\mu$ VRMS Typ.	1.2° Typ.
Cauer	0.1Hz - 50 kHz (100:1)	0dB ± 0.4dB	75dB Typ.	120dB/octave Typ.	165 $\mu$ VRMS Typ.	2.5° Typ
High-Speed	0.1 Hz - 50 kHz standard (100:1)	0dB - 0.5	90dB Typ.	90dB/octave Typ.	135 $\mu$ VRMS Typ.	1.0° Typ.
Cauer	0.1 Hz - 100 kHz modified (50:1)	+ 0.1 dB	90dB Typ.	90dB/octave Typ.	135 $\mu$ VRMS Typ.	1.0° Typ.
High-Speed	0.1 Hz - 100 kHz standard (50:1)					
Linear Phase	0.1 Hz - 200 kHz modified (25:1)	***	75dB Typ.	55dB/octave Typ.	175 $\mu$ VRMS Typ.	1.7° Typ.

NOTE; Please indicate cutoff frequency choice at the time the order is placed.

\* To 47 kHz below 55°C with external clock.

\*\* Bessel passband performance: Group delay approximately 1/2 of one cycle at fc, passband group delay variation <1%; amplitude 3 dB down at fc.

\*\*\* High-speed linear phase passband performance: Group delay approximately one cycle of fc; passband group delay variation < 2% max., 1% typ.

## Connector Pin Assignments

All I/O connections from the AAF-1 are made via a keyed 40-pin dual-row male connector that extends out of the rear of the computer.

SCF CLOCK	1	2	DIGITAL GROUND
FREQ IN	3	4	DIGITAL GROUND
ANALOG GROUND	5	6	CHAN 0 OUT HI
CHAN 0 OUT LO	7	8	CHAN 1 OUT HI
CHAN 1 OUT LO	9	10	CHAN 2 OUT HI
CHAN 2 OUT LO	11	12	CHAN 3 OUT HI
CHAN 3 OUT LO	13	14	CHAN 4 OUT HI
CHAN 4 OUT LO	15	16	CHAN 5 OUT HI
CHAN 5 OUT LO	17	18	CHAN 6 OUT HI
CHAN 6 OUT LO	19	20	CHAN 7 OUT HI
CHAN 7 OUT LO	21	22	ANA LOG GROUND
ANALOG GROUND	23	24	CHAN 7 IN LO
CHAN 7 IN HI	25	26	CHAN 6 IN LO
CHAN 6 IN HI	27	28	CHAN 5 IN LO
CHAN 5 IN HI	29	30	CHAN 4 IN LO
CHAN 4 IN HI	31	32	CHAN 3 IN LO
CHAN 3 IN HI	33	34	CHAN 2 IN LO
CHAN 2 IN HI	35	36	CHAN 1 IN LO
CHAN 1 IN HI	37	38	CHAN 0 IN LO
CHAN 0 IN HI	39	40	ANALOG GROUND

## Options

**Stand-alone System.** Up to 8 AAF-1 may be mounted in our AT-SYS400. This system provides power and a rugged chassis for the AAF-1.

**Screw Terminal Card.** The STA-AAF-1 provides screw terminals for connection of the customer wiring, a breadboard area, and a 40 pin I/O connector which is identical to the AAF-1 I/O.

**Custom Cable Accessories.** A variety of custom cable accessories, including twisted-pair ribbon cables and BNC connector boxes and cables, are available for connecting the AAF-1 to any A/D board.

## Specification

### Input Characteristics

Input impedance .....	800 k $\Omega$ differential, 400 k $\Omega$ common-mode
Differential Input Voltage .....	$\pm$ 5V
Common-Mode Voltage .....	$\pm$ 200V
Common-Mode Rejection .....	70 dB min, 80 dB typ
DC Offset.....	$\pm$ 30mV typ
Input Protection .....	Metal oxide varistor to ground (Common & Differential) .....
	( $\pm$ 250V to 350V)

### Output Characteristics

Load Resistance .....	2 k $\Omega$ min
Output resistance .....	50 $\Omega$
Linear Voltage Range .....	$\pm$ 5V

### Environment & Installation

Power Requirements .....	ISA bus power
Nominal Voltage .....	Maximum Load
+12V.....	30mA per filter channel
+5V.....	50mA
-5V.....	10mA
-12V.....	35mA per filter channel
Operating temperature.....	0°C to 70°C
Dimensions.....	5" (W) x 3.9" (H) (195mm x 100mm)

For more information, contact Alligator Technologies or your local Alligator Distributor

**Alligator Technologies**

2183 Fairview Ave., Suite 220 • Costa Mesa, CA 92627 USA Tel: 949-515-1400 • Fax: 949-515-4724 info@alligatortech.com • www.alligatortech.com