Low Cost isoSPI Coupling Circuitry for High Voltage High Capacity Battery Systems

by **Jon Munson**

The isoSPI™ feature built into the LTC6804 battery stack monitor, when combined with an LTC6820 isoSPI communications interface, enables safe and robust information transfer across a high voltage barrier. isoSPI is particularly useful in energy storage systems that produce hundreds of volts via series-connected cells, which require full dielectric isolation to minimize hazards to personnel.

In a typical isoSPI application (Figure 1) pulse transformers provide the dielectric isolation and reject common-mode interference that can be impressed on the wiring. The isoSPI function operates with readily available and inexpensive Ethernet LAN magnetics, which typically include a common-mode-choke section (as shown in Figure 1) to improve common-mode line noise, along with the usual 100Ω line termination resistors and common-mode decoupling capacitors.

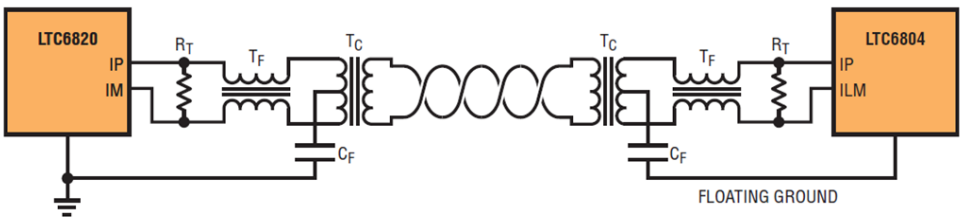

Figure 1. Generalized isoSPI point-to-point link.

Ordinary signal transformers, including Ethernet and gate-driver types, are wound with enameled wire that can have pin-hole sized insulation defects, which expose the copper to the atmosphere, inherently limiting the inter-winding bias that for which such transformers are certified. Such units are tested in production with high potential (called hi-pot screening) to identify gross insulation problems, typically with 1.5kV. This is established as a safe design margin for long-term bias of 60V, since the tiny corrosion sites tend to require more than 60V to form conductive paths between windings.

Problem: High Voltage = High Cost

For battery-stack voltages in the 400V range, good design practice is to specify transformers with reinforced (double) insulation and hi-pot testing to 3750V or higher. Such transformers are difficult to find as small parts due to the creepage (surface distance) and clearance (air spacing) dimensions required, and they are relatively expensive. isoSPI is applied in battery systems up to 1kV, which requires transformers with hi-pot testing to 5kV for conservative design margin. At this level, isolation components can become bulky, costly, and compromise pulse fidelity.

Solution: Divide and Conquer

One alternative to using reinforced transformers is to separate the bias requirement from the magnetics by moving the extra insulation to coupling capacitors instead. While capacitors alone could provide a seemingly complete isolation option, they offer neither common-mode rejection nor the shock-resistant

isolation characteristics that transformers offer, so an L-C approach is actually optimal. In this way capacitors charge to the nominal DC bias and leave the transformer to handle transients, for which even ordinary units are well suited.

The coupling capacitors are biased by high value resistors, generally tied to the transformer center-tap connection, as shown in Figure 2. As a bonus, if the DC current of the biasing resistors is monitored, then any dielectric breakdown becomes a detectable fault. The resistance is chosen to be a high value, like 10MΩ, so that fault currents are within the fine wire rating of the transformers and the shock hazard to personnel is minimal.

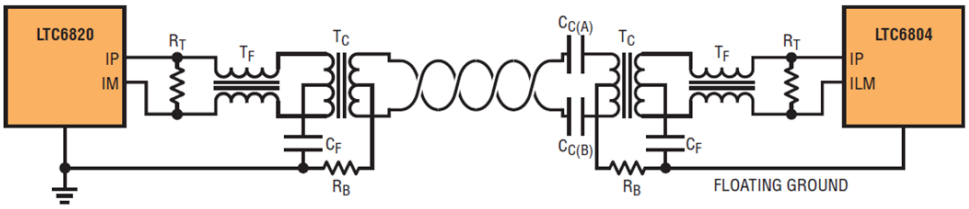

Figure 2. AC-coupled isoSPI point-to-point link for increased voltages.

Eliminating the high voltage requirement from the transformer magnetic design enables a number of relatively low cost options. One is to simply use appropriately approved Ethernet transformers. Another is to use other off-the-shelf low profile magnetics to reduce component height and part mass (reducing solder fatigue issues). These can be installed via surface-mount automated assembly methods like any other part, reducing production costs. A good candidate with these features is the discrete common-mode-choke (CMC), a transformer structure that is ordinarily used as a filtering element. Such parts are available up to 100µH and carry approvals for use with automotive systems, making them desirable for isoSPI configurations as well.

Suitable CMCs are inexpensive. They can be quickly and easily produced as a machine-wound wire pair on a chip-sized ferrite form. Although isoSPI designs require somewhat higher inductance to effectively pass the longer pulse waveforms, adequate inductance can be achieved by using two of the chokes with windings in series to produce 200µH. This has the additional benefit of forming virtual center-tap connections, which are useful for common-mode biasing and decoupling functions.

Figure 3 shows an equivalent transformer model realized with two CMCs. The chokes indicated have an 1812 SMT footprint and bifilar windings (wires paired in construction), so primary and secondary are intimately matched—minimizing the leakage inductance and thus preserving high frequency performance. Types with physically separated windings have poor pulse fidelity due to excessive leakage inductance. The units shown have a 50V DC continuous rating.

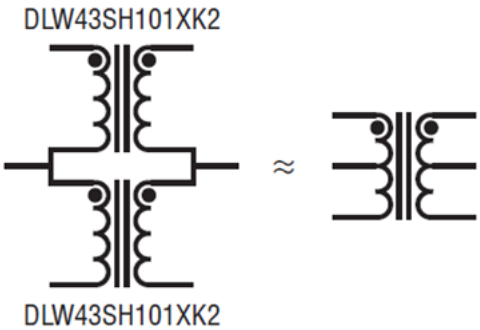

Figure 3. Using two common-mode-chokes as a center-tapped isoSPI transformer.

Complete the Picture

Figure 4 shows the complete circuit when using the L-C solution with CMCs as the transformers. Since the usual isoSPI application includes beneficial CMC filtering sections (integrated in the case of standard LAN parts), this circuit includes a recommended discrete part to retain that function. The coupling capacitors are high quality 10nF–33nF parts with an 1812 footprint (630V or 1kV rating). Here, we assume that the LTC6820 is operating at chassis ground potential, so that biasing of the twisted pair is at a safe level.

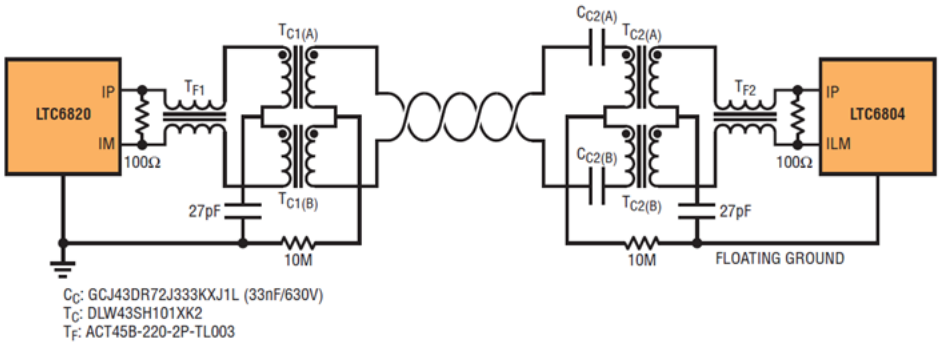

Figure 4. Complete high voltage isoSPI point-to-point link.

In situations where both ends of the pair are at floating potentials, as in links between daisy-chained LTC6804-1 modules, then capacitors can be used at both ends of the link and the pair itself can be biased to “earth” potential with high value resistors to each line as shown in Figure 5. Since the capacitors are in series in this situation, at least 22nF is recommended (33nF/630V type shown).

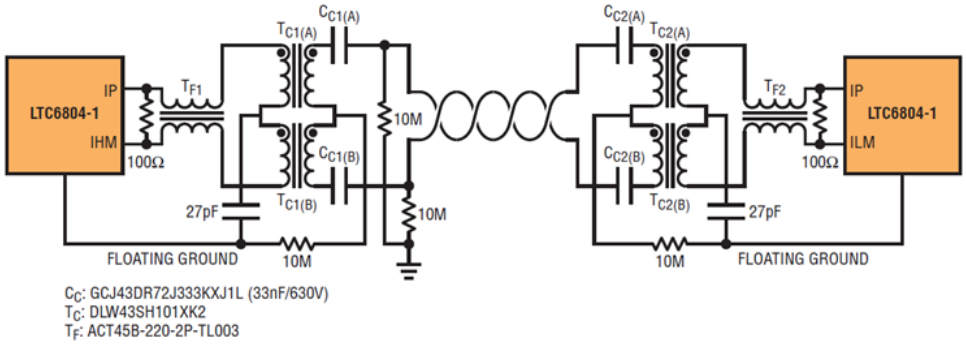

Figure 5. High voltage daisy-chain isoSPI link with isolated wiring.

Links between daisy-chained LTC6804-1s on the same board do not need any capacitor couplings since the potential is ordinarily < 50V, usually requiring only a single transformer section as well (Figure 6) since the noise ingress without a cable is far smaller.

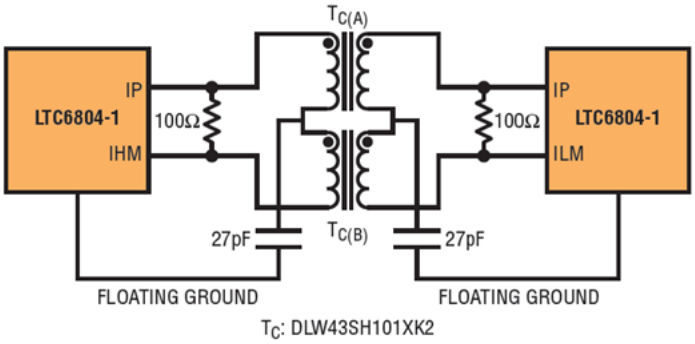

Figure 6. Daisy-chain isoSPI link for same-board interconnections.

High Voltage Layout

The printed circuit layout should include wide isolation spacing across the main dielectric barrier, namely, the capacitors. Figure 7 shows a placement example that provides good high voltage performance, with the blue regions representing frame ground (left side, with twisted-pair connector) and IC common (right side).

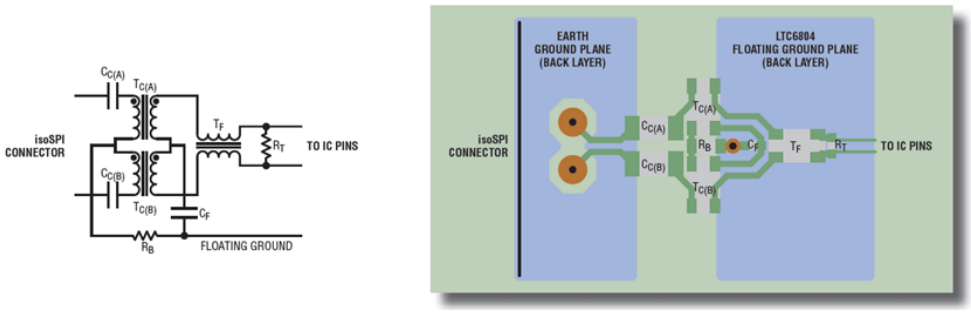

Figure 7. Suggested printed-circuit layout for high voltage performance at an isoSPI interface.

Note that the transformers must withstand HV transient potentials, so clearance is maintained there as well by using a 1206 size-biasing resistor. The HF decoupling capacitor and impedance termination resistor can be small parts (0602 size depicted).

Another good practice to avoid leakage current across the HV barrier is to suppress soldermask in the area of the HV components (parts over the “gap” between grounds). This facilitates effective rinsing of flux residue under the parts, and avoids moisture retention in the porous soldermask layer.

Special Considerations for an isoSPI Bus

The previous circuits apply to point-to-point isoSPI links, but one of the important cases for providing a high voltage solution is the bus-connected addressable LTC6804-2 with the twisted-pair link passing through each “tap” connection, as shown in Figure 8. The bus application places a high voltage requirement on every transformer since the same twisted-pair potential must interface with any voltage on the floating cell-stack.

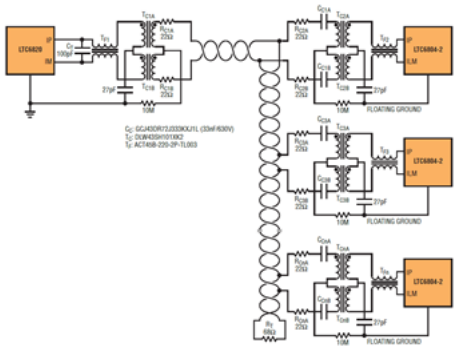

Figure 8. Complete high voltage isoSPI bus with echo control.

The use of the CMC and AC-coupling capacitors for added insulation is the same as previously described, but we suggest slightly different coupling circuitry to damp the multitude of reflections and provide a consistent wave shape for communicating devices irrespective of their physical position in the network. There are three differences:

- The LTC6820 termination is changed to a 100pF capacitor (C_T).
- Far-end termination is only applied to the live bus (R_T) and set to 68Ω (no termination at any of the LTC6804-2s).
- 22Ω coupling resistors (R_C) are used for all bus connections to decouple stray capacitive loading.

These are shown in the Figure 8 circuit, which again assumes the LTC6820 is operating at a safe "earth" potential. The modified waveforms are band-limited to control distortion from reflections, so the received pulses at the IC pins appear more rounded as in Figure 9, but the isoSPI pulse discriminator circuit works fine with this filtered shaping and supports a full sixteen address bus. Depending on actual losses encountered in a given system, it may be necessary to lower the pulse-detection thresholds for optimal operation (configure thresholds to be 40%–50% of the differential signal peak).

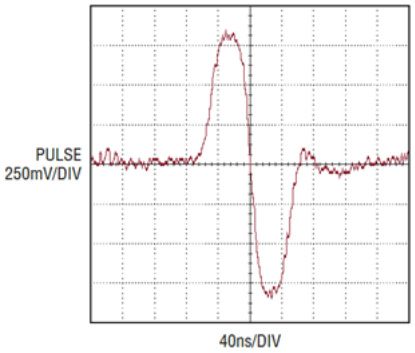

Figure 9. Modified pulse shaping for echo control in isoSPI bus applications.

Note that for networks of five or less addresses, the reflections are generally not a significant problem, so standard resistive end-terminations can be retained (namely 100Ω at the C_{TERM} and R_{TERM} positions of Figure 8, with the R_Cs omitted).

Conclusion

Use an AC-coupling method to mitigate the cost impact of high voltage isoSPI systems, eliminating the double insulation requirement on magnetics. Cost can be further reduced by replacing specialty toroidal transformer magnetics with inexpensive bobbin-wound common-mode-choke (CMC) components. Both

the capacitors and CMCs are relatively low profile surface-mount chip components that are competitively priced and available with automotive approvals for high reliability. The biasing resistors for the AC coupling offer a useful means of monitoring the dielectric integrity of the system.

Author

Jon Munson

Jon Munson is a senior applications engineer for Analog Devices, supporting their Signal Conditioning product line. Jon has a BS in electrical engineering and computer science from Santa Clara University. He has designed hardware for instrumentation, video, and communications products. Jon's hobbies include hi-fi audio, aviation and do-it-yourself projects, as time permits while raising his two daughters.