ME 3109: Measurement & Instrumentation

Azmir Hasan Mojumder
Lecturer

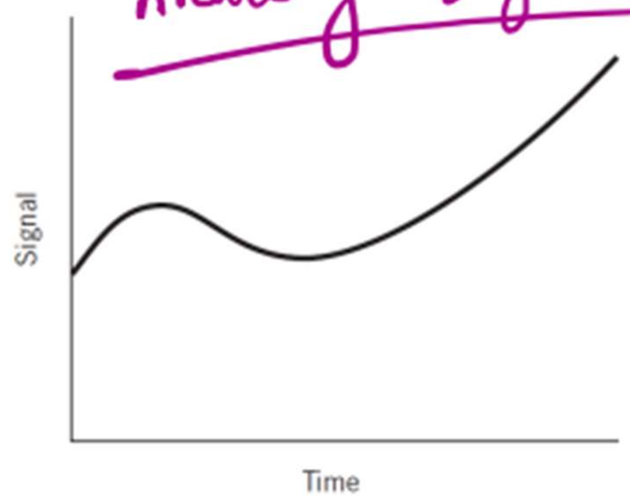
Department of Mechanical and Production Engineering
Ahsanullah University of Science and Technology

Topic_06: Data Acquisition System[1]	
1	Signals
2	A/D Conversion
3	D/A Conversion
4	DAS

[1] Figliola's "***Theory & Design for Mechanical Measurements***", 5th Edition

1. Signals

Analog signal



(a) Analog signal representation

(b) Analog display

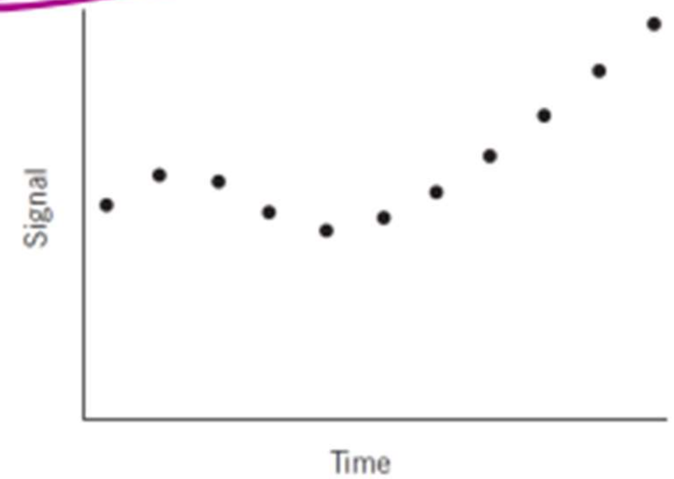
- Continuous in time
- Exact time dependent behavior
- most natural processes
- $\boxed{-10 \text{ to } +10\,V}$ or $\boxed{4 \text{ to } 20\ mA}$

Signals: They are defined by how they convey information

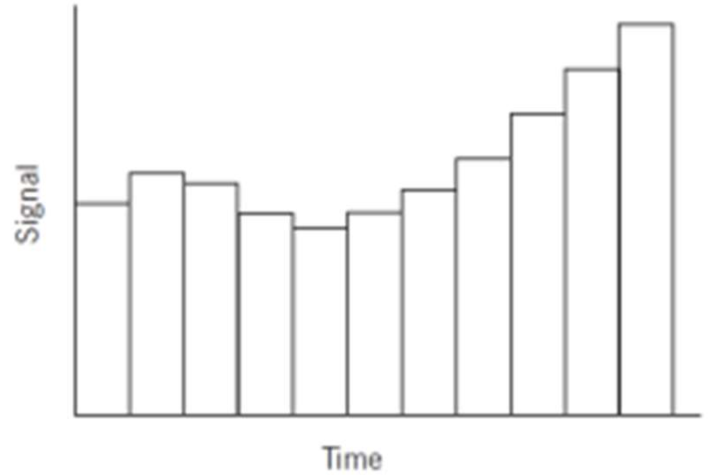
Amplitude, state, frequency, pulse width, phase ← useful!

1. Signals

Discrete Time Signal



(a) Discrete time signal

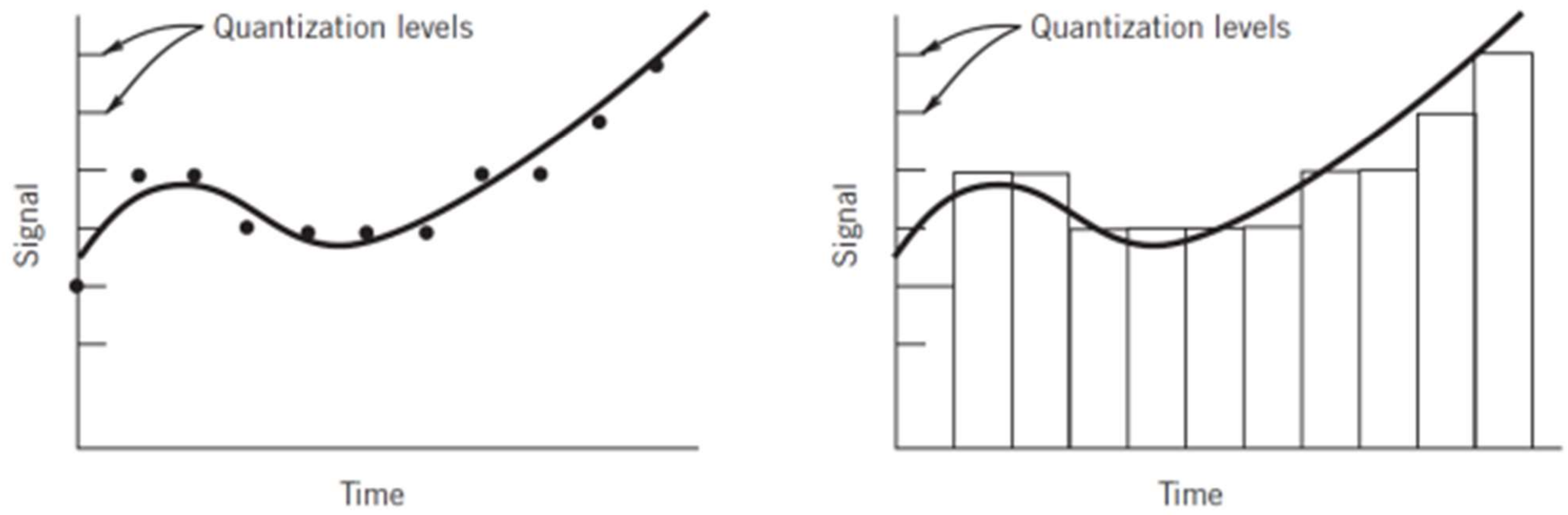


(b) Discrete time waveform

- Information available only at discrete time
- Results from sampling at repeated finite time interval
- No restriction on the amplitude of the signal

1. Signals

Digital Signal



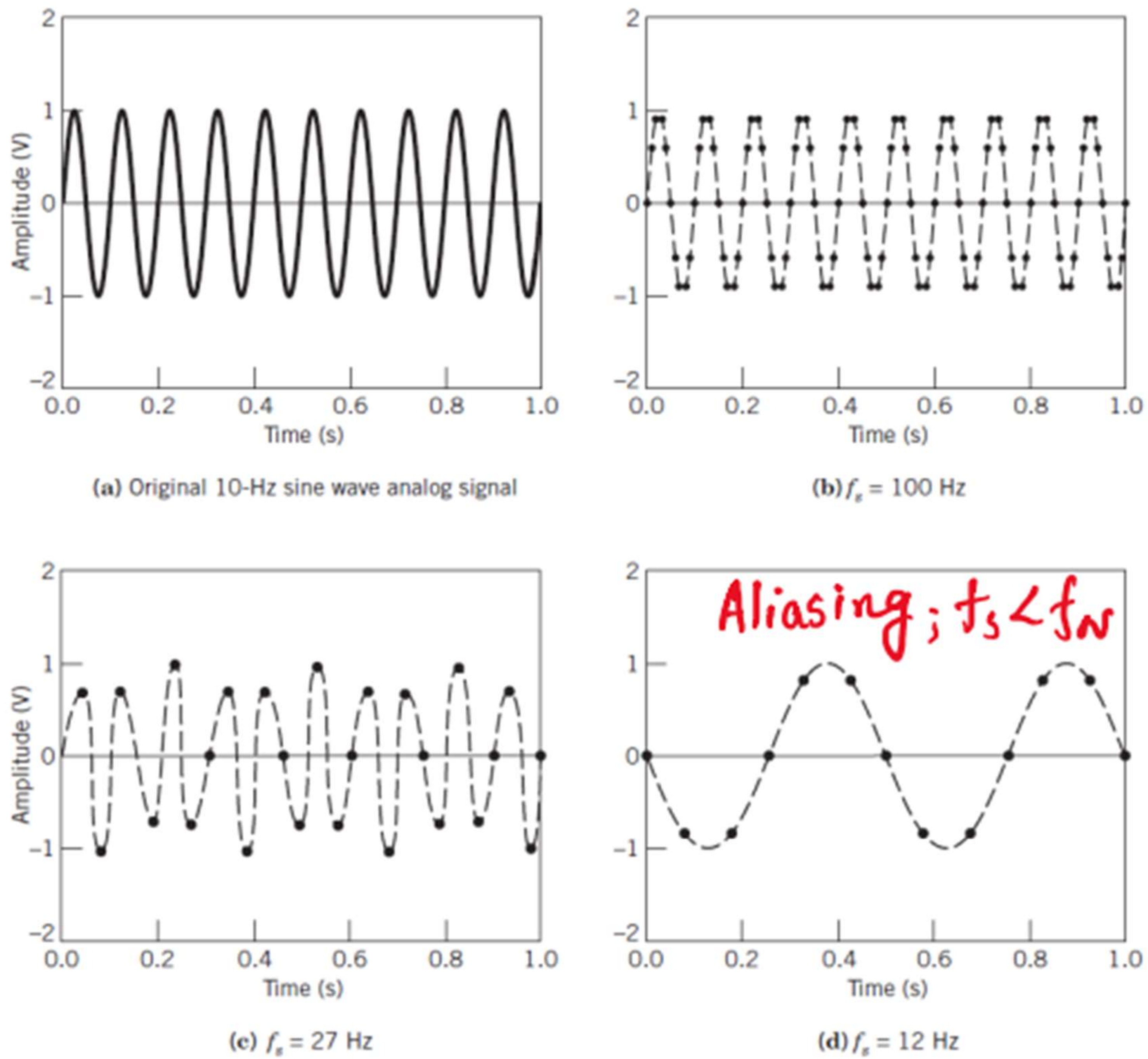
(a) Digital signal (b) Digital waveform

Sampling

- Discrete values in time
- Magnitude of signal is also discrete

Quantization

2. A/D Conversion Compromise



Sampling: Acquiring data at discrete intevals in time.

Sampling Rate: Shanon's sampling Theorem

$$f_s > f_N = 2 f_{max}$$

f_N → Nyquist frequency

$$\Delta t = \frac{1}{f_s}$$; time interval

2. A/D Conversion Compromise

ADC Process

Analog side
E_{FSR}

$\Rightarrow$

Digital side
M- bit Register

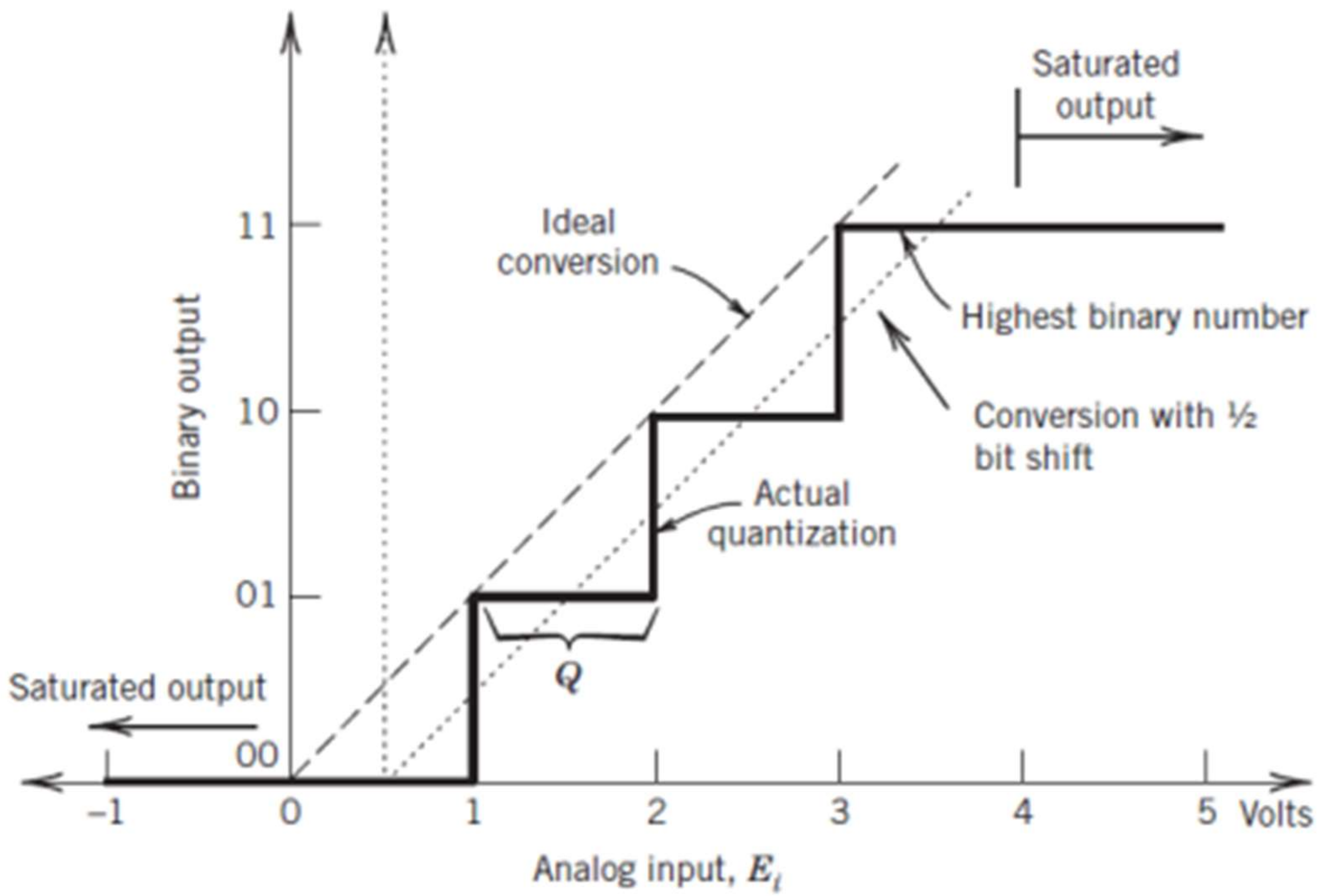
2^M - possible binary value

Resolution : Smallest voltage increment that causes a bit change.

$$Q = E_{FSR}/2^M$$

- Quantization error is the inherent uncertainty in the A/D conversion due to the finite resolution of the system

2. A/D Conversion Errors



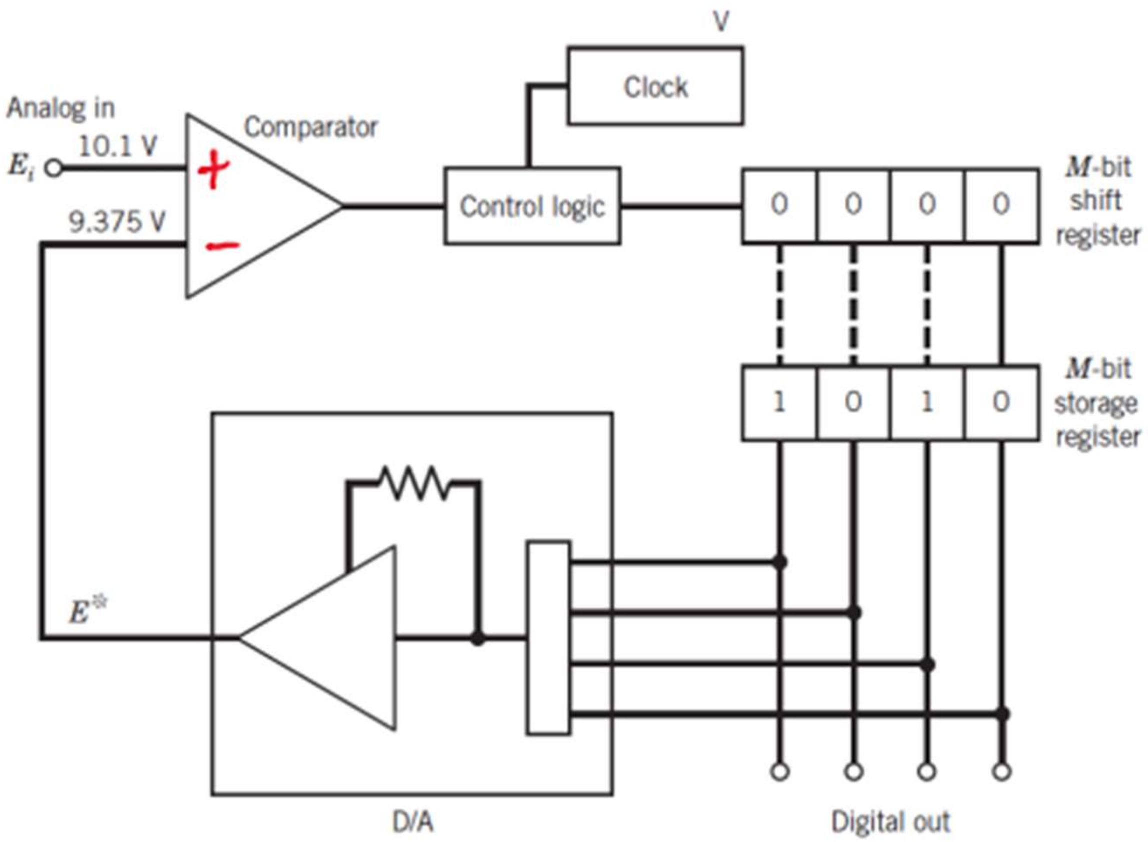
Bits M	Q^a (V/bit)	SNR (dB)
2	2.50	12
4	0.625	24
8	0.0390	48
12	0.00244	72
16	0.153 (10^{-3})	96
18	0.0381 (10^{-3})	108

[a]Assumes E_{FSR} = 10 V.

$SNR = 20 \log 2^M$ [dB]

* Saturation Error and Conversion Error

2. Successive Approximation ADC



Sequence	Register	E^*	E_i	Comparator
Initial status	0000	0	10.1	
MSB set to 1	1000	7.5	10.1	High
Leave at 1	1000	7.5		
Next highest bit set to 1	1100	11.25		Low
Reset to 0	1000	7.5	10.1	
Next highest bit set to 1	1010	9.375		High
Leave at 1	1010	9.375		
LSB set to 1	1011	10.3125	10.1	Low
Reset to 0	1010	9.375		

- 4-bit
- 0-15 V

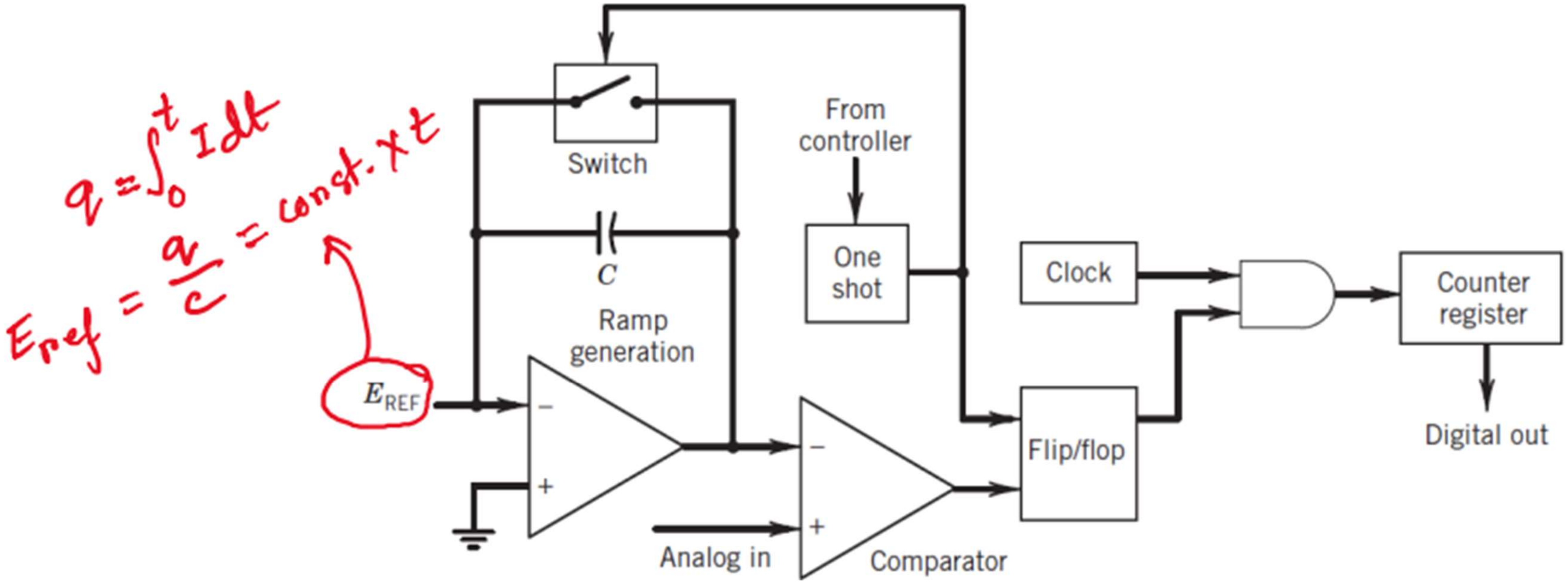
$$Q = \frac{15}{2^4} = 0.9375$$

$$1000 \rightarrow \underbrace{8 \times Q = 7.5\text{ V}}_{D/A}$$

* Typically used with a SHC

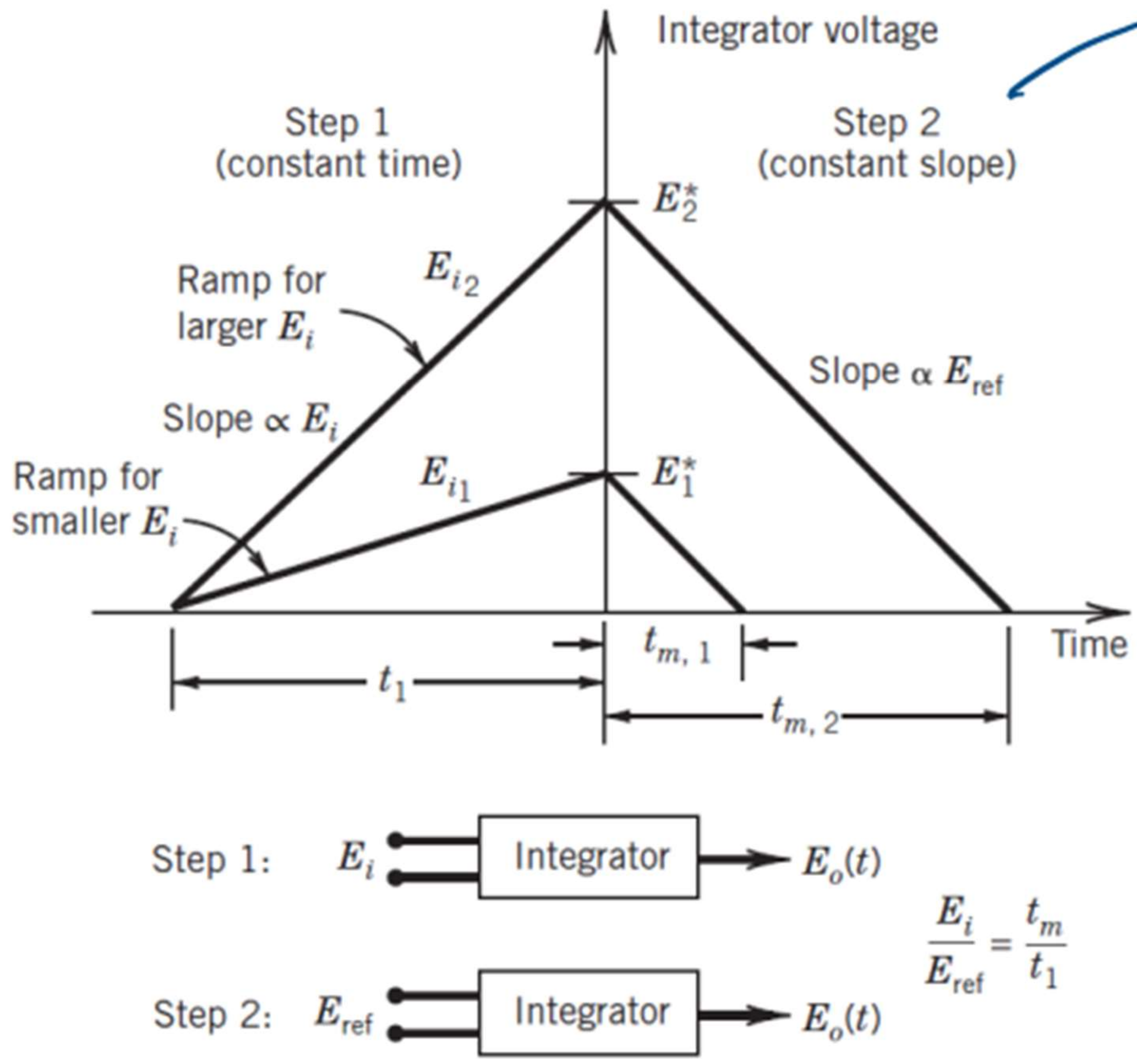
* Noise is main drawback

Ramp (Integrating) Converters



Time is integrated by a counter that increases the register value by 1 bit at each time step. Time step size depends on the value of 2^M. When the input voltage and ramp voltage magnitudes cross during a time step, the comparator output goes to zero, which flips a flip-flop halting the process. The register count value then indicates the digital binary equivalent of the input voltage.

Dual Ramp/Slope Integrating Converters



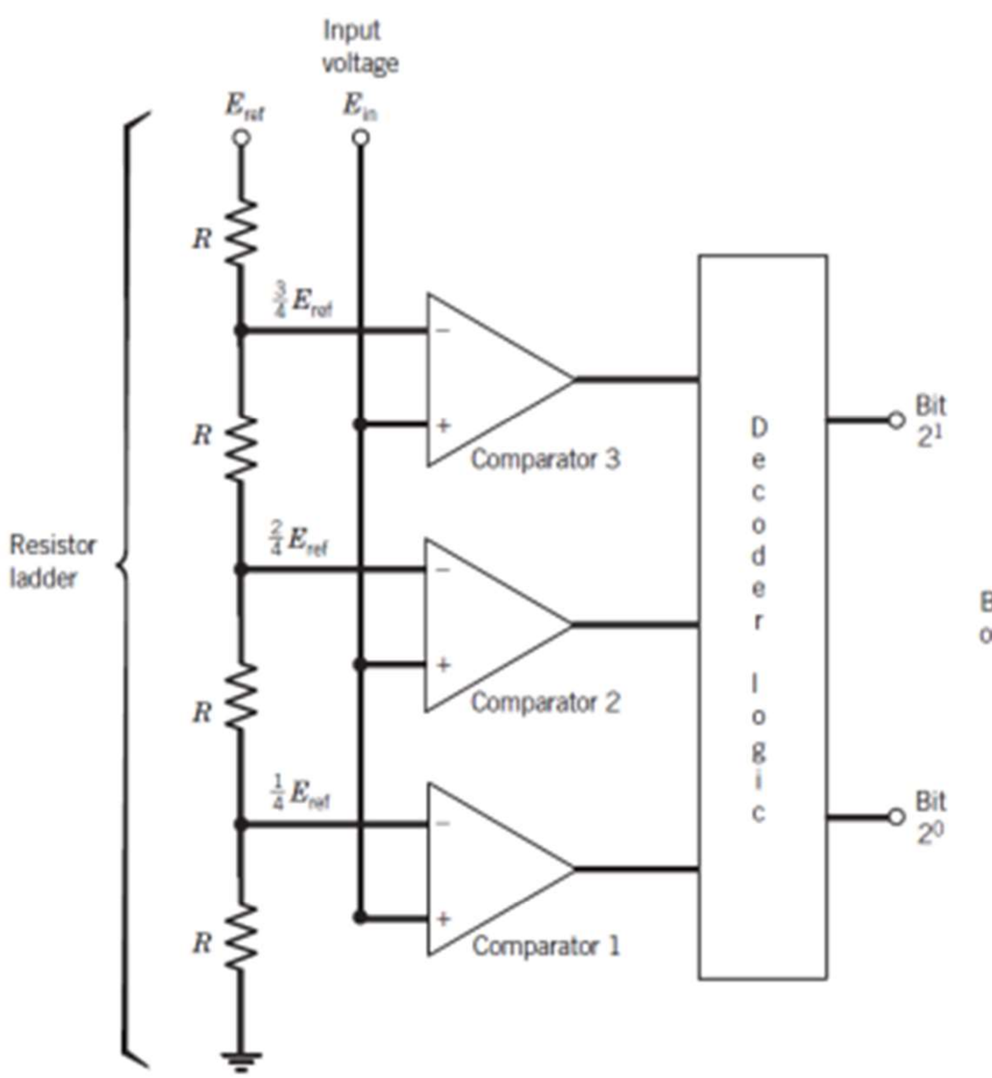
* Increased accuracy

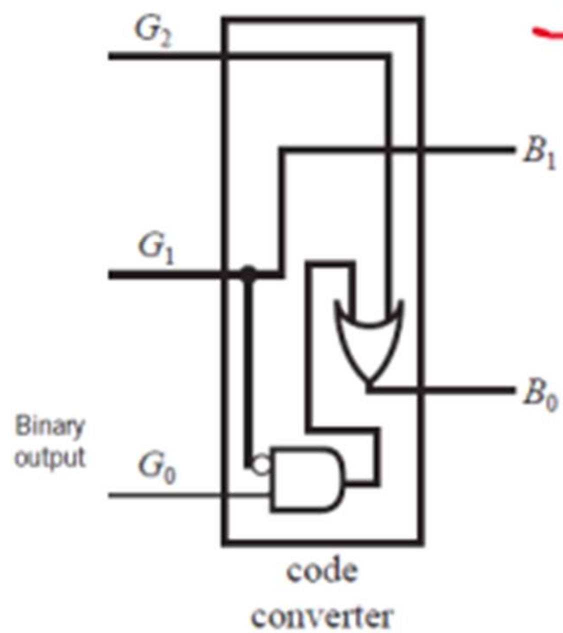
Ramp Converter Notes

* Slow
* Integration process average out noise
* Attractive for low-level signal

2. A/D Conversion

Parallel/Flash Converters





$$B_0 = G_0 \cdot \overline{G_1} + G_2$$

$$B_1 = G_1$$

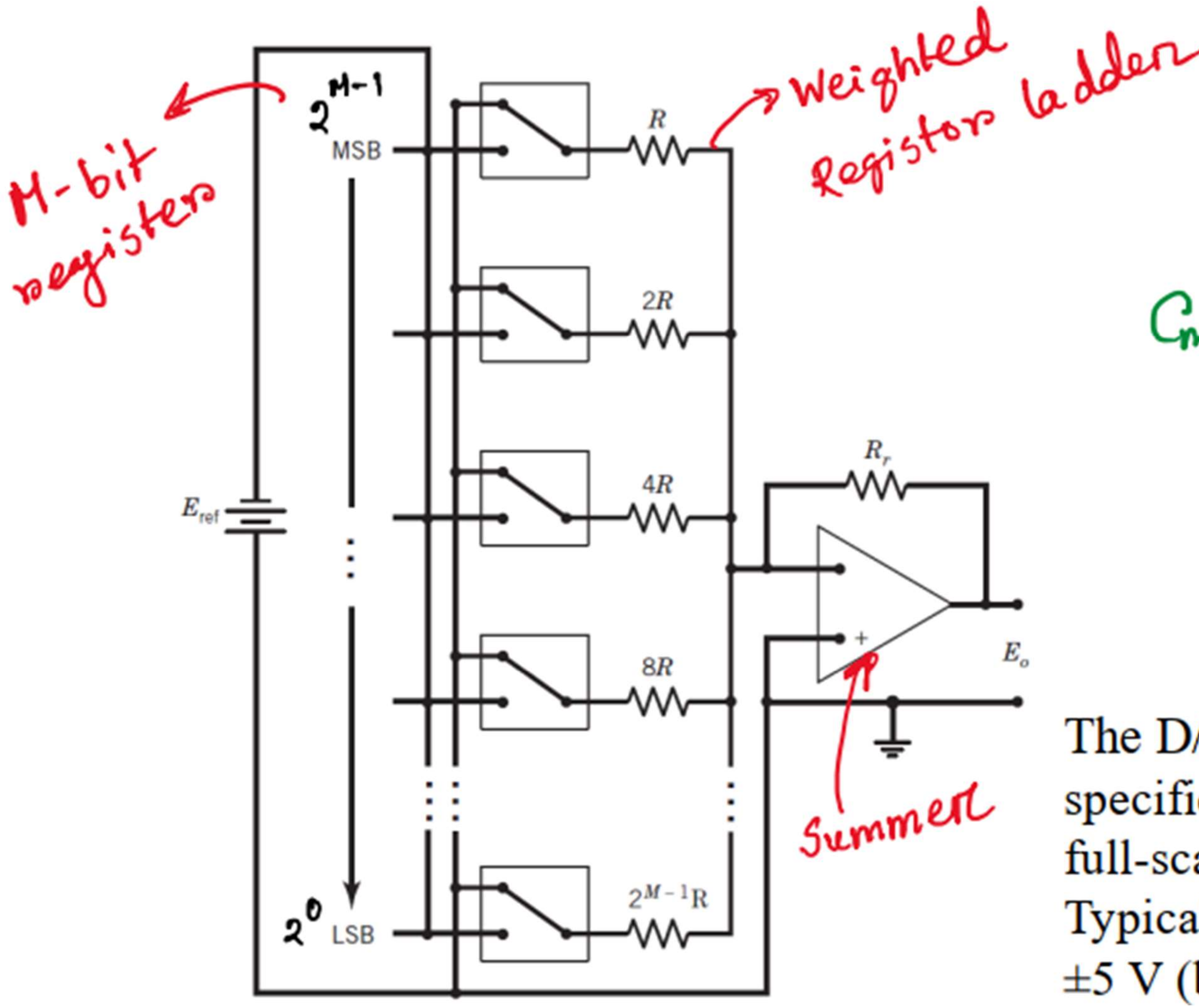
- Fast (Digital O-scope) but costly

2-bit Flash ADC

Comparator 1	Comparator 2	Comparator 3	Binary output
HIGH	HIGH	HIGH	11
LOW	HIGH	HIGH	10
LOW	LOW	HIGH	01
LOW	LOW	LOW	00

- $2^M - 1$ comparators
- 2^M different HIGH/LOW combination
- Logic circuits transfer this information to register

3. D/A Conversion



$$I = E_{ref} \sum_{m=1}^{M} \frac{c_m}{2^{m-1} R}$$

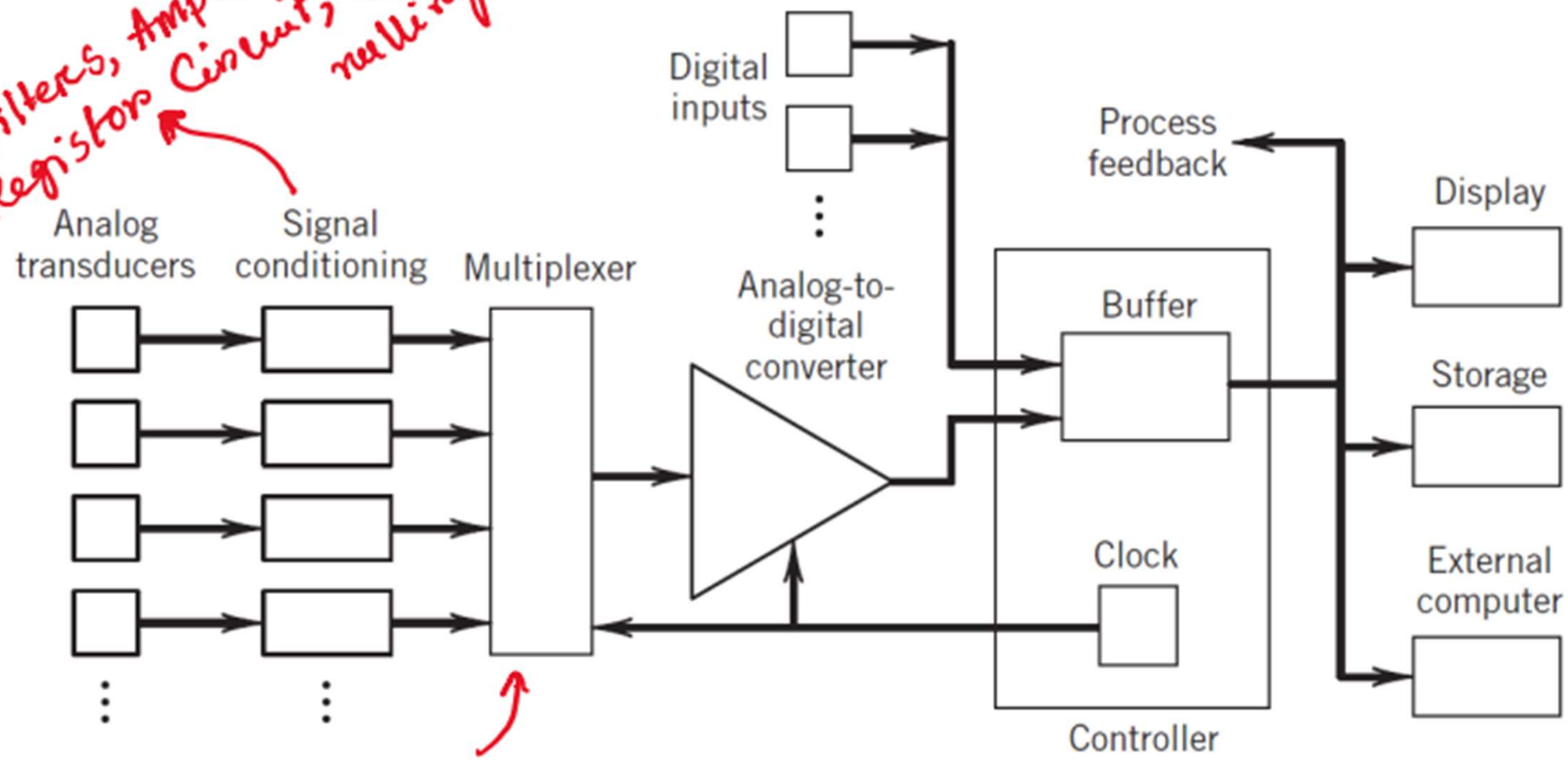
$c_m = 0$ or 1; depending on the mth bit value of the register

$$E_0 = I R_r$$

The D/A converter will have both digital and analog specifications, the latter expressed in terms of its full-scale analog voltage range output (E_{FSR}). Typical values for E_{FSR} are 0 to 10 V (unipolar) and ±5 V (bipolar) and for M are 8, 12, 16, and 18 bits.

4. DAS

Filters, Amplifiers,
shunt Registor Circuit, offset
nulling Circuit



Switching
between connections and A/D
converter one at a time

Reading

Theory and Design for Mechanical Measurements, 7th Edition, *Richard S. Figliola & Donald E. Beasley*

- ***Chapter 2***
  - ✓ *2.1, 2.2*
- ***Chapter 7***
  - ✓ *7.1-7.7*
  - ✓ *Example problem: 7.3, 7.4, 7.5, 7.6*

Thank you