Advanced Integrated Circuit Design Lab

Cadence Virtuoso Design Flow

Overview of the Design Flow

- Virtuoso Schematic Editor

- Virtuoso Symbol Editor

- Virtuoso Analog Design Environment

- Virtuoso Layout Editor

- Assura DRC

- Assura LVS

- Assura QRC

- Virtuoso Analog Design Environment

Overview of the Design Flow

Design Specifications

Schematic Capture

Create Symbol

Simulation

Layout

DRC – Design Rule Check

LVS – Layout versus Schematic Check

Extraction

Post-Layout Simulation

Tape-out

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