Advanced Integrated Circuit Design Lab

Cadence Virtuoso Tutorial – part 2

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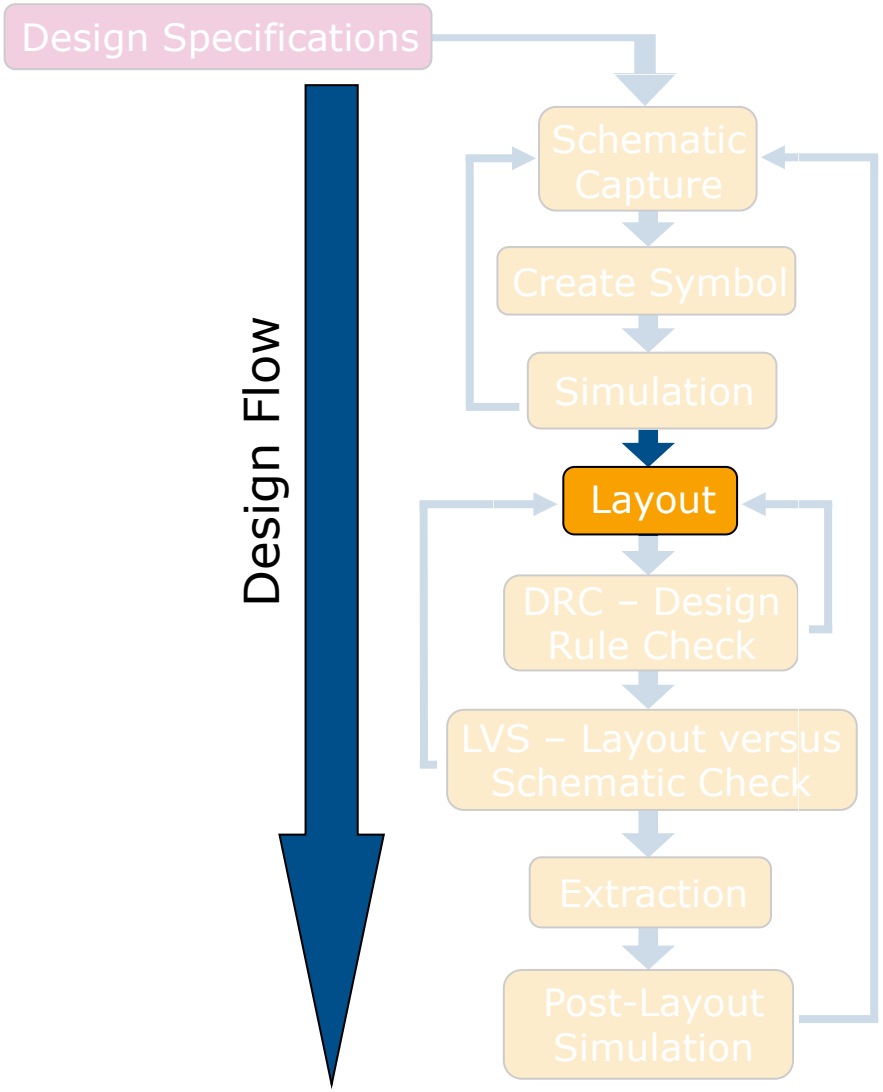
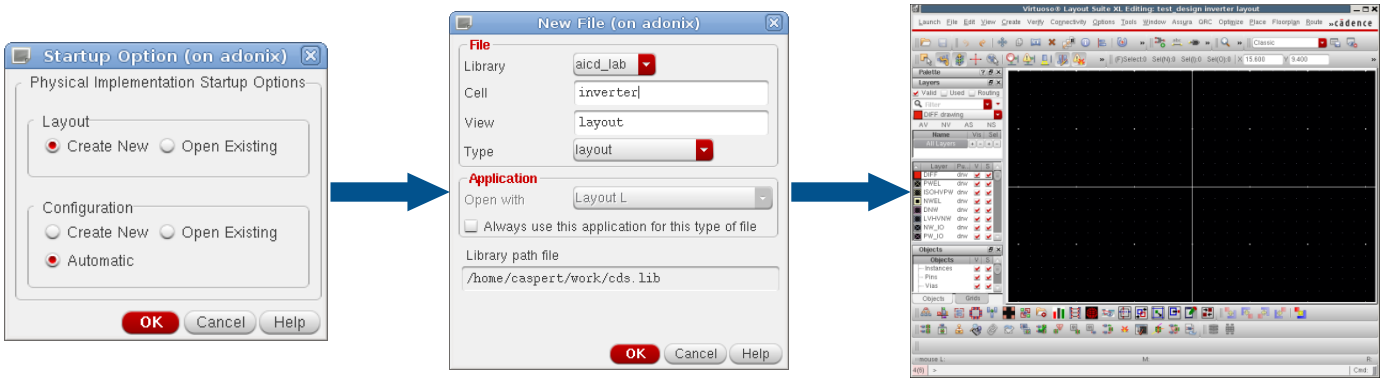
Overview of the Design Flow



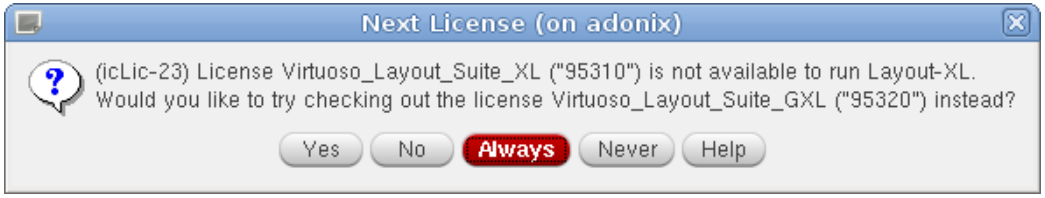
- Virtuoso Schematic Editor
- Virtuoso Symbol Editor
- Virtuoso Analog Design Environment
- **Virtuoso Layout Editor**
- Assura DRC
- Assura LVS
- Assura QRC
- Virtuoso Analog Design Environment

Layout Editing

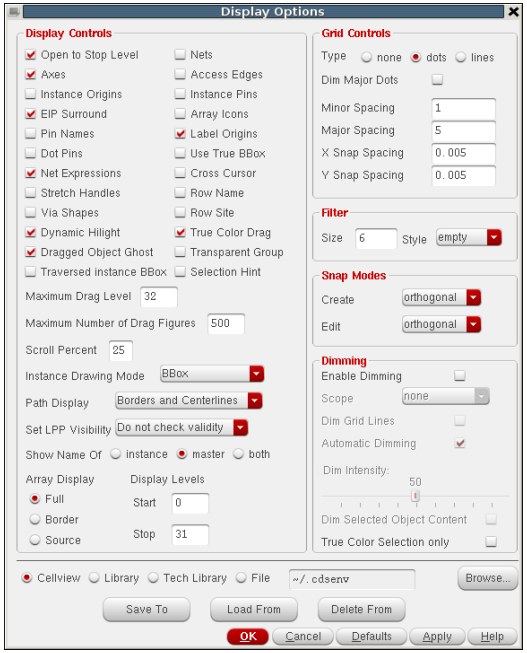
- To create a layout for the finished inverter, first open the schematic view of the *inverter*.
- Go to *Launch → Layout XL*. A small window appears (see upper left figure below).
- Select *Create New* and click *OK*. In the next window, make sure that *View* is set to *layout* and that the *type* is set to *layout*. Click *OK*.
- The Virtuoso Layout XL window appears (see bottom right). The Layers toolbar should also be available on the left hand side of the window. If it does not show up, go to *Window → Assistants → Layers* to activate it. This toolbar displays all the layers available in the *umc65ll* technology.

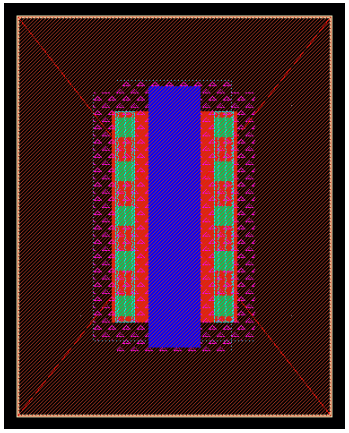


- In the case that a license error as shown below appears, don't worry and just click *Always*.



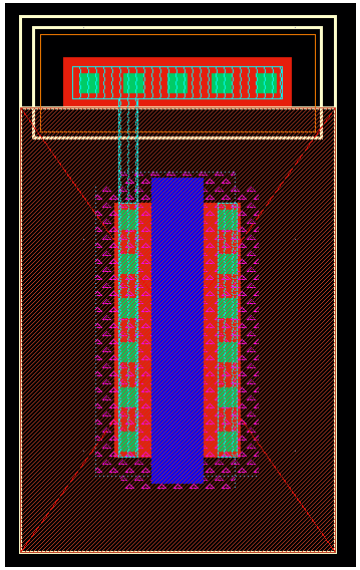
Layout Editing

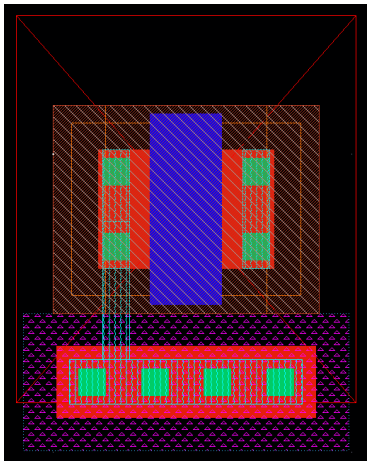




- In the *Virtuoso XL* window go to *Options→ Display* and set the *X Snap Spacing* to *0.005* and *Y Snap Spacing* to *0.005* (see on the top left). This will ensure that the minimum distance in the layout view is always *0.005µm = 5nm*, as required by the *umc65ll* design rules.
- Cadence offers parameterized cells for all the components present in *umc65ll*. Parameterized cells allow the user to create schematics and layouts at a higher level of abstraction. We will use the parameterized cells to create the layout.
- Create a layout instance of the transistor *P_25_LL* by using the keyboard shortcut *i* or going to *Create→ Instance*.
- In the *Create Instance* window use the *Browse* button to go to *umc65ll* library and select the *layout* view of the *P_25_LL* transistor. Click *Close* in the *Library Browser* window.
- In the *Create Instance* window enter the same values for *Length* and *Total Width* that you used in the schematic view of the inverter cell. Leave the rest of the values at their defaults.
- Click *Hide* and than place the layout of the PMOS transistor anywhere in the *Virtuoso XL* window (see on the bottom left).
- We can see the source and drain regions as well as the blue poly representing the gate (press *shift+f* and *ctrl+f* to switch between two levels of detail).

Layout Editing





- We also need a bulk contact to connect the *NWEL* layer of the PMOS transistor to a high voltage.
- Go to *Create → Via* or press *o* to open the *Create Via* window and select *Via Definition* as *M1_NWEL*. You can select the number of rows and columns that you want. Here we need only two columns, so select *Columns* as *5* since this fits nicely.
- Click *Hide* and place the *M1_NWEL* above the PMOS transistor in the layout.
- In the Layers toolbar, select the *ME1* layer with drawing as its purpose and then use a rectangle (go to *Create→ Shape→ Rectangle* or press *r*) in the *Virtuoso XL* window to draw a connection between the *M1_NWEL* and one of the contacts of the PMOS transistor. This connected contact is by this connection defined as the *Source*.
- Finally, surround the whole PMOS transistor and *M1_NWEL* via with an *NWEL* drawing layer from the *Layers* toolbar by again using a rectangle.
- The PMOS layout should look as shown in the top left figure.
- Repeat the above steps for the NMOS transistor *N_25_LL* with a *M1_PSUB.* However, do not use the *PWEL* drawing layer to surround the NMOS transistor. In the *umc65ll* technology, the entire area in *Virtuoso XL* is considered as a *PWEL* by default.
- The NMOS layout should now look like in the bottom left figure.
- Connect the two drains of the transistors using the *ME1* layer from the *Layers* toolbar. Also connect the two poly or gate regions of the transistors using the poly layer *PO1* from the *Layers* toolbar.
- Use the *Create → Via* window to create a contact *M1_POLY* from the poly layer *PO1* to the first metal layer *ME1*.

Layout Editing

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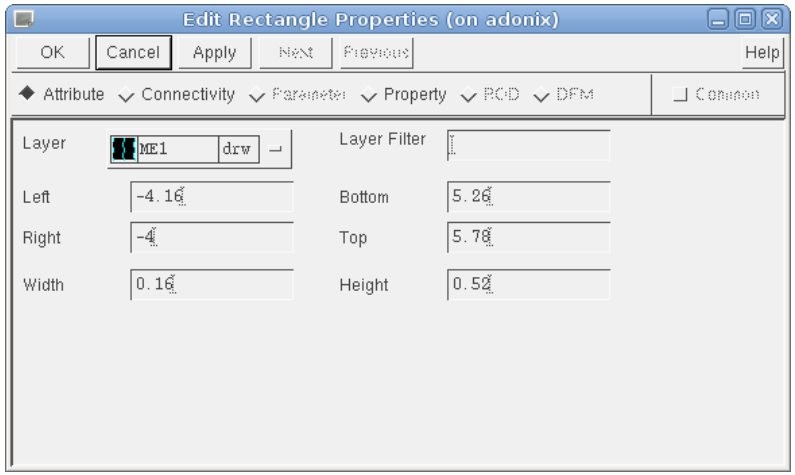
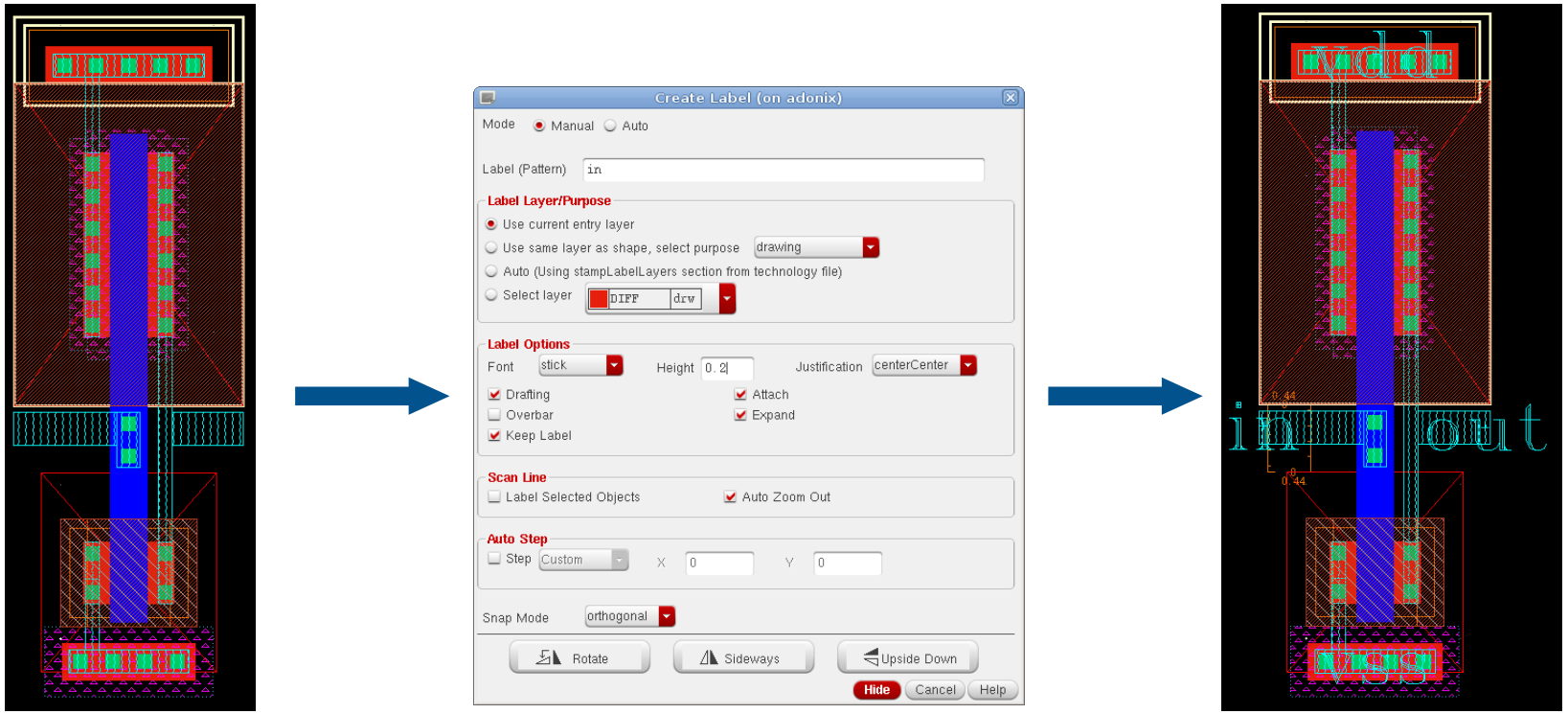
- To change the size of an already created object, there are two possibilities. The first option is to go to *Edit→ Stretch* or shortcut *s* and then use the mouse to change the size directly in the Virtuoso XL window. Regarding this approach, the stretch tool does not work like the click and drag method known from changing sizes of windows in operating systems. Instead, the click, move and click approach must be used here. The second and maybe more precise method is to go to the property window of the object (click the object and use the shortcut *q*) and change attributes like *Left*, *Right Bottom*, *Top*, *Width* and *Height*.

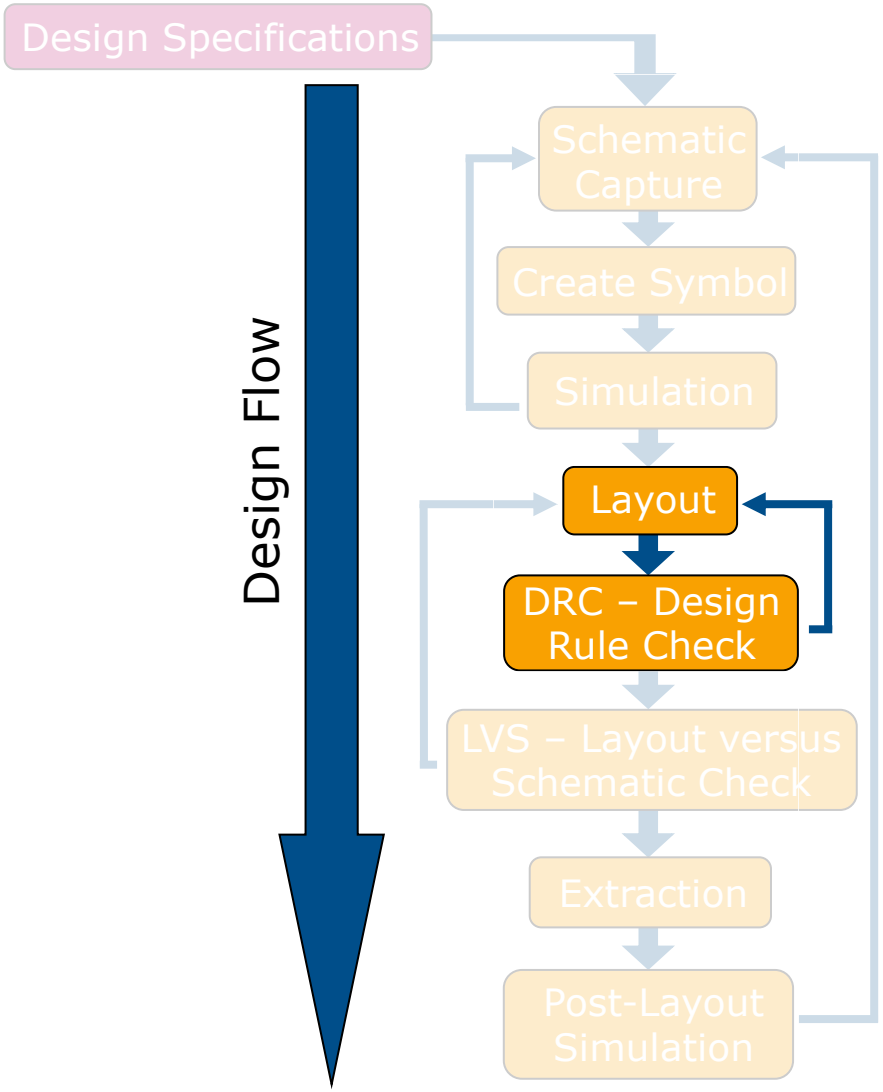


Layout Editing

- The layout should now look as shown in the bottom left figure.
- We need to annotate the schematic pins to the layout. To do this, select from the toolbar *Layers* the metal layer of each pin (in our case, *ME1*) and go to *Create → Label* (keyboard shortcut *l*).
- Set *Label (Pattern)* to *in*, *Height* to *0.2* and *Font* to *roman*. Then, attach the label to the *ME1* layer that corresponds to the input pin. Make sure that the center of the small cross corresponds to the desired metal region!
- Do the same for the *out*, *vdd* and *vss* pin labels. The result can be seen in the figure at the bottom right.



Overview of the Design Flow



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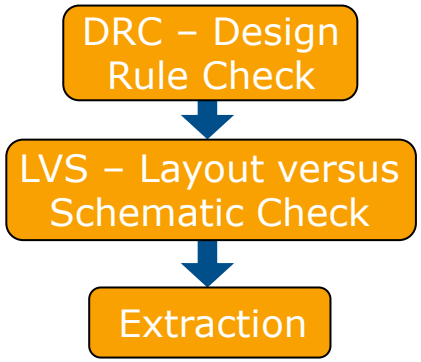
Design Flow at IES



- Assura DRC
- Assura LVS
- Assura QRC

HINT: At the IES institute, these steps are done on the **SERVER**. They might not work on the local machines.
When working remote, you are already on a server and do not have to worry.

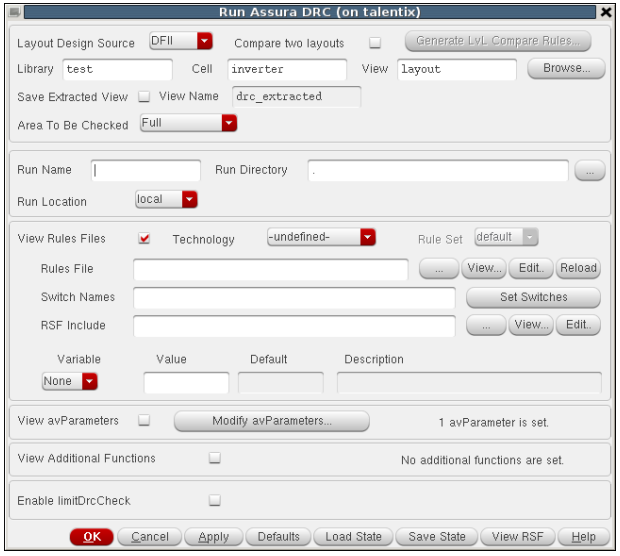
If you are working on the **local clients** (Computers at the lab), then you have to connect to a server:

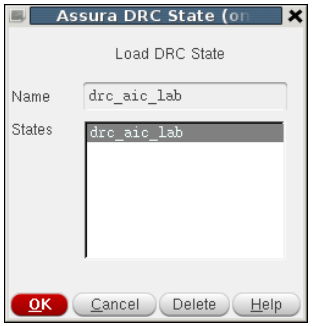
- Close your current Cadence session
- Open a terminal and enter *ssh –X amnesix*
- Confirm the connection and enter your password when prompted
  - Note: A linux terminal does not show any characters when typing your password
- Start Cadence inside this terminal as usual:
  cd /home/aicXX/AICD_lab_project and then *./start_virtuoso.sh*
  - Note: replace ## with your group number. Ex: cd /home/aic07 for group 07

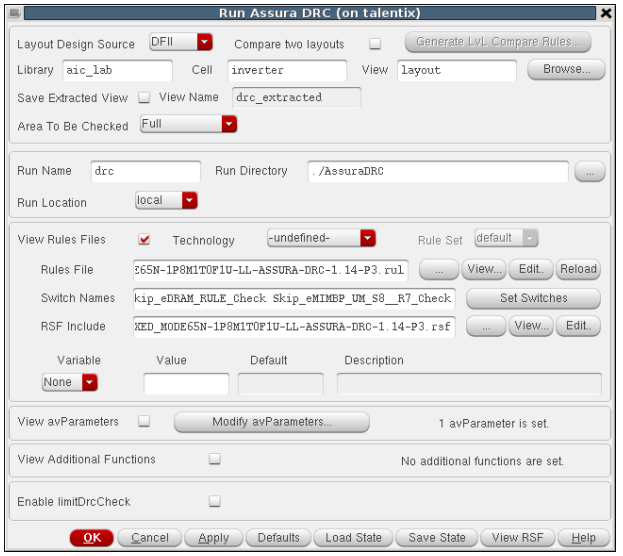
AVOID running a cadence session on the local machine and server concurrently. Make sure to close any cadence sessions that are open locally before switching to the server!

Design Rule Check (DRC)

- To perform the DRC, open the layout view of the cell. Then, go to *Assura → Run DRC*
- Load the preconfigured state by clicking on the *Load State* Button. Then select *drc_aic_lab* on opening window and click *ok*
- Make sure, that library and cell match with the design you are currently working. (right image, you will need to change the library name to your own library name [aicd_lab_##])
- Click *OK* and the DRC should run. A small progress window will appear, indicating that the drc is currently running. This can take some time, up to 5 min.

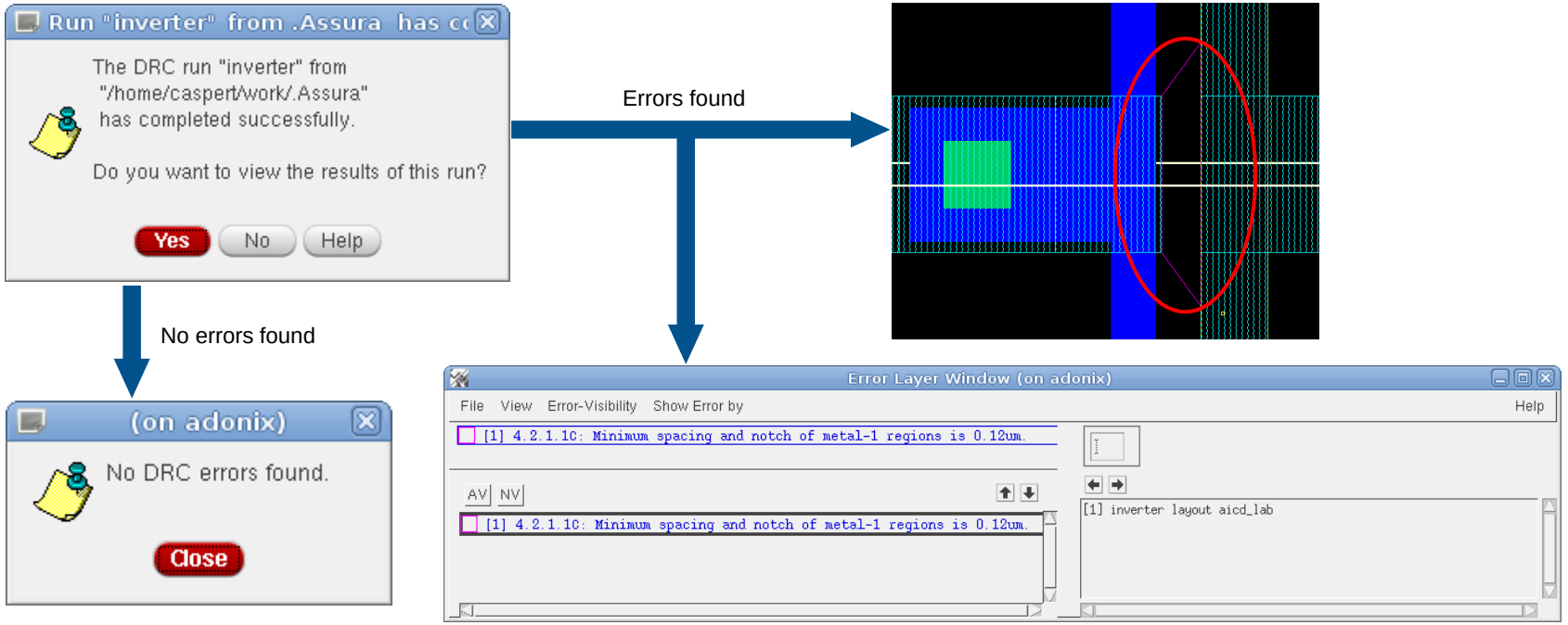




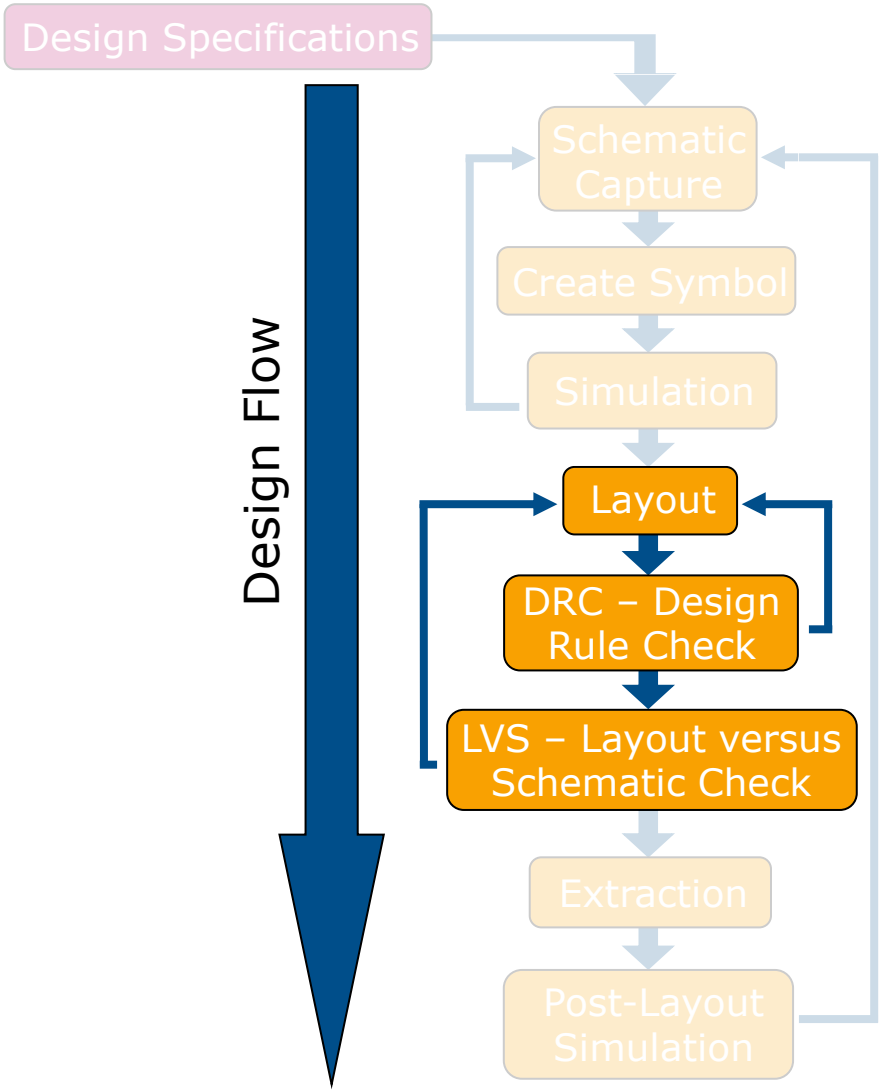


Design Rule Check (DRC)

- When the DRC run is completed successfully, you will get a window as shown below. Clicking *Yes* in this window will show you the results of the DRC run.
- If the DRC is completed successfully, you will see a window as shown below. Click *Close*.
- If the layout has errors, then DRC will show an *Error Layer Window* (ELW) as shown below. Selecting the DRC errors in the ELW and pressing *f* in the *Virtuoso XL* window highlights the respective errors.
- All errors must be corrected in the layout before proceeding to the LVS check!



Overview of the Design Flow



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Layout Versus Schematic (LVS)

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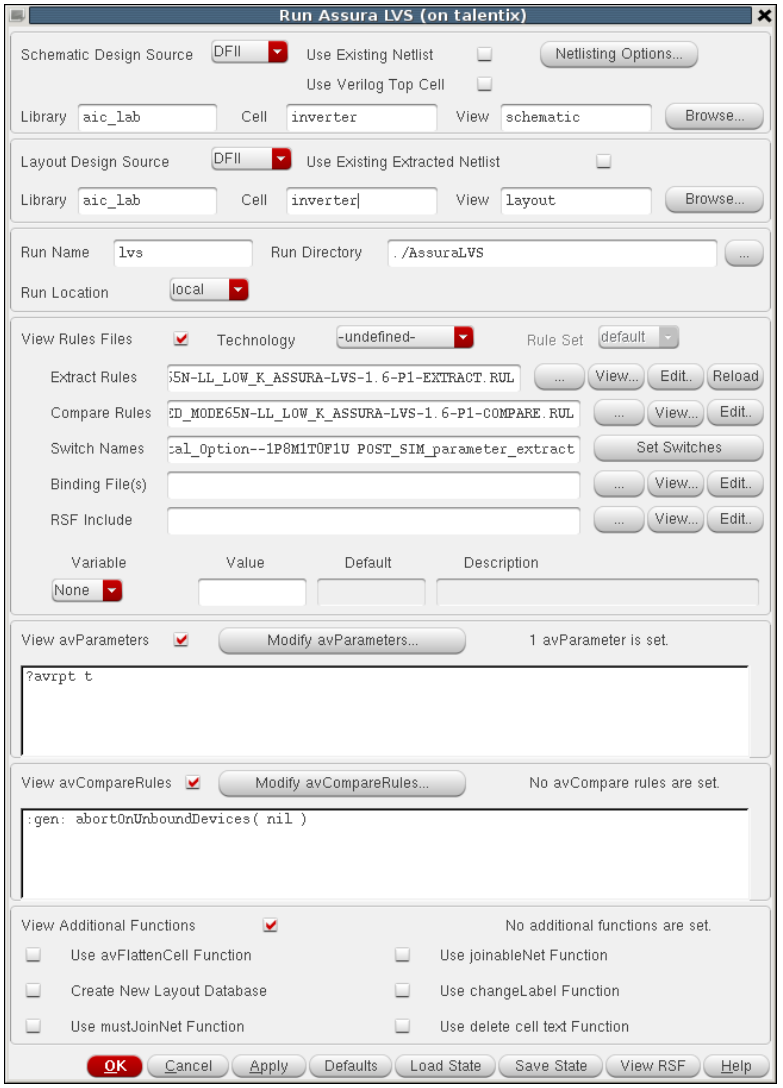
- To perform the LVS check, open the layout and go to *Assura → Run LVS*
- Load the preconfigured state by clicking on the *Load State* Button. Then select *lvs_aic_lab* on opening window and click *ok*
- Make sure, that library and cell match with the design you are currently working. (right image, you will need to change the library name to your own library name [aicd_lab_##])
- Click *OK* and the LVS check should run. A small progress window will appear, indicating that the lvs is currently running. This can take a couple of minutes.



Layout Versus Schematic (LVS)

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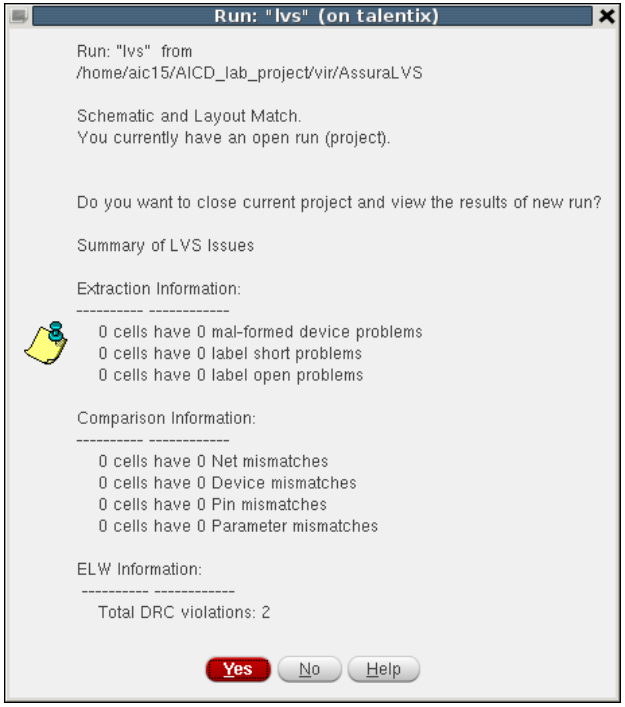
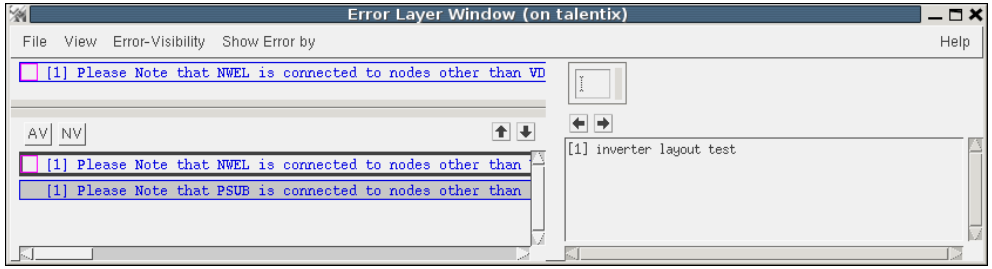
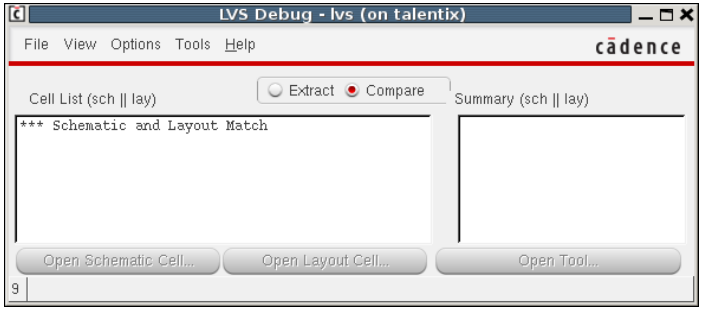
- On successful completion of the LVS run and if the layout and schematic match, you will get the window as shown below.
- Click *Yes* and the *LVS Debug* window opens. Here, you get the notification that schematic and layout match.
- Notice, two DRC violations are listed (left figure) and the error window will open (top right figure). If the error is identical, you can ignore this as it is caused by the net name configuration.

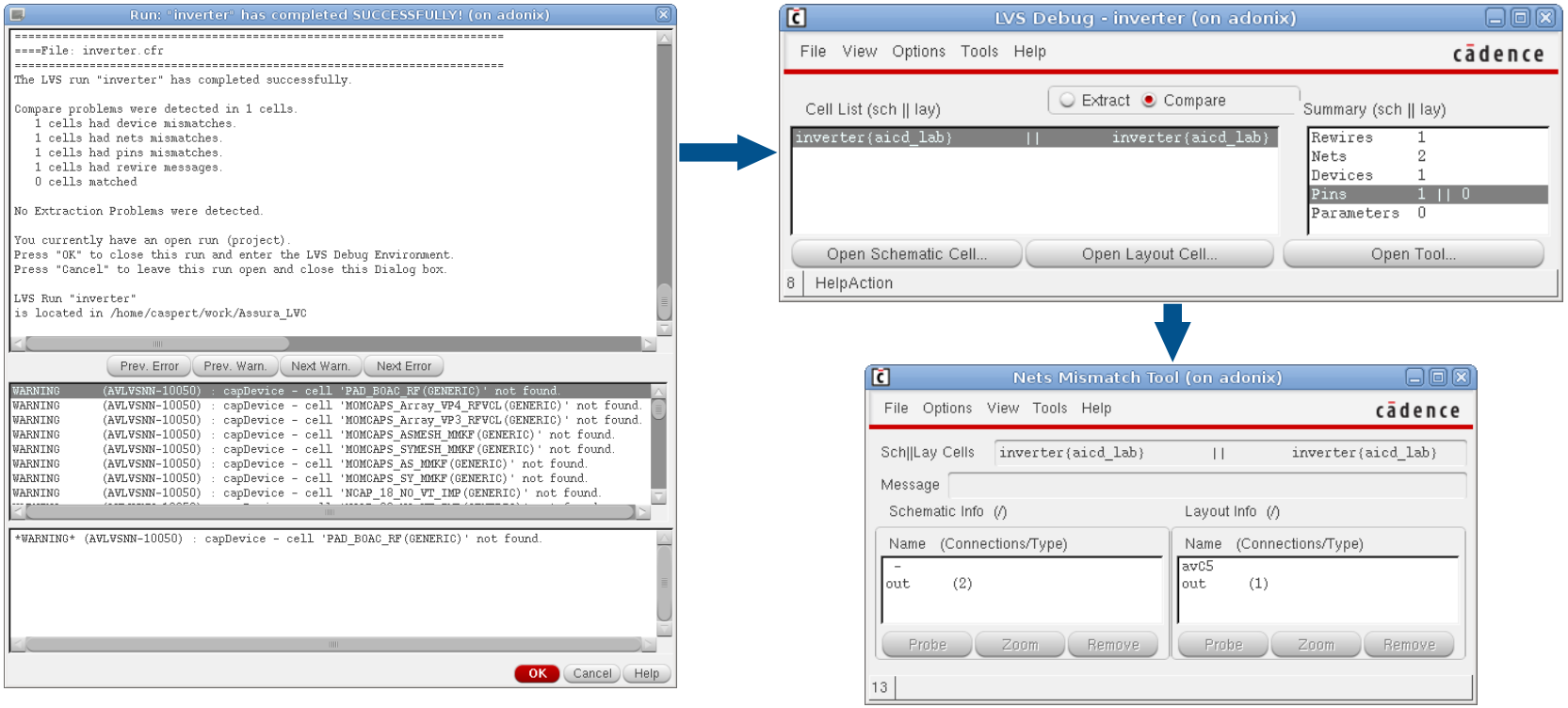




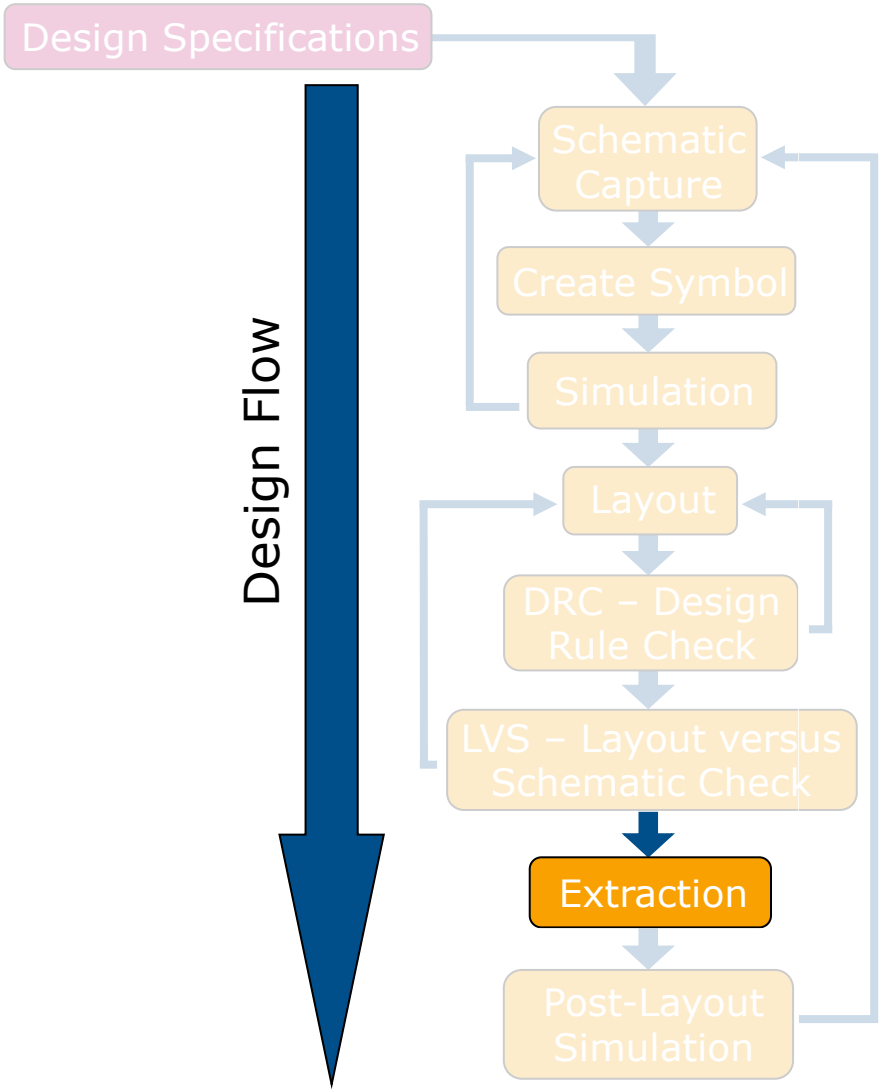


Layout Versus Schematic (LVS)

- If the layout and schematic do not match, then you will get a window as shown on the left.
- Click *OK* and you get the *LVS Debug* window, where the details of the mismatch can be seen.
- To access more information on a specific mismatch, select one of the entries of the *Summary* on the right hand side an press *Open Tool*.
- As for the DRC, all the LVS errors must be corrected before proceeding to the next step!



Overview of the Design Flow



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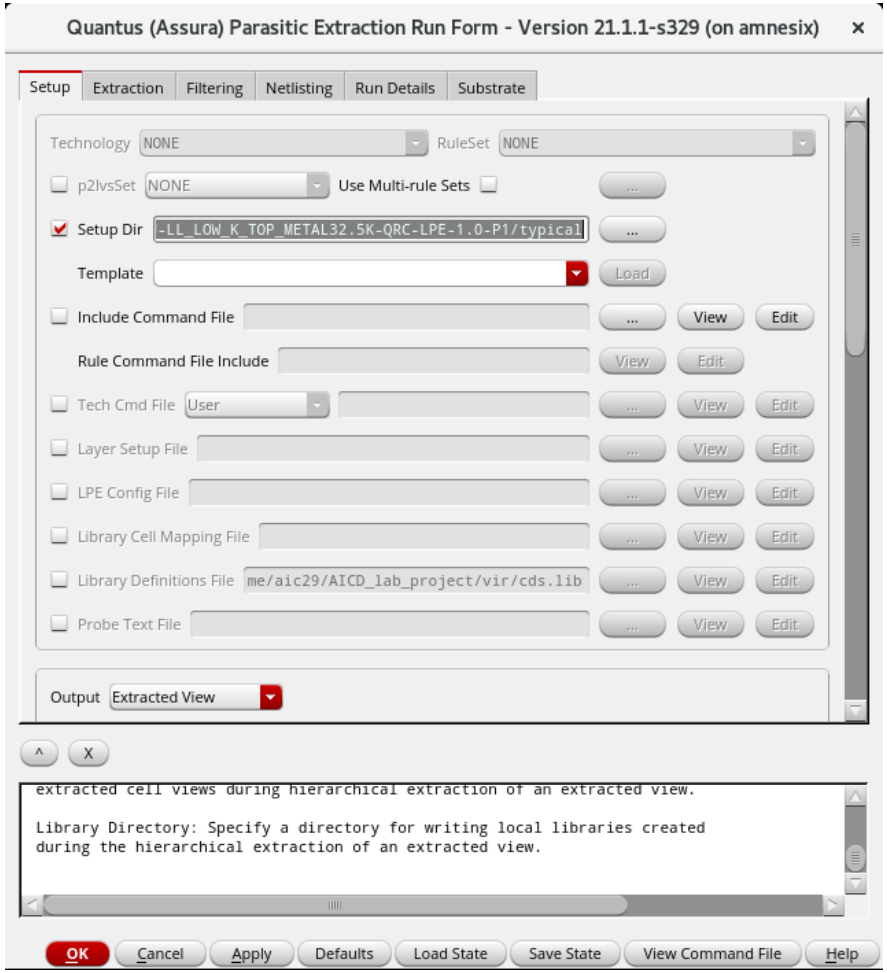
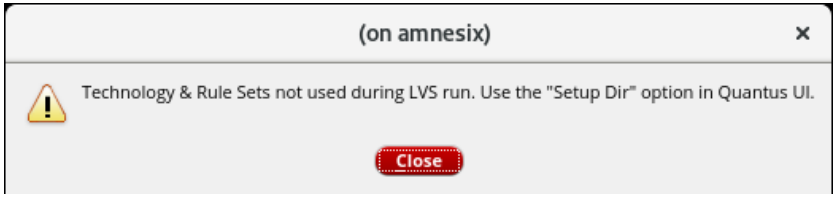
Parasitic Extraction

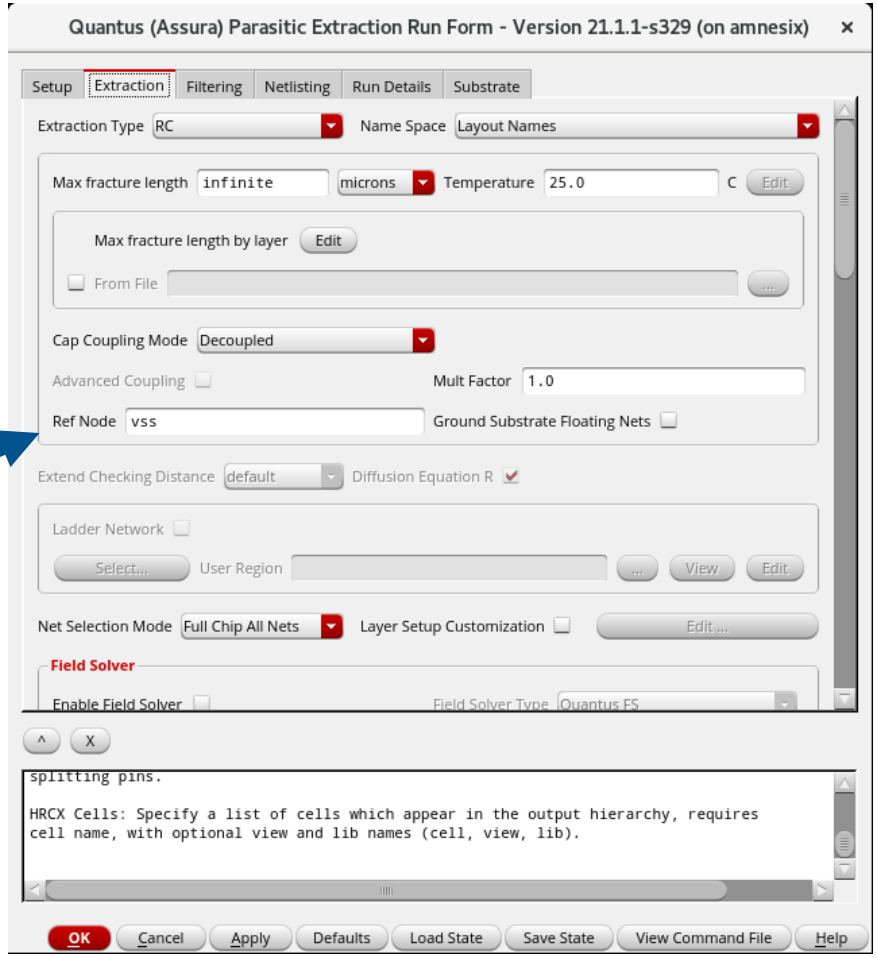
- After LVS check is successfully completed, go to *Assura → Run Quantus*
- *A setting window should appear* (right figure). If the window at the bottom figure appears, then click close and the setting window will open afterwards
- Load the preconfigured state by clicking on the *Load State* Button. Then select *qrc_aic_lab* on opening window and click *ok*
- Hint: If you experience any error/problems here, make sure that you have completed the LVS check without any errors!

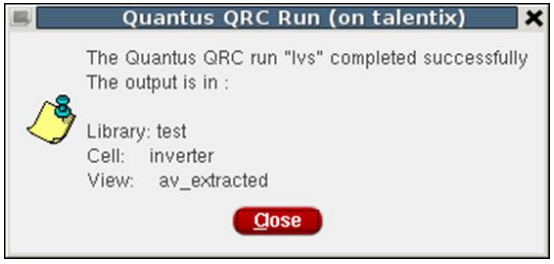




Parasitic Extraction

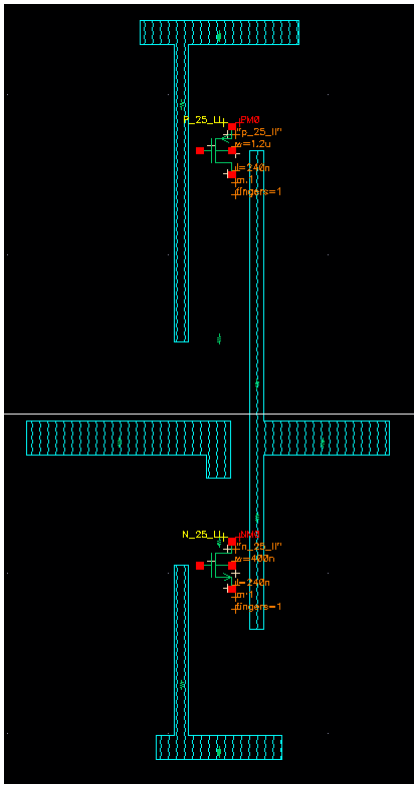
- In the *Extraction* tab, set the properties of different fields as shown in the figure.
- Set *Ref Node* to *vss*. (This must be your circuit ground node. Your opamp design might have another name)
- Click *OK* in the Assura Parasitic Extraction window and watch the progress of the QRC run. It will complete in a few minutes.
- On successful completion, you will get a window as shown below.

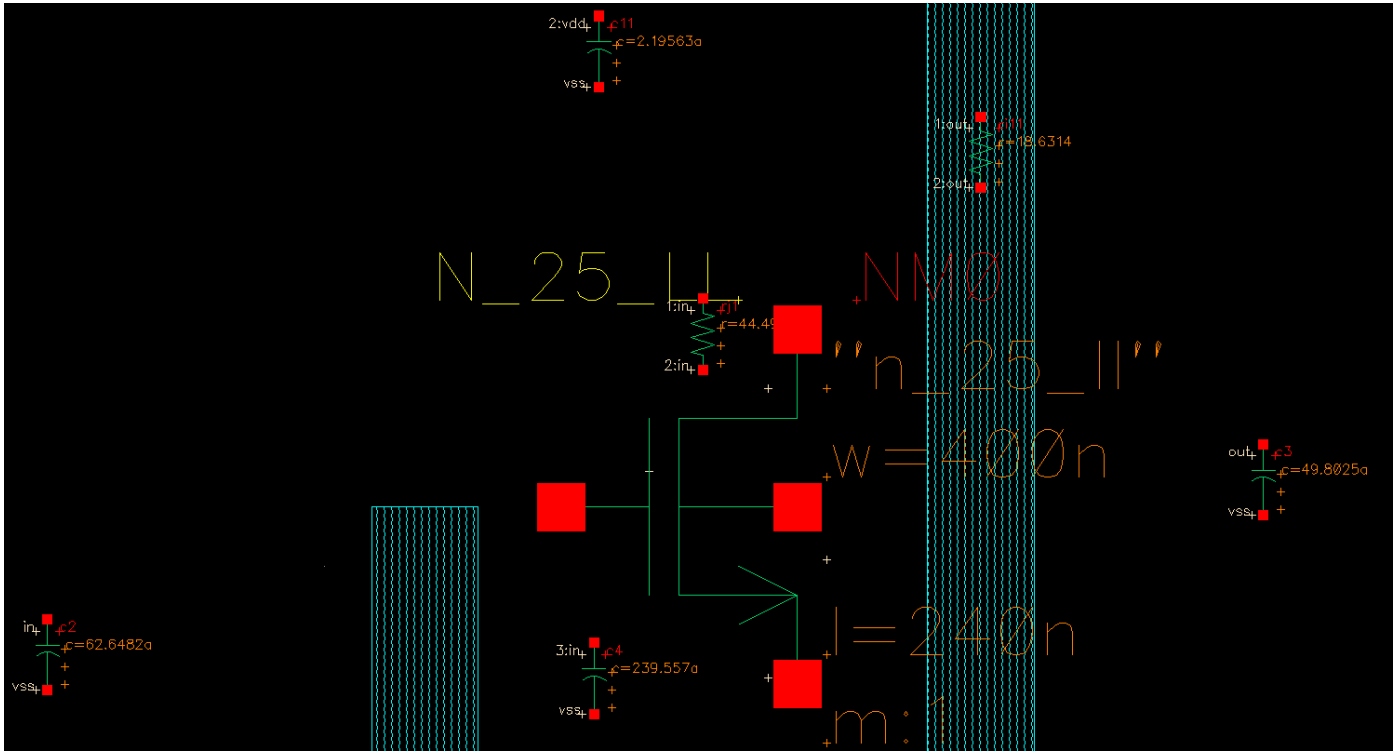




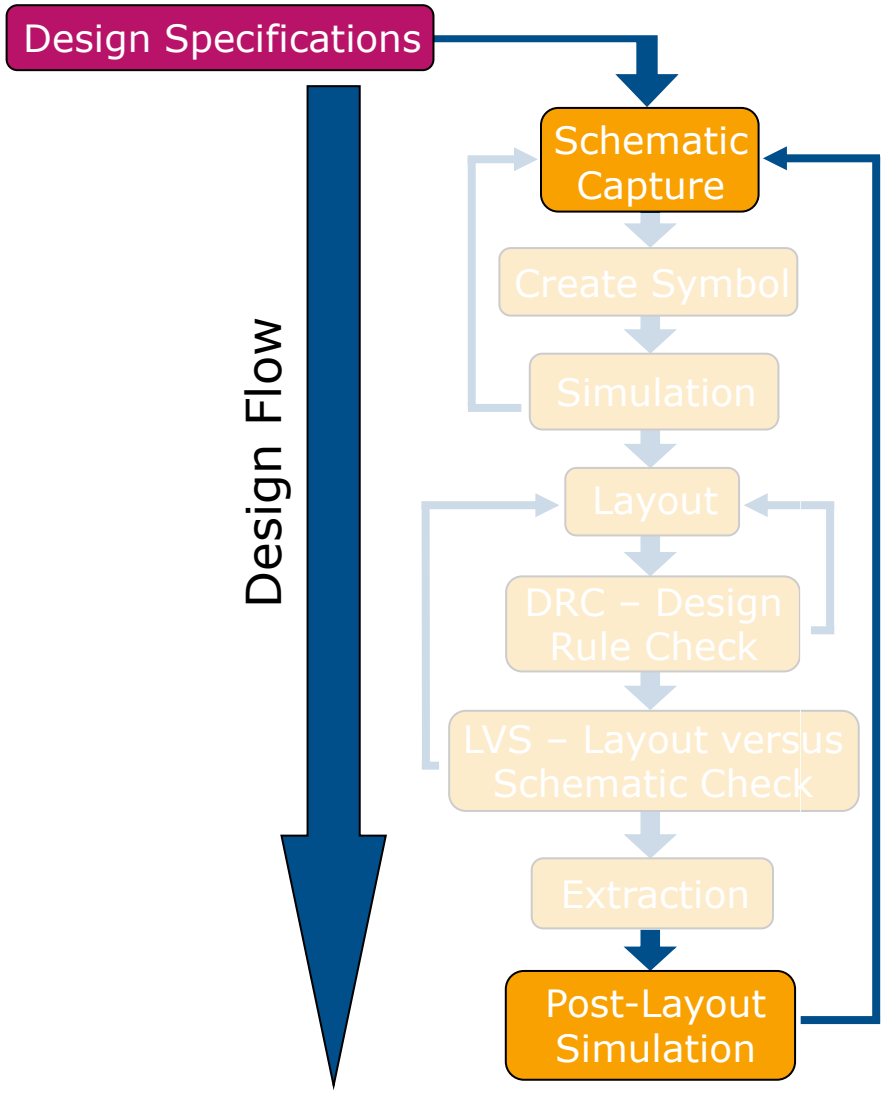
Parasitic Extraction

- An *av_extracted* cellview has been created, which includes parasitic resistances and capacitances of the traces and vias
- An example is shown below





Overview of the Design Flow



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Post-Layout Simulation

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- Refer the file 'Post_Layout_Simulation.pdf' to obtain detailed instructions on how to perform Post Layout Simulation once the parasitic extracted file has been created.
- A brief overview is provided here:
  - For the testbench you have used for schematic level simulation, create a new config cell view.
  - Setup the config file and add av_extracted to the view list in the config file.
  - In the ADE state for the testbench, change the design type to config (instead of schematic which is the default option).
  - Perform the post layout simulations.
  - Depending on the type of simulation desired, switch the view type between av_extracted and schematic for the block under consideration.
  - You could also create multiple instances of the same test block within the test bench and configure one instance as schematic and the other as av_extracted in the config file view type. This way you will be able to compare the results of the schematic level simulations and post layout simulation from the same testbench.

Documentation

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- For further information about Cadence Virtuoso you can access its documentation section by navigating to *Help→ Virtuoso Documentation* in the Virtuoso main window.

Recommended topics/documents:

- Virtuoso ADE Explorer User Guide
- Virtuoso ADE Assembler User Guide
- Overview of Plotting Calculator Expressions
- Virtuoso Schematic Editor L User Guide
- Cadence Library Manager User Guide
- Introducing the Virtuoso Spectre Circuit Simulator
- Virtuoso Layout Suite XL User Guide