Advanced Integrated Circuit Design Lab

Cadence Virtuoso Tutorial– Part 1

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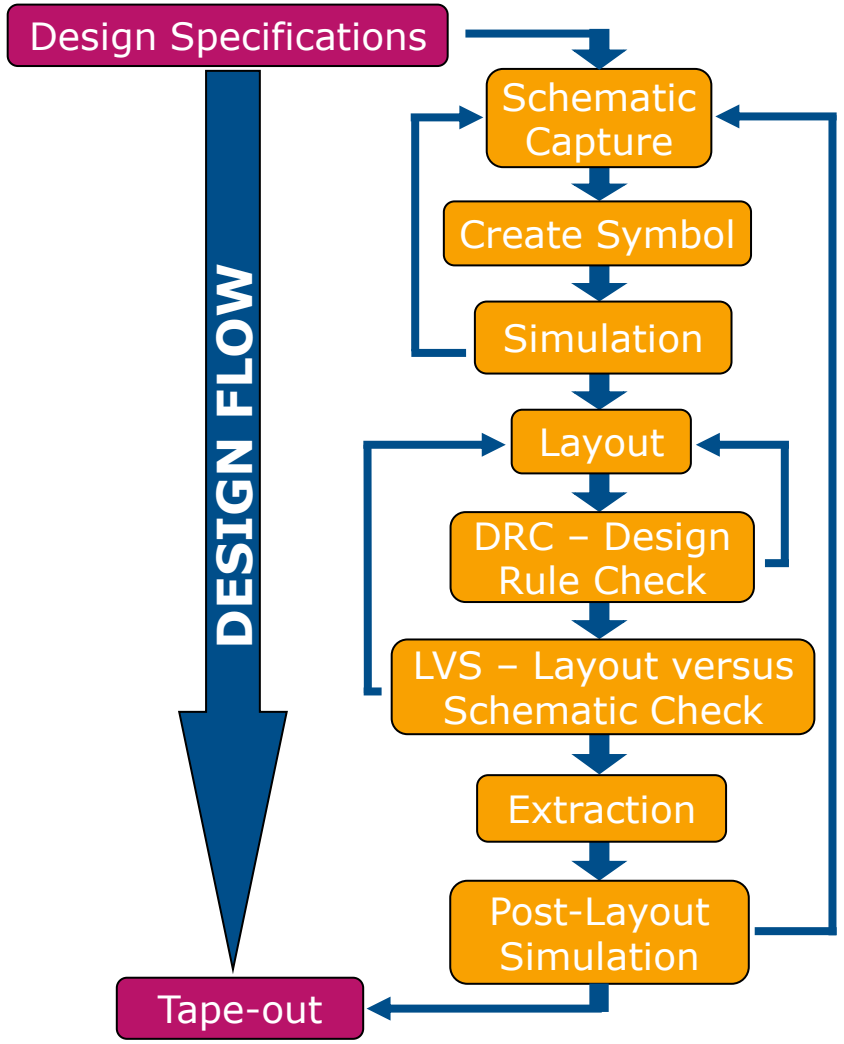
About this tutorial

- In part 1 of this tutorial we create the schamtic of a simple inverter and simulate its output voltage
  - We start by creating the schematic of a simple CMOS inverter
  - We create a symbol to use the inverter in other schematics. So, we just draw a schematic once and use its symbol in other schematics
  - Finally, we create a testbench for the inverter and simulate its output voltage



Quick Start Instructions

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To start working with Cadence Virtuoso, open a terminal and follow these steps:

For first time users:

- *cp –r ~/lehrepub/aic/AICD_lab_project /home/aic##/*
  - *This command copies the master project folder within your home folder.*
  - *Note: replace ## with your group number. Ex: cd /home/aic07 for group 07.*
- *cd /home/aic##/AICD_lab_project/*
  - *This command sets your home folder '/home/aic##/' as the working directory in the terminal.*
- *./vir/create_initfiles.sh*
  - *Creates initial setup files necessary for UMC65 nm technology.*
- *./start_virtuoso.sh*
  - *Starts Cadence Virtuoso*

The command flow looks a bit different for users who have already created Cadence Workspace and started virtuoso before:

- *cd /home/aic##/AICD_lab_project*
- *./start_virtuoso.sh*

Quick Start Instructions

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If you are asked by the supervisor/tutor to start Virtuoso from a server instead of the local machine, please follow the following command flow:

- *ssh -X amnesix*
  - *Switch to the server named "amnesix". The server "informatix" and "popeline" are available as well. When the command is executed, it will ask you for a password. Enter the password for your aic## account.* ***This command should be used when specifically instructed or when running extensive simulations.*** *By default local machines should be used for your work.*
- *cd /home/aic##/AICD_lab_project*
- *./start_virtuoso.sh*

UMC 65 nm Technology Node

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During this tutorial and during the lab, you will use a 65 nm process of the UMC semiconductor foundry (United Microelectronics Corporation, http://www.umc.com/). Here are the important devices and parameter for this lab:

- Technology library name — *umc65ll*
- NMOS (4-terminal) — *N_25_LL*
- PMOS (4-terminal) — *P_25_LL*
- Supply voltage — *1.8 V*
- Capacitor (MIMCAP) — *MIMCAPS_20F_MM*
- Capacitor (MOMCAP) — *MOMCAPS_AS_MMKF*
- Resistor (3-terminal) — *RNHR_LL*
- Bulk contacts (in layout)
  - NMOS — *M1_PSUB via*
  - PMOS — *M1_NWEL via*
  - RESISTOR — *M1_NWEL via*

UMC 65 nm Technology Node

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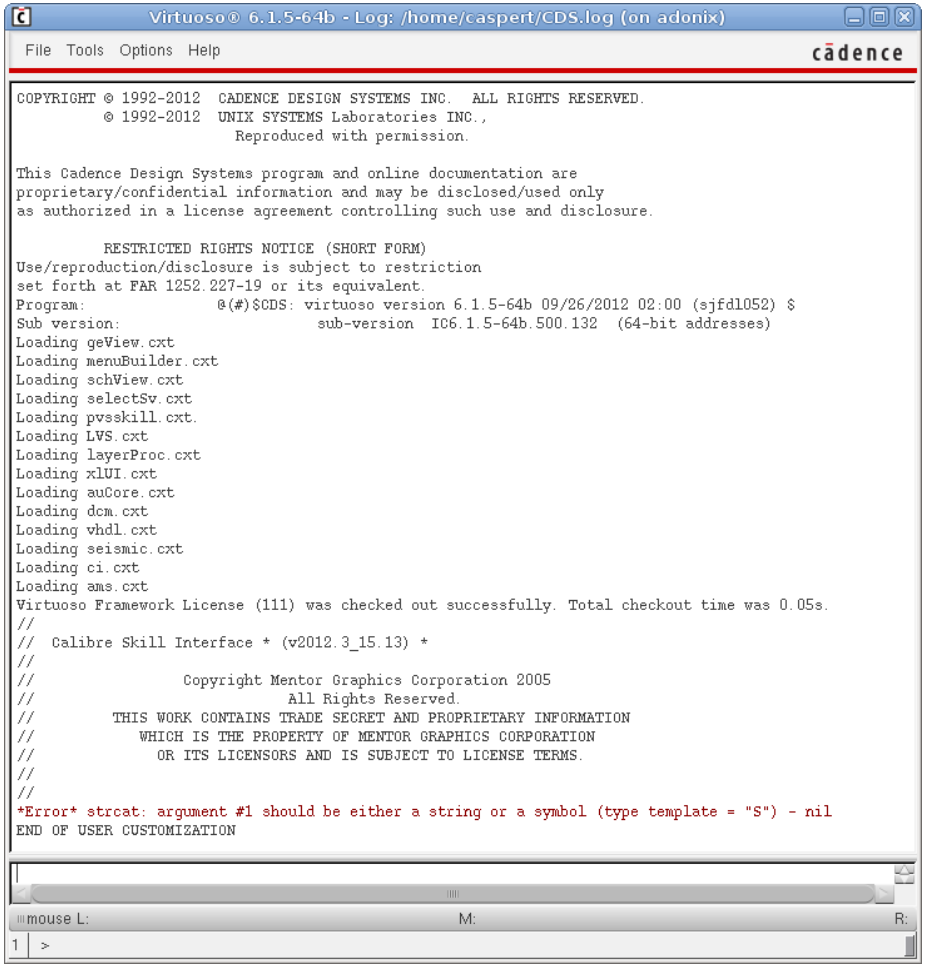
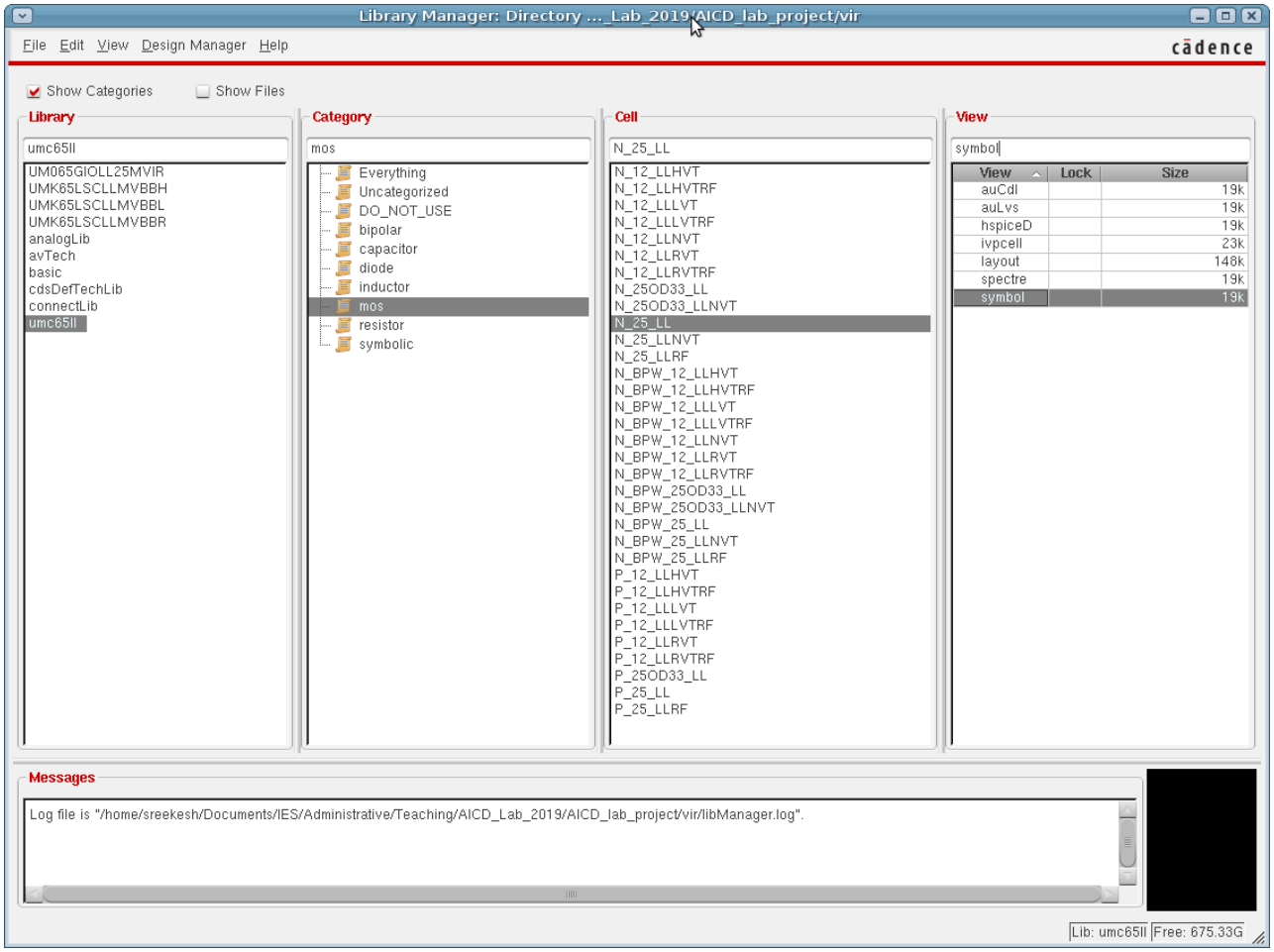
- You will see a main window, as shown below.



- In this window, click *Tools → Library Manager* to open the Library Manager (see next slide). This is where you can see all the installed cell libraries and create your own libraries.
- From the libraries that you can see, you have to take all the elements from the technology that you are using (here *umc65ll*).
- Also check *Show Categories* to see the different devices in each library.

UMC 65 nm Technology Node

- If you click on *umc65ll*, you can see the different devices available and specifically the two core MOS transistors, *N_25_LL* and *P_25_LL*, as shown in the figure below.



UMC 65 nm – Bulk Contacts

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- **Bulk connections in NMOS and PMOS transistors**
  - In order to eliminate bulk effects, the bulk terminals of the NMOS (PMOS) transistors are often connected to their source terminals. Although the *umc65ll* technology supports twin wells in the substrate, which means NMOS transistors can have their own separate wells, it is not a standard process. Therefore, **always(!)** connect the NMOS transistor's bulk terminal to the lowest potential, i.e., *gnd*. Generally, the PMOS bulk terminal can be connected to any voltage, since it is in a separate well. However, for this lab it is recommended to connect it to the highest voltage, i.e., *vdd*.
  - In the layout the NMOS (PMOS) components do not have a bulk terminal. You have to provide the bulk contact by an *M1_PSUB* (*M1_NWEL*) via cell from the *umc65ll* library.
- **Bulk connections in Resistors**
  - The *RNHR_LL* resistors also have a bulk terminal, which should be connected to the supply voltage *vdd*.
  - In the layout the *RNHR_LL* components do not have this bulk terminal. You have to provide the bulk contact by an *M1_NWEL* via, as it done for contacting the n-well of the PMOS transistors.

AnalogLib Library

AnalogLib library is a generic library available in Cadence. You can use the elements from this library for components (e.g. voltages sources, ground etc.) required in your design or testbench which are not available in *umc65ll* technology library.

- Library name *analogLib*
- DC voltage source *vdc*
- AC voltage source *vsin*
- Global ground *gnd*
- Ideal Capacitor *cap*
- Ideal Resistor *res*

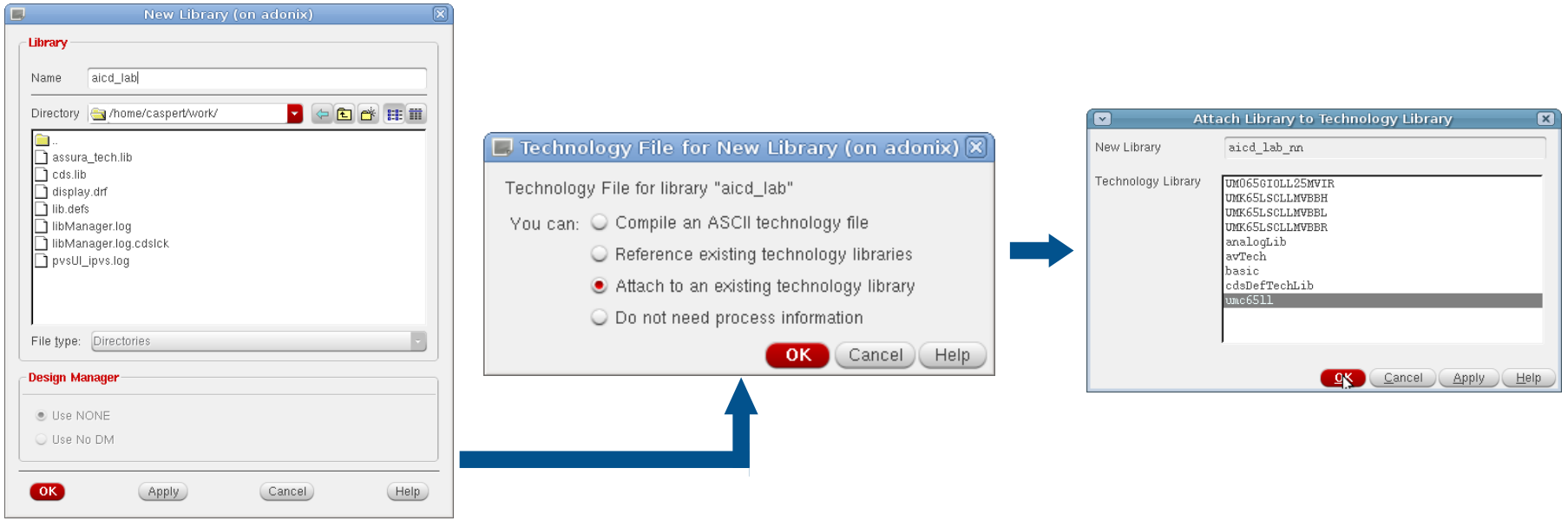
Passive circuit components

For the initial schematic simulations you can use the ideal capacitor and resistor components *cap* and *res* from the *analogLib* library. However, before you finalize your design you have to change the capacitors and the resistors in your design to the ones from the *umc65ll* library (*MIMCAPS_20F_MM / MOMCAPS_AS_MMKF* and *RNHR_LL*).

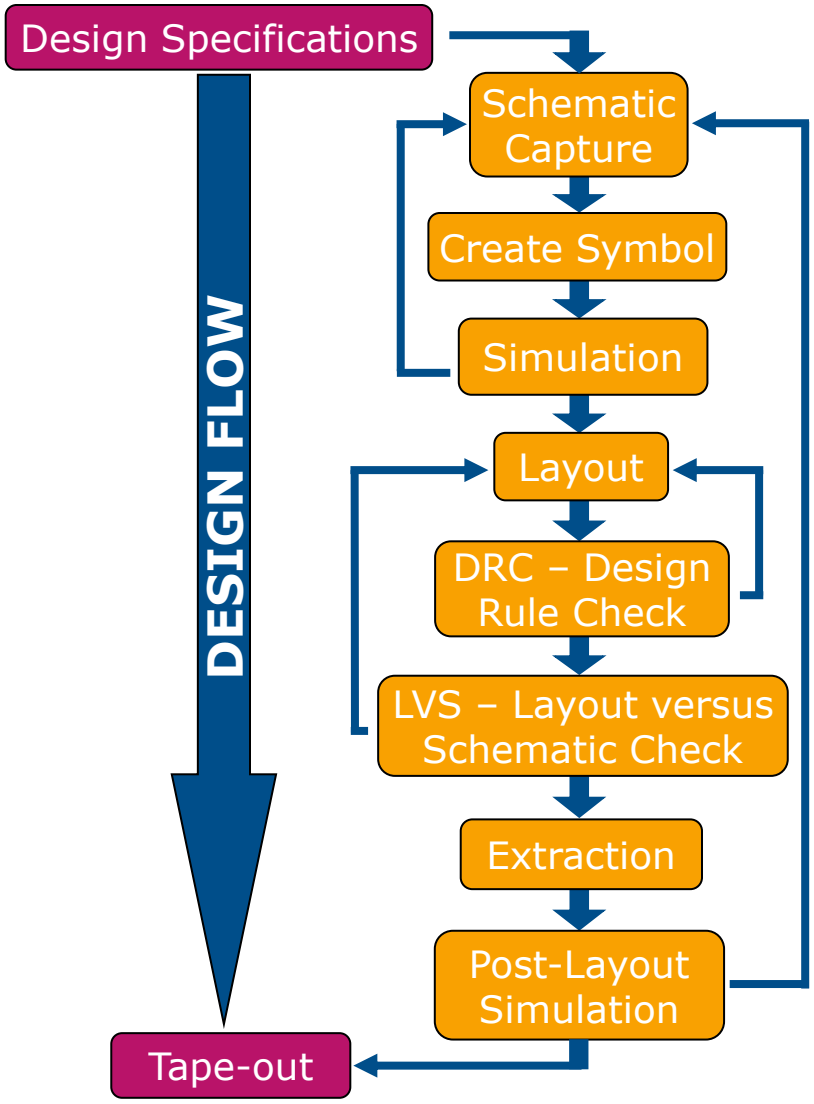
Creating Your Design Library

- Create a library for your design by clicking *File → New → Library* in the Library Manager.
- Name your library *aicd_lab_##*, where *##* should be replaced by your group number!
  Ex: For group 01, the library name would be aicd_lab_01. For group 12 it would be aicd_lab_12.

  Attention: All your designs for the lab have to be created exclusively in this library!
- Attach the library to an existing technology file, here *umc65ll*, provided by UMC. To perform this step, first check *Attach to an existing technology library* and click *OK*. Then choose *umc65ll* from the drop-down menu and click *OK* (see right figure below).
- In the library manager you can see that the new library *aicd_lab_##* has been created. In this library we will now do the circuit design, layout and verification of a simple CMOS inverter.

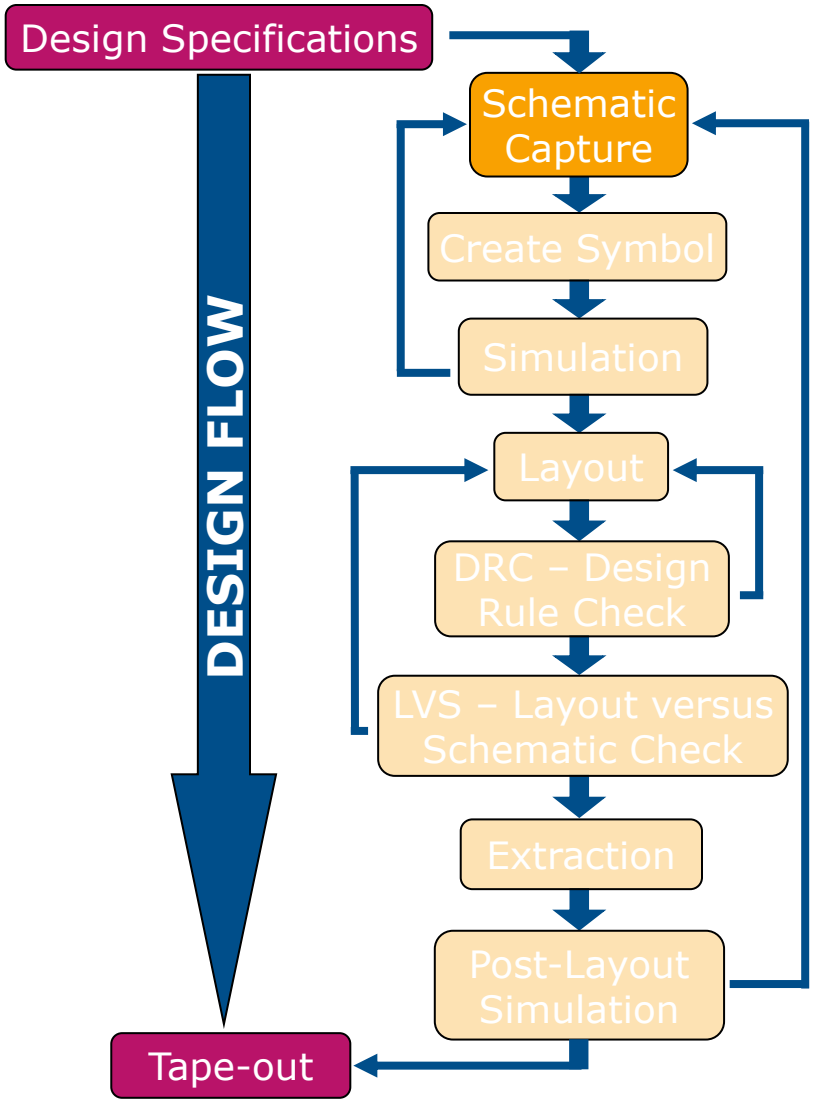


Overview of the Design Flow



- Virtuoso Schematic Editor
- Virtuoso Symbol Editor
- Virtuoso Analog Design Environment
- Virtuoso Layout Editor
- Assura DRC
- Assura LVS
- Assura QRC
- Virtuoso Analog Design Environment

Overview of the Design Flow



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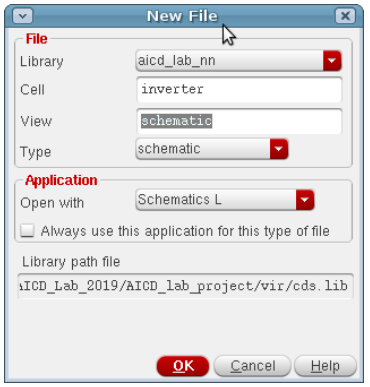
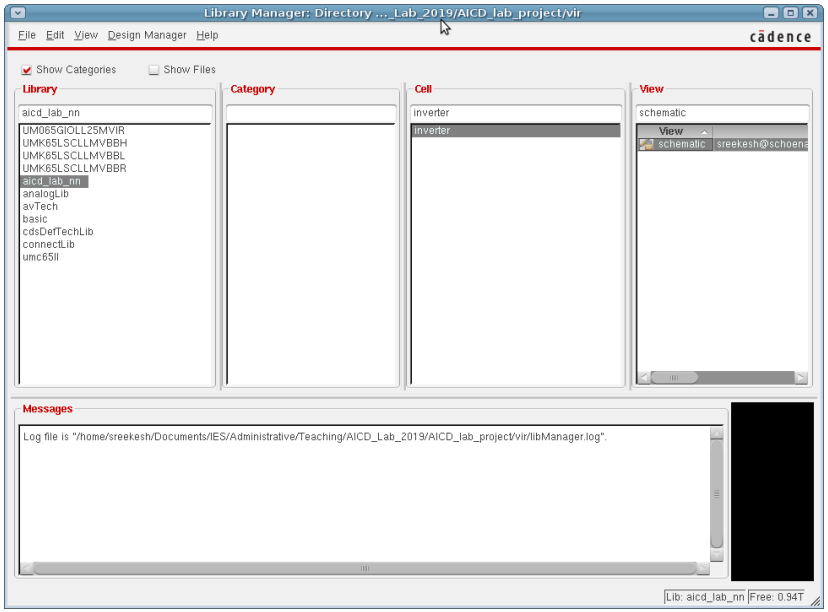
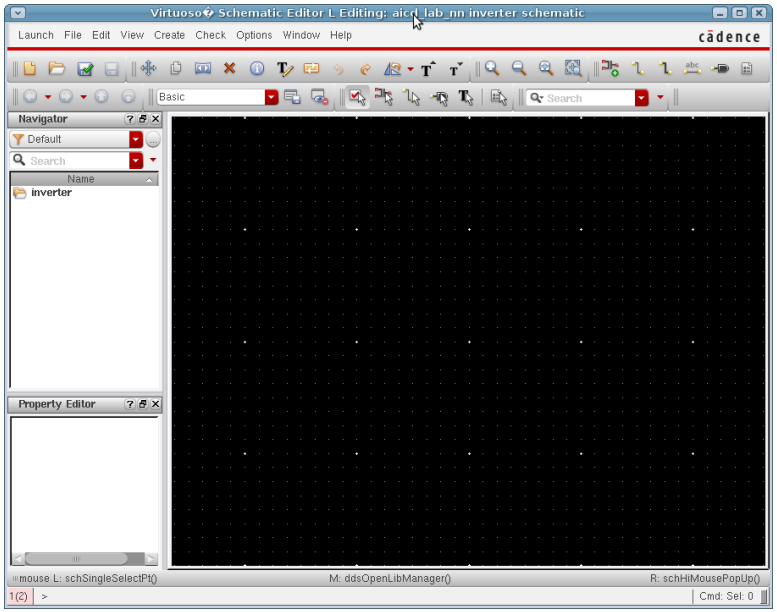
Schematic Capture

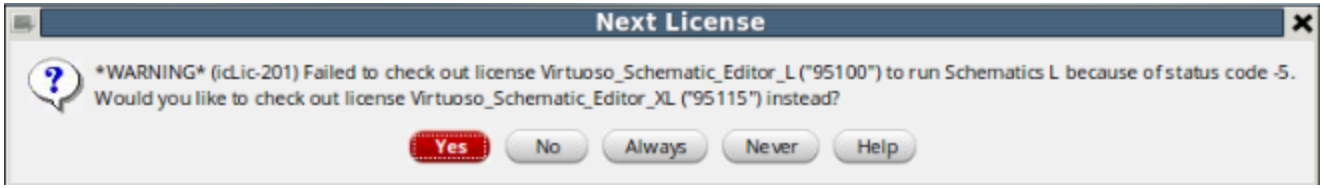
- Create a new cell in the library *aicd_lab_##* by clicking *File→ New→ Cell View* in the Library Manager.
- Make sure that *aicd_lab_##* is shown in the *Library* field, type *inverter* in the *Cell* field and make sure that *schematic* is shown in the *View* field. Finally, in the *Open with* drop-down menu, choose *Schematics L* and click *OK* (see figure on the right).
- The last step will open the Virtuoso Schematic Editor window (see bottom right) which will be used for schematic editing. If the editor is not automatically opened, you can browse to the newly-created cell in the Library Manager and double-click on the *schematic* cell view (see bottom left).





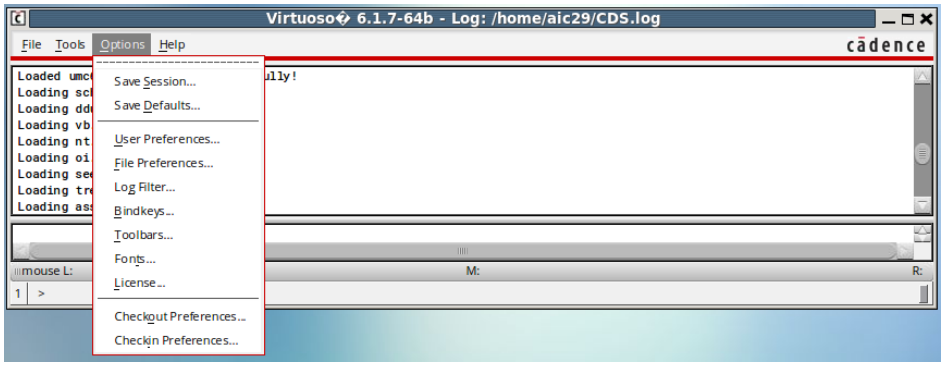


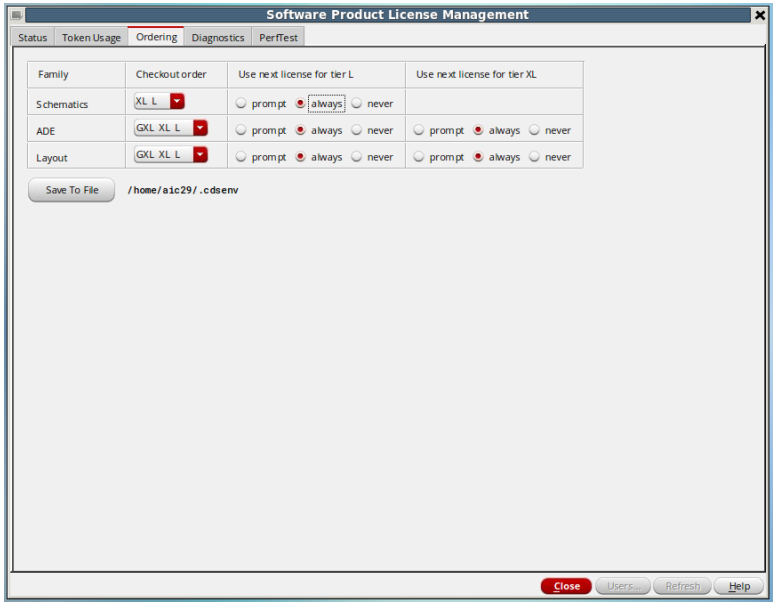
Licensing



First time users might encounter a “Next License” warning like above. You can simply click always to avoid further messages in the future.

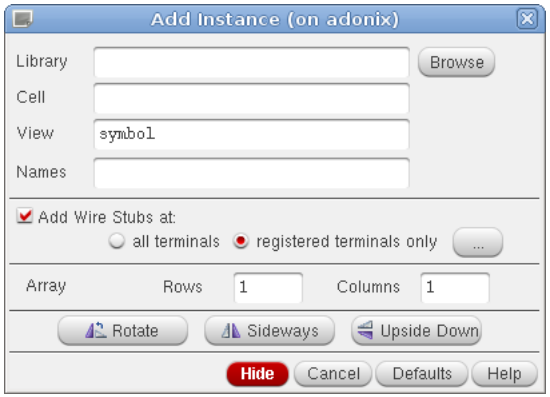
License ordering can be changed to provide a faster checkout. Usually, the benefit is small and this step is optional. Go to *Options → License* in the virtuoso window (see below) and go to the *Ordering* tab. Apply the license settings as shown on the right.

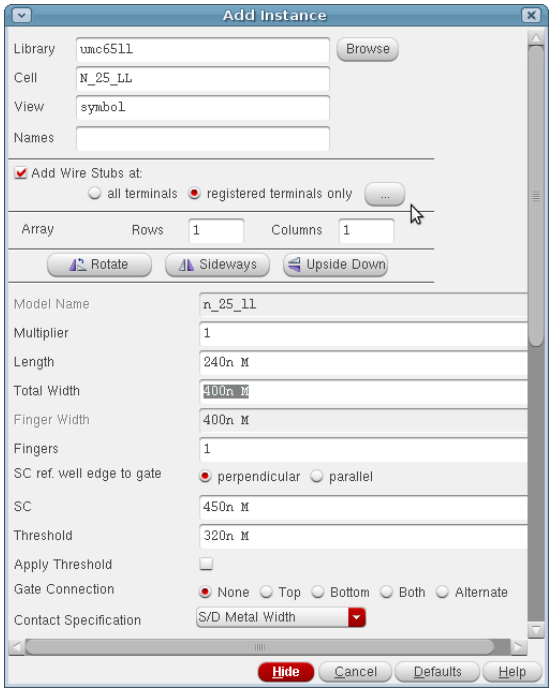




Schematic Capture

- To place a device, go to *Create→ Instance* in the schematic editor or simply use the keyboard shortcut *i*.
- Try to remember the important keyboard shortcuts such as those for *move (m), delete (del), wire (w), object property (q), check and save (shift+x)* and *add instance (i).*
- Click on *Browse* to open the Library Manager and select the required NMOS transistor for the inverter: *umc65ll→ mos→ N_25_LL→ symbol*. Click *Close*.
- In this example, we will design an inverter with W/L = 400 nm/ 240 nm for the NMOS and W/L = 1.2 um/240 nm for the PMOS.
- Enter *Length=240n* and *Total Width=400n* in the *Add Instance* window (see figure on the bottom right). '*n*' means nanometer and '*u*' means micrometer. Leave the rest at default. Click *Hide* and place the NMOS by left-clicking in the schematic editor.
- Repeat these steps to place a PMOS *P_25_LL*.
- To connect the devices, go to *Create→ Wire (narrow)* in the schematic editor or simply use the keyboard shortcut *w*. When all connections are done, the inverter will look as shown on the bottom left.



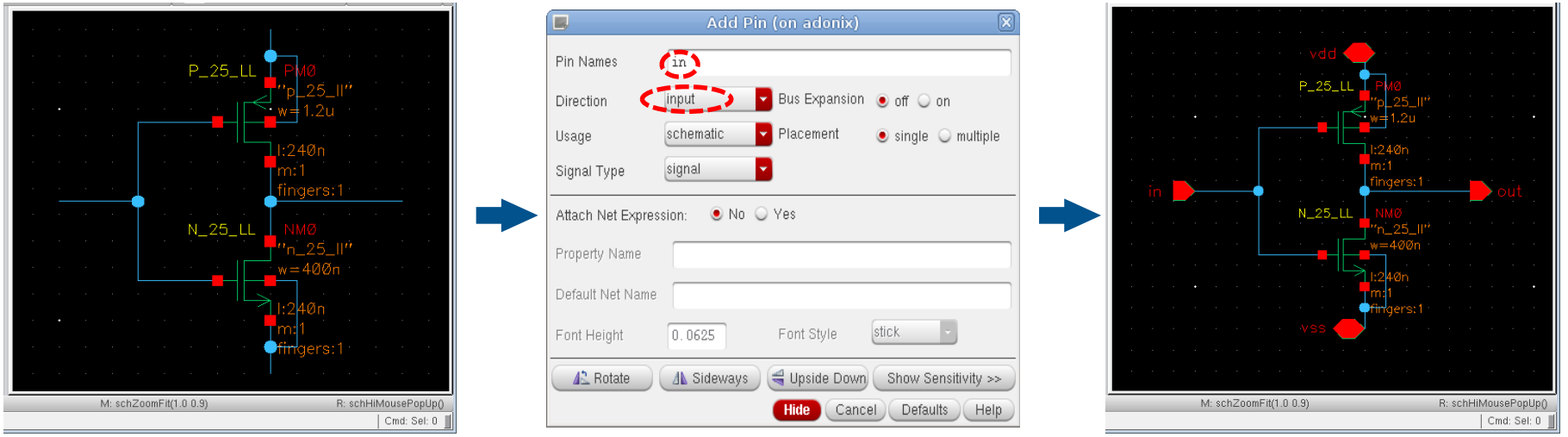


Schematic Capture

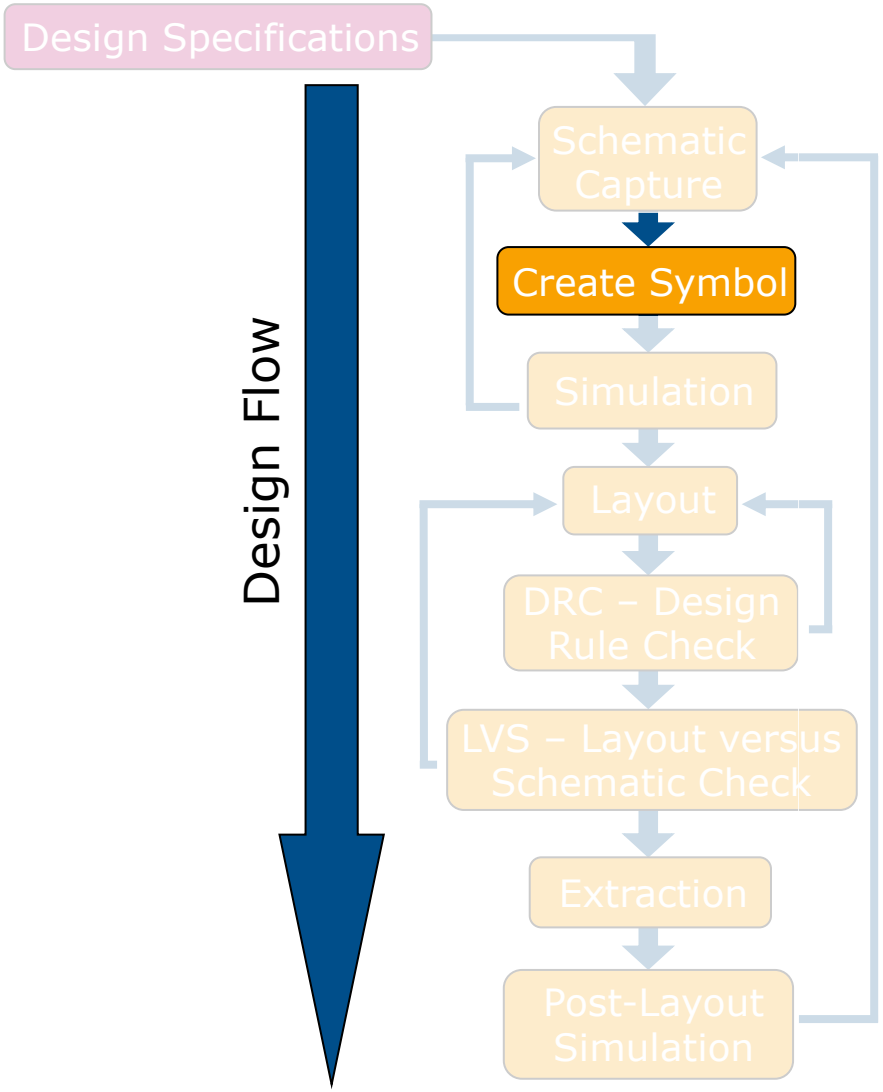
- Now, add pins to the design. Pins connect the cellview to other cellviews in your design hierarchy.
- To create a pin, go to *Create→ Pin* in the schematic editor or use the *keyboard shortcut p*.
- Now, create the following pins and complete the schematic as shown below:

Pin Name	Direction	Pin Name	Direction
in	*input*	*vdd*	*inputoutput*
out	*output*	*vss*	*inputoutput*

- Go to *File→ Check and Save* or use the keyboard shortcut *shift+x* in the schematic editor to check and save the design. Perform this step every time you make changes to the design and if you get information about any mistakes or warnings in the schematic.



Overview of the Design Flow



- Virtuoso Schematic Editor
- **Virtuoso Symbol Editor**
- Virtuoso Analog Design Environment
- Virtuoso Layout Editor
- Assura DRC
- Assura LVS
- Assura QRC
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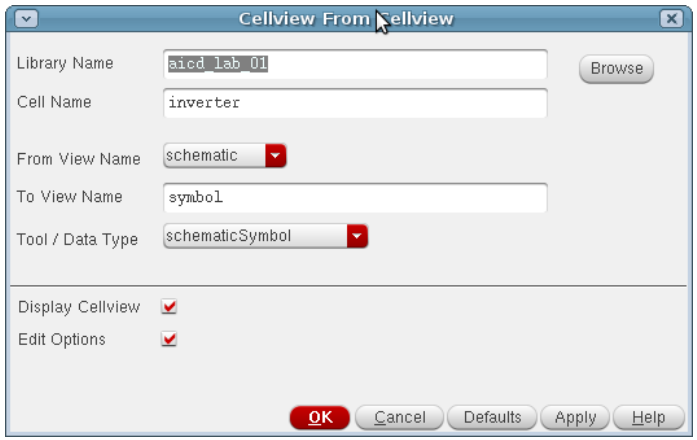
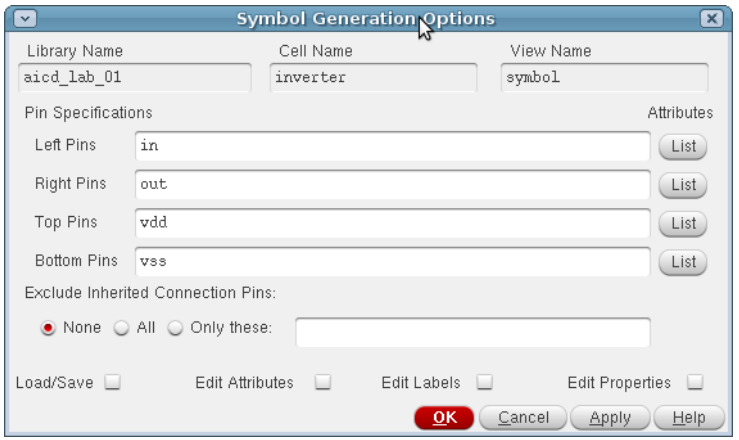
Symbol Editing

- In the next step go to *Create→ Cellview→ From Cellview* in the schematic editor to create a new cell view of the schematic. You will see the window as shown in the figure on the bottom left.
- Make sure the entries are as shown in this figure and click *OK*.
- The next window should look like the one on the bottom right. If it does not, type *in* in the *Left Pins* field, *out* in the *Right Pins* field, *vdd* in the *Top Pins* field and *vss* in *Bottom Pins* and click *OK*.

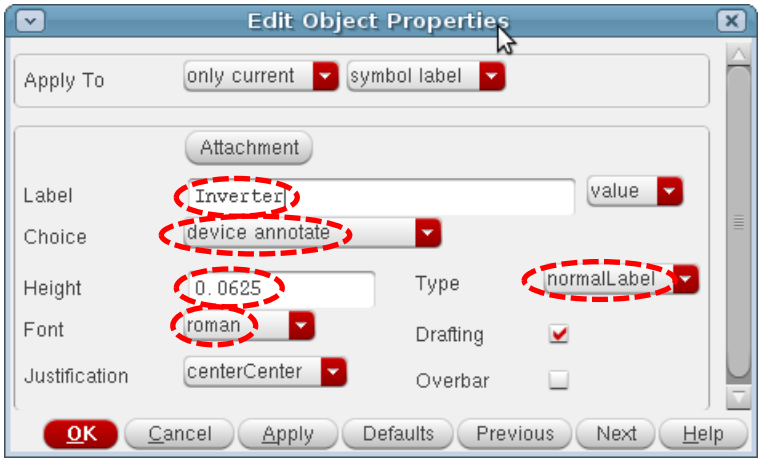


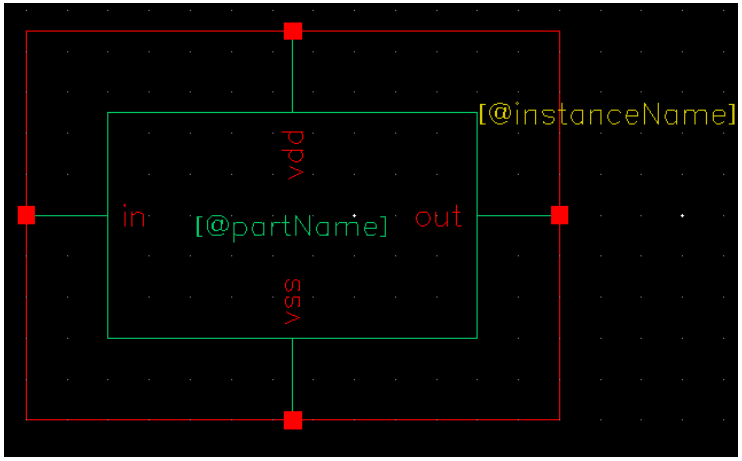


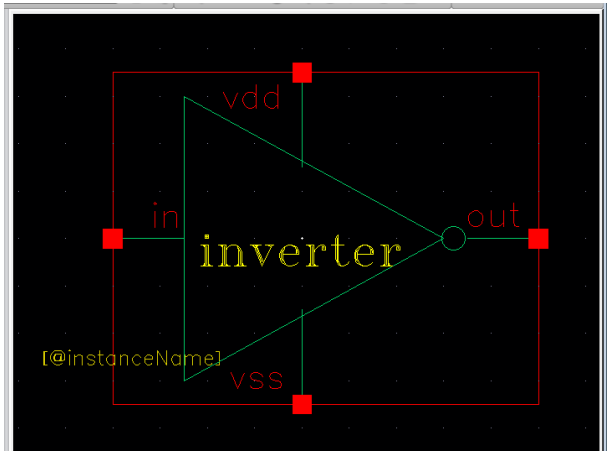
- A symbol editor window will appear (see next page) and a default symbol will appear. You can re-draw the symbol in such a way that the cell view is easily recognizable as an inverter (or transmission gate, OPAMP and so on) when instantiated on a higher level cellview.
- To modify the default symbol, use the tools *Line*, *Delete*, *Move*, *Undo* and others from the symbol editor window.
- Try editing the symbol to make it appear as shown in the next page

Symbol Editing

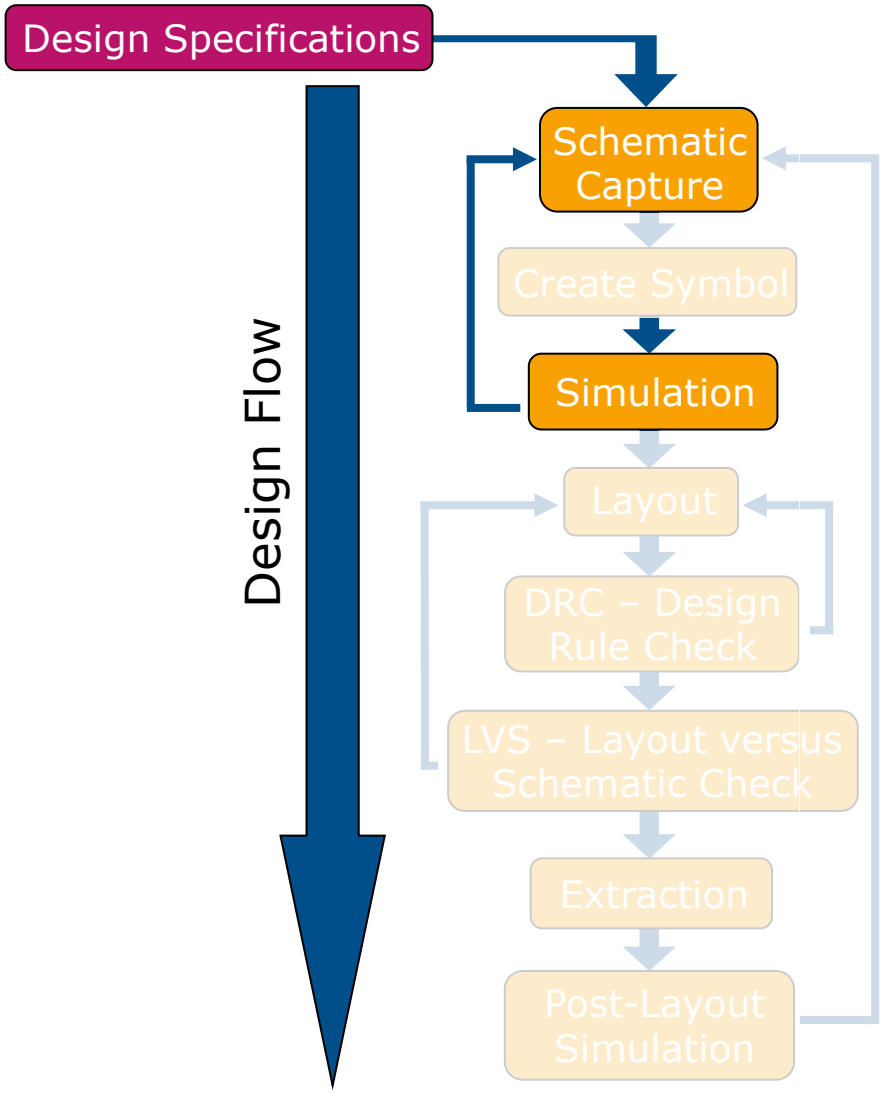
- Notice that the *[@partName]* has been renamed as *Inverter* and its font style has been changed. This is done by selecting the label *[@partName]* and pressing *q* to open its properties for editing.
- If you made a mistake, use *Edit → Undo* or the shortcut *u* to go back.
- *Save* the Symbol once you have finished editing it. *Check and save* the schematic as well.
- You may now close both the schematic and symbol editor. In the Library Manager you can now see a *schematic* and a *symbol* cell view for the *inverter* cell of the *aicd_lab_##* library.







Overview of the Design Flow



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Simulation – Create Testbench

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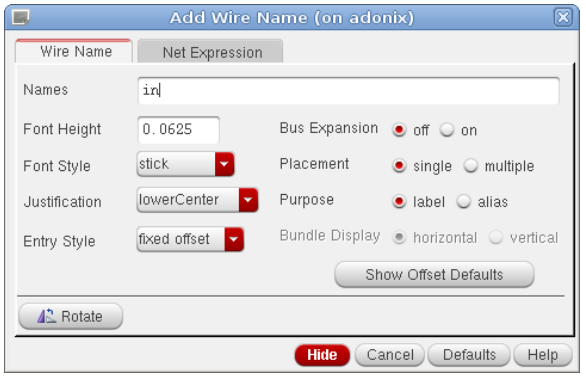
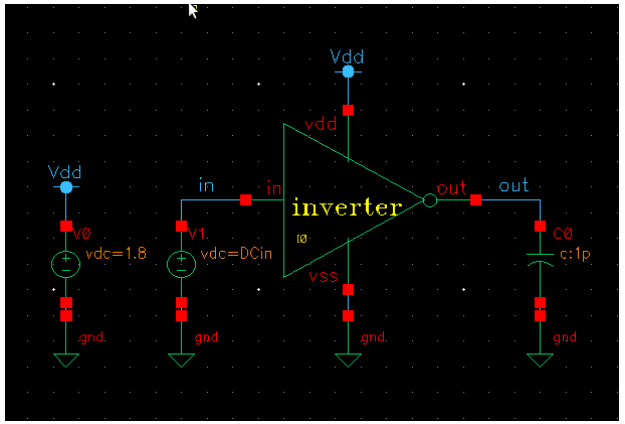
- Create a new schematic cell view and call it *inverter_test*. Add the symbol cell view of the inverter (see figure below) that you created in the previous slide as an instance.
- Add the following instances from *analogLib* as well (see figure at the bottom right):
  - A DC input voltage source *vdc*. Enter *DC Voltage = DCin*. You can click on any object in the schematic editor window and open its properties by using keyboard shortcut *q*.
  - A DC voltage source *vdc* to specify the supply voltage *vdd = 1.8 V*.
  - A ground node *gnd*.
  - A load capacitor *cap* of *1 pF*.
- Finally use *Wire* to connect the different cell views together.
- Add labels to the nets (i.e. wires) by going to *Create→ Wire Name* or press the keyboard shortcut *l (small L)* to specify labels (see figure). Type *in*(*out*) in the *Names* field and click on the net that you want to label. Once you are finished click *Cancel* or escape keyboard shortcut.
- Labels could also be used to connect nodes (without having a wire connection between them) and make the schematic appear more compact. Use label *Vdd* to connect 1.8 supply to the *vdd pin* of Inverter cellview.
- The schematic is ready for simulation (see figure). Check and save the schematic.





Simulation– ADE Explorer Setup

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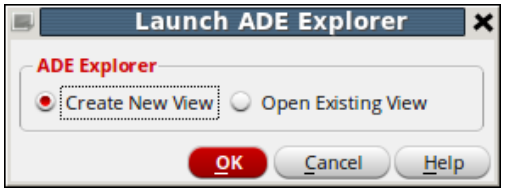
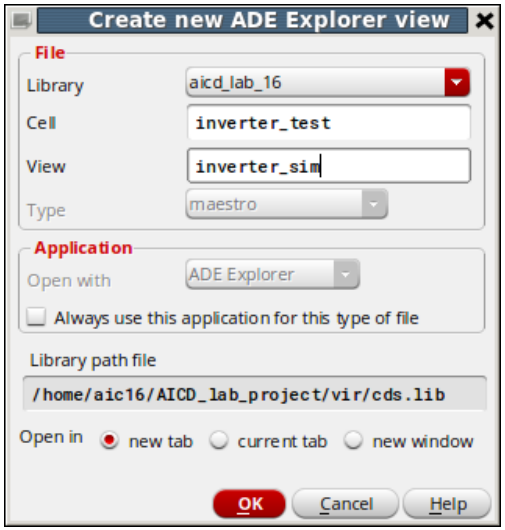
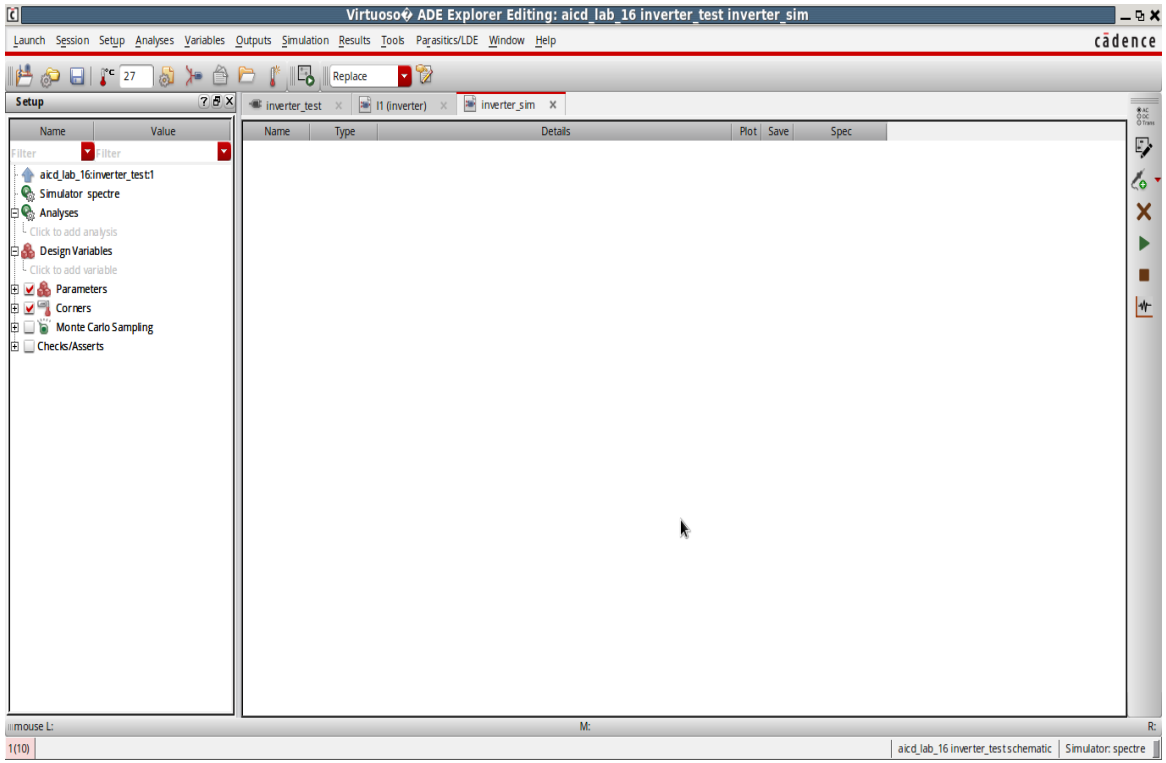
- Go to *Launch→ ADE Explorer* in the schematic editor to start simulating the circuit in Virtuoso Analog Design Environment (see on the bottom left). Here, we perform simulations by specifying the type of analysis, global sources, parameter sweeps, Corner, Monte Carlo simulations and so on.
- By selecting *Create New View*, a new ADE Explorer view like the figures below will open. The new window will be like the figure on the right below.

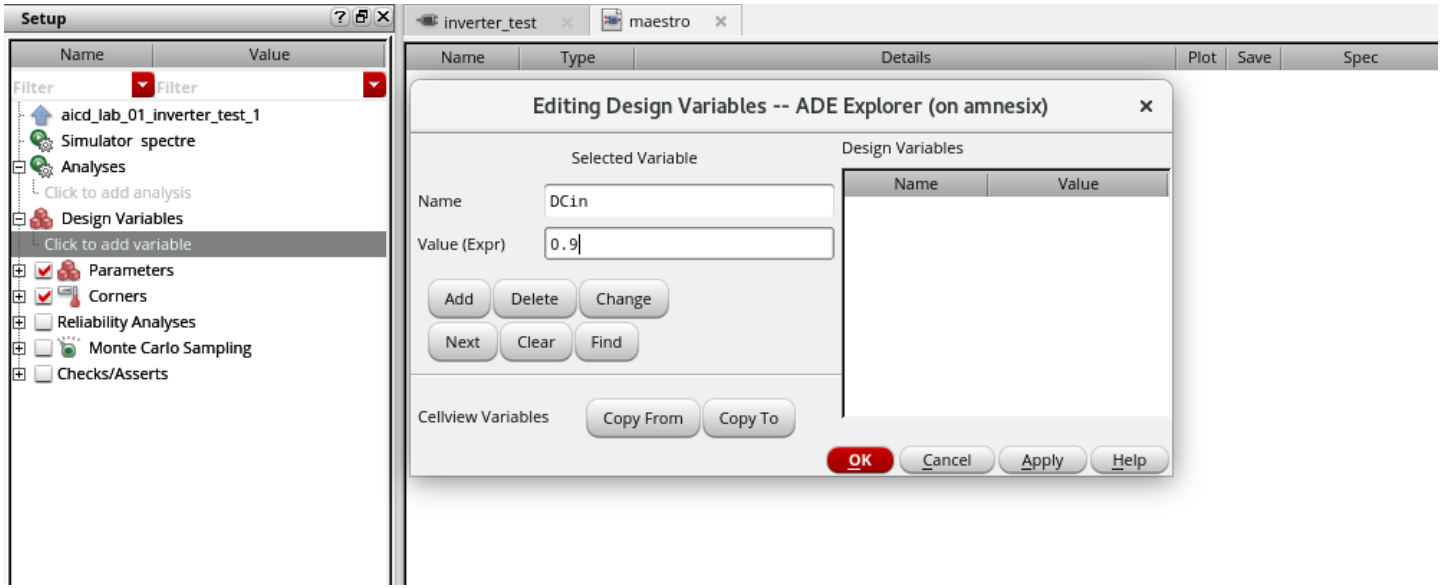






Simulation– ADE Explorer Setup

- From the menu bar, go to *Variables→ Edit* in ADE to add the variable *DCin* that we defined on the previous slide. Type *DCin* in the *Name* field and enter a value of say *0.9* in the *Value (Expr)* field. Click *Add* and then *OK* (Alternatively, you can select *Copy From* button to import variables from the design directly; see on the figure below). The variable will then appear in the ADE window in the *Design Variables* section.



Simulation– ADE Explorer Setup

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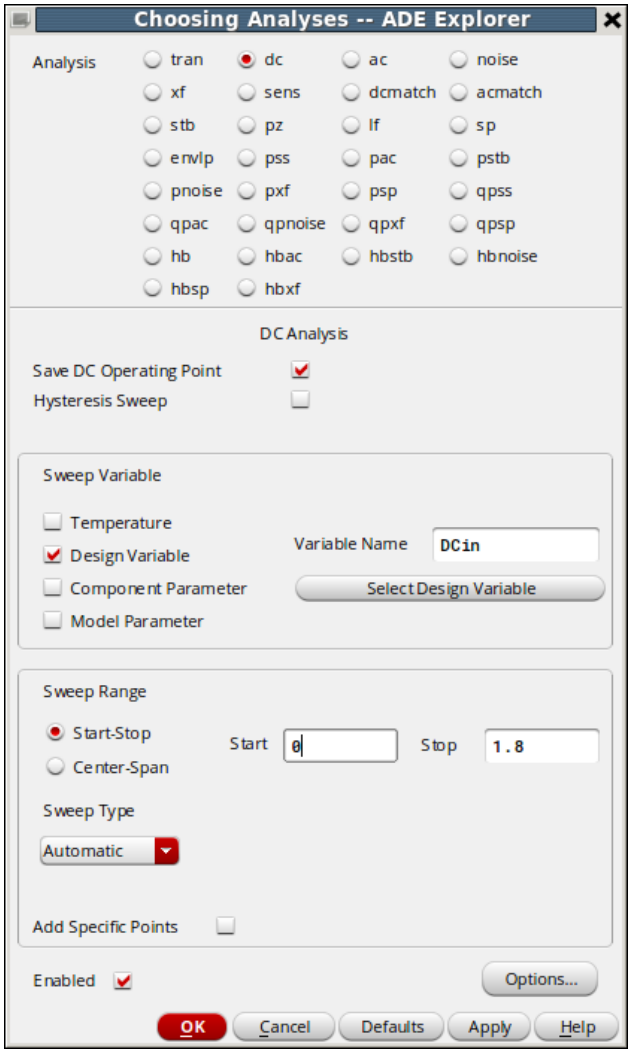
- To specify the type of simulation go to *Analyses→ Choose* or use the uppermost shortcut on the right hand side in ADE.
- Check *Analysis=dc* and *Save DC Operating Point*. Checking Saving the DC Operating Point gives us access to the DC operating points and thereby, the DC biasing conditions of the device under test, *dut* (in this case the *inverter*).
- In this tutorial, we will sweep the input voltage and see the corresponding outputs. So, in the section of *Sweep variable*, we set *Variable Name* to DCin as *Design Variable*.
- We sweep the input voltage from 0V to 1.8V. Therefore, on *Sweep Range*, we set the DCin sweep from *start* 0 to *end* 1.8



Simulation– ADE Explorer Setup

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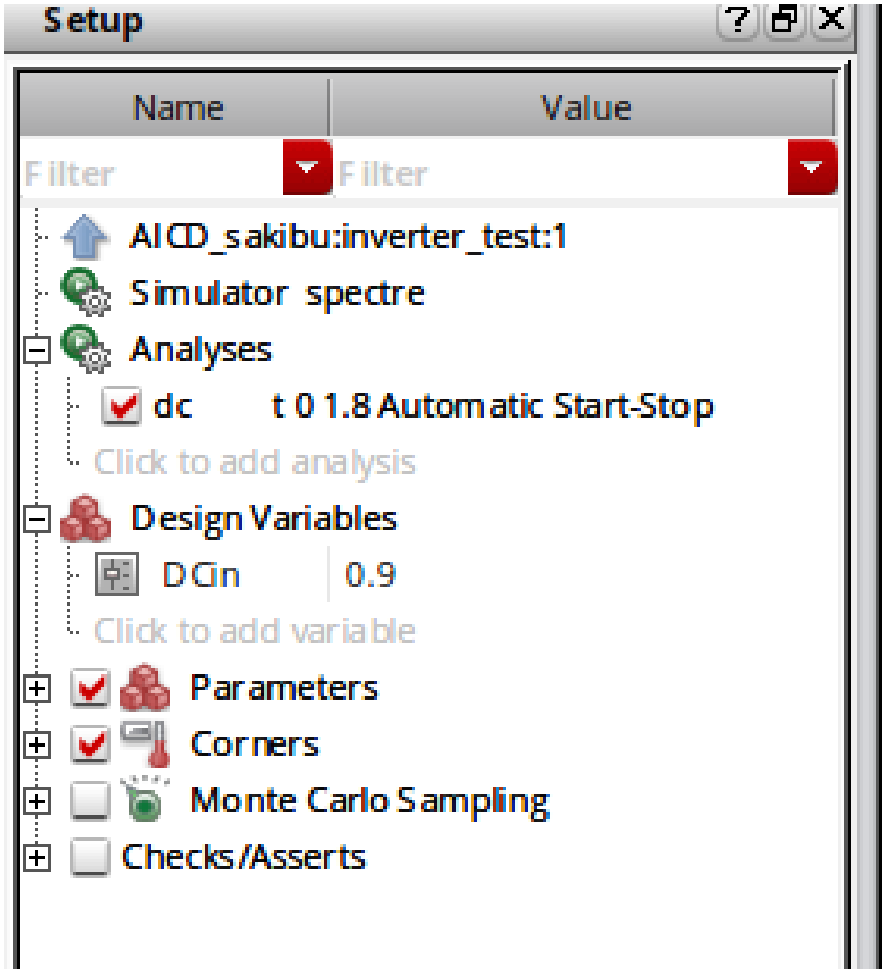
- After adding design variables and analyses, the setup will look like the following picture:



Simulation– ADE Explorer Setup

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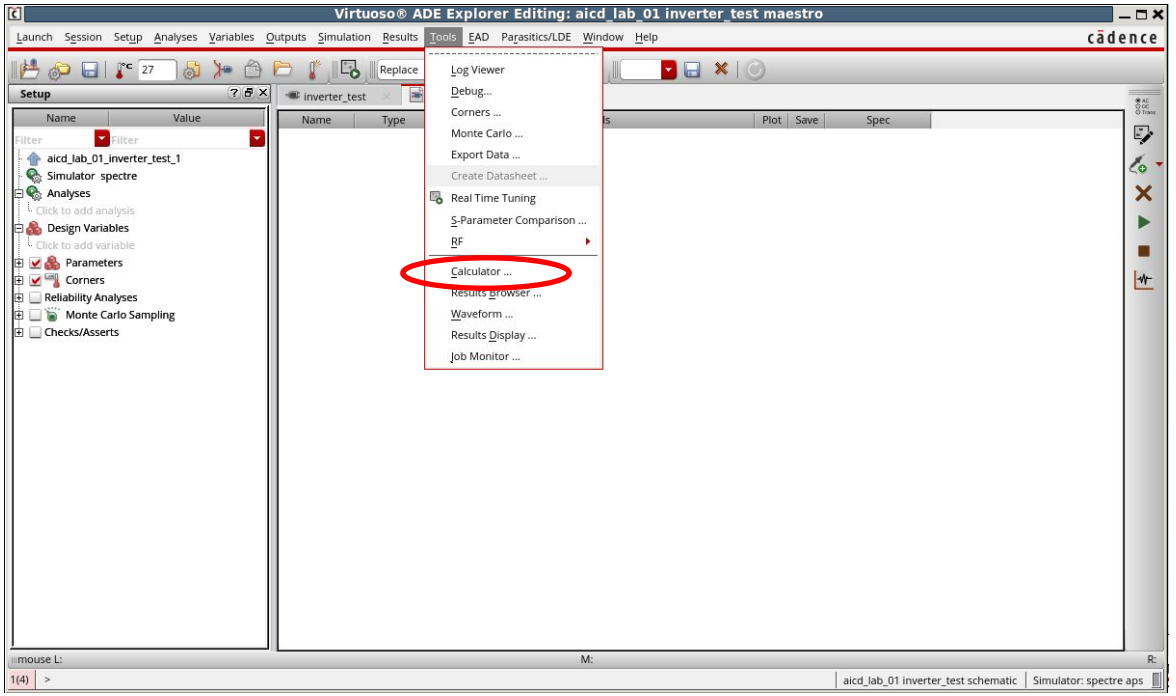
For the inverter testbench, only the dc response is required. We will now try to add the DC response of the input and output nets (*in* and *out*) to the ADE simulation setup. To set it, from ADE window, go to *Tools→ Calculator.*

A calculator window will open.



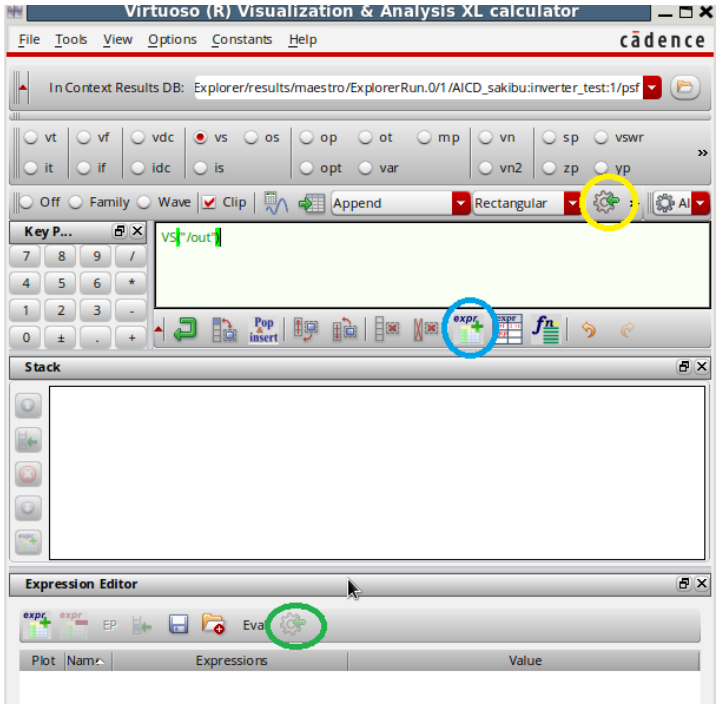
- Calculator toolbox of the ADE Explorer lets us setup expressions to be saved/plotted during the simulation.
  - *vdc* and *idc* options in Calculator toolbox could be used for setting DC voltage and current outputs, respectively.
  - *vs* and *is* options could be used for the expressions of DC sweep voltage and current, respectively.
  - *vf* and *if* options could be used for setting AC outputs.
  - *vt* and *it* for setting up transient outputs.

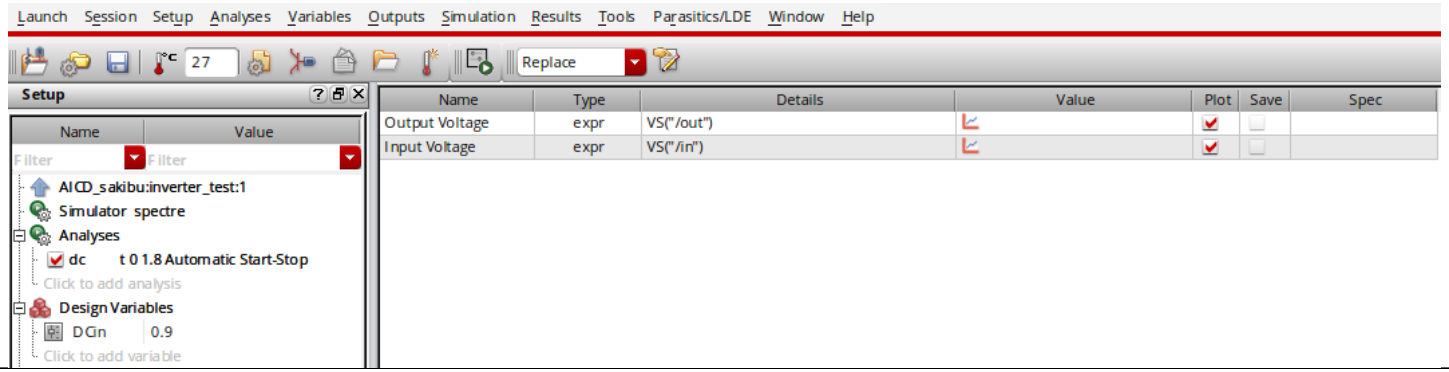
Simulation – ADE Calculator

- Click on *vs* and select the net *out* from the schematic. Once you have selected the net, the expression *VS("/out")* appears in the calculator.
- To send the expression to ADE window, click *send buffer expression* to ADE outputs (marked yellow).

[Tips: Sometimes you may need to add multiple expressions. On those cases, you may send the expressions to the expression editor (marked blue) and editing it there and finally when done, send all of the expressions together to the ADE window (marked green)]

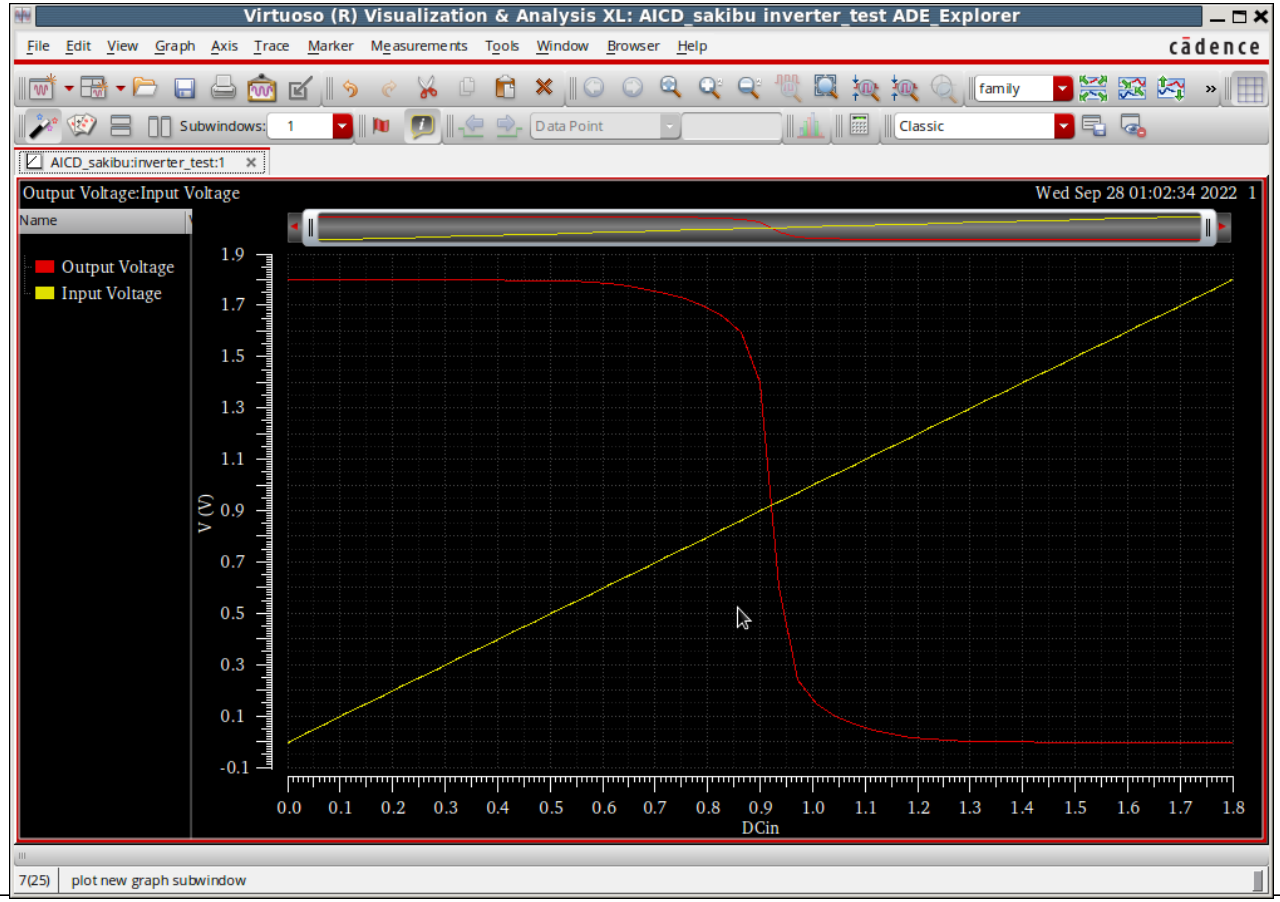
- Do the same for net *in*. Make sure *Plot* is checked for the signal expressions on ADE window. Add name according to the expression.





Simulation– ADE Explorer Setup

- Now our setup for the plotting of DC response is done. We can now run the simulation using the green run button (On the right side panel).
- After the simulation is done, the result will be shown by the input output characteristics plot like the one below:



Simulation– ADE Explorer Setup

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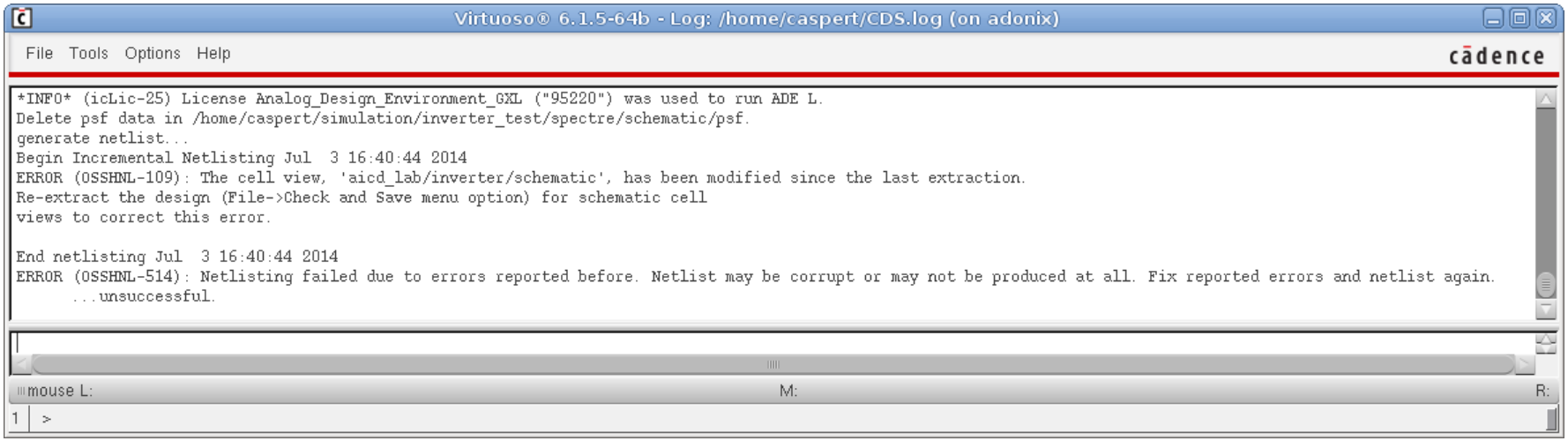
[Note: If nothing happens after starting the simulation, have a look at the main Virtuoso logging window (the first window that appeared when starting Virtuoso). A very common error is that one of the involved cells has not been saved before starting the simulation (in such a case, check and save all testbenches and cellviews being used by the simulation and try to run the simulation again). The screenshot below shows the Virtuoso logging window in this case.]



Simulation– ADE Explorer Setup

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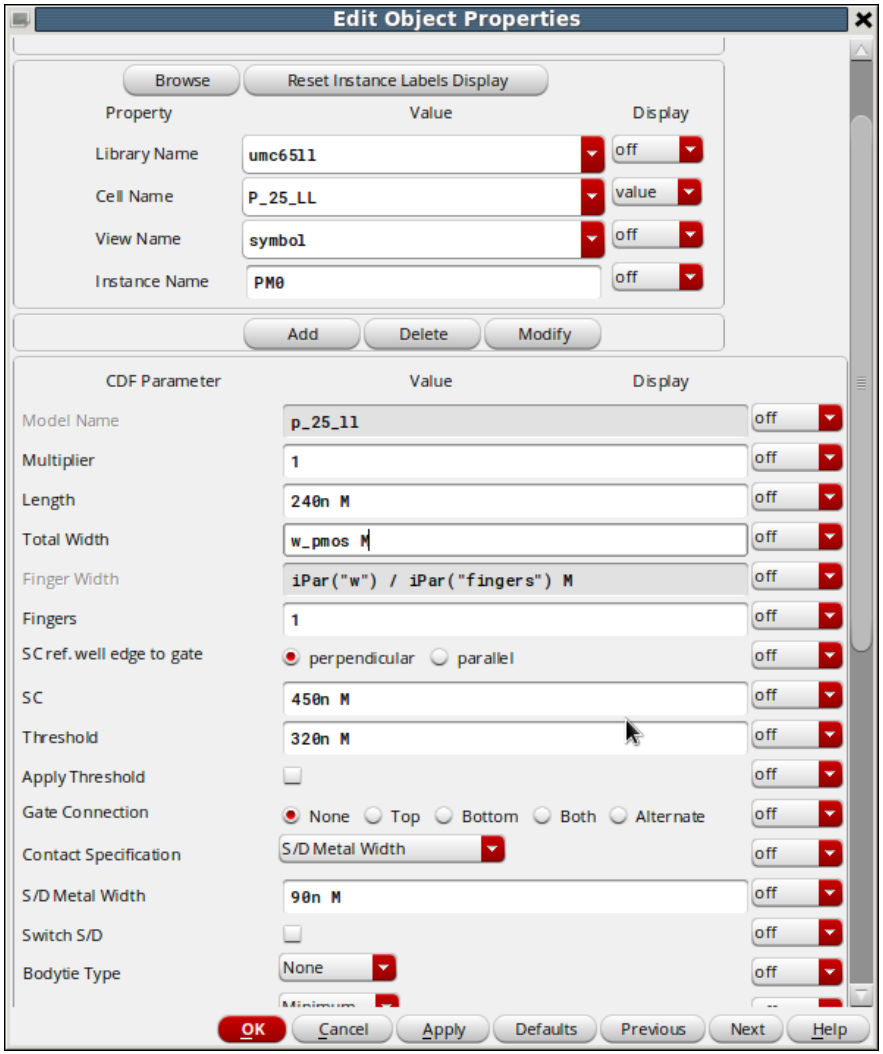
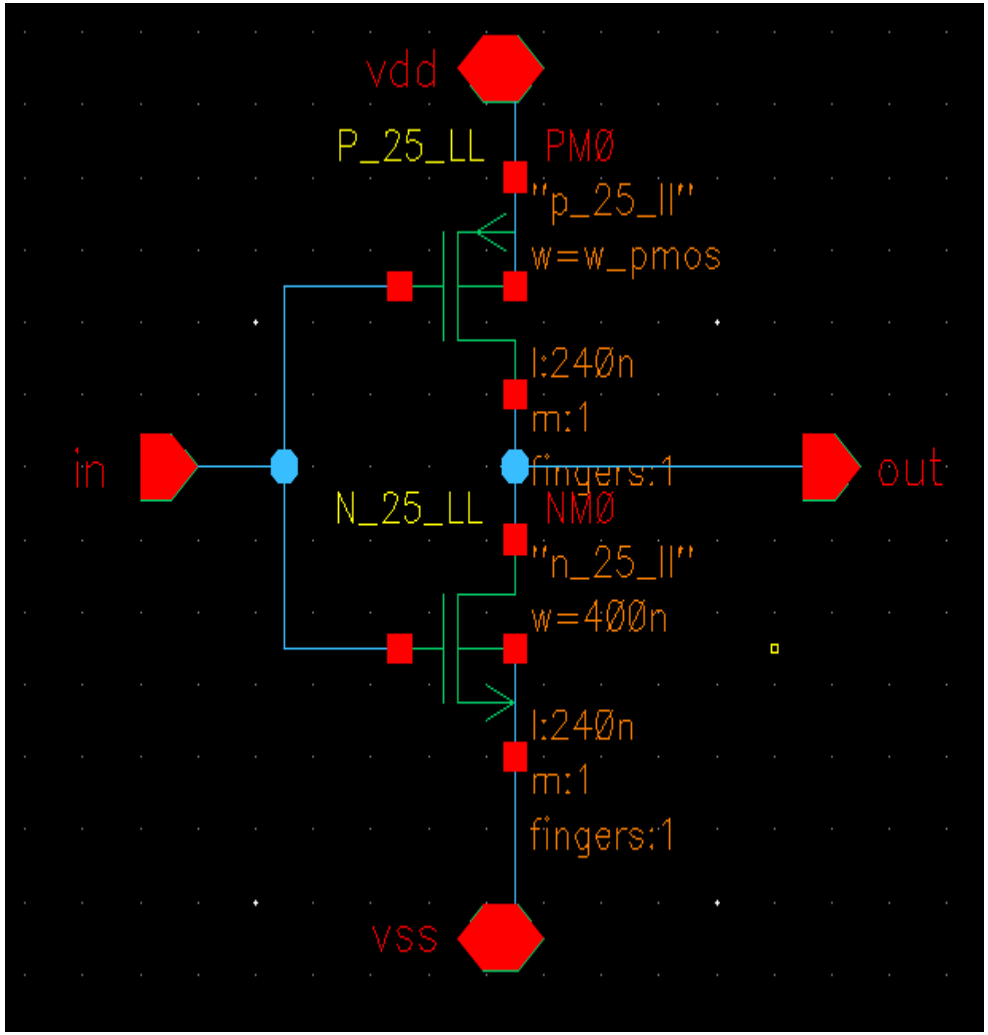
- At some point, you might be interested to annotate the DC operating point to your circuit by which you will be able to see the voltage and current flow on each node of your design. For this purpose, use the ADE window and go to *Results→ Annotate→ DC Operating Points*. In this menu you also find other useful options, give it a try!
- Now we have successfully completed the input output characteristics of the inverter. Let's now try something a bit advanced. Suppose, we want to see how the curve behaves once we change some parameters of a component. For example, we want to change the width of our pmos and see how the curve changes.
- To make the width of pmos a variable instead of a fixed value, go to your schematic, select the pmos and click *q*; which will bring the *Edit Object Properties* window.
- In *Total Width* section, write *w_pmos* and click *ok.*



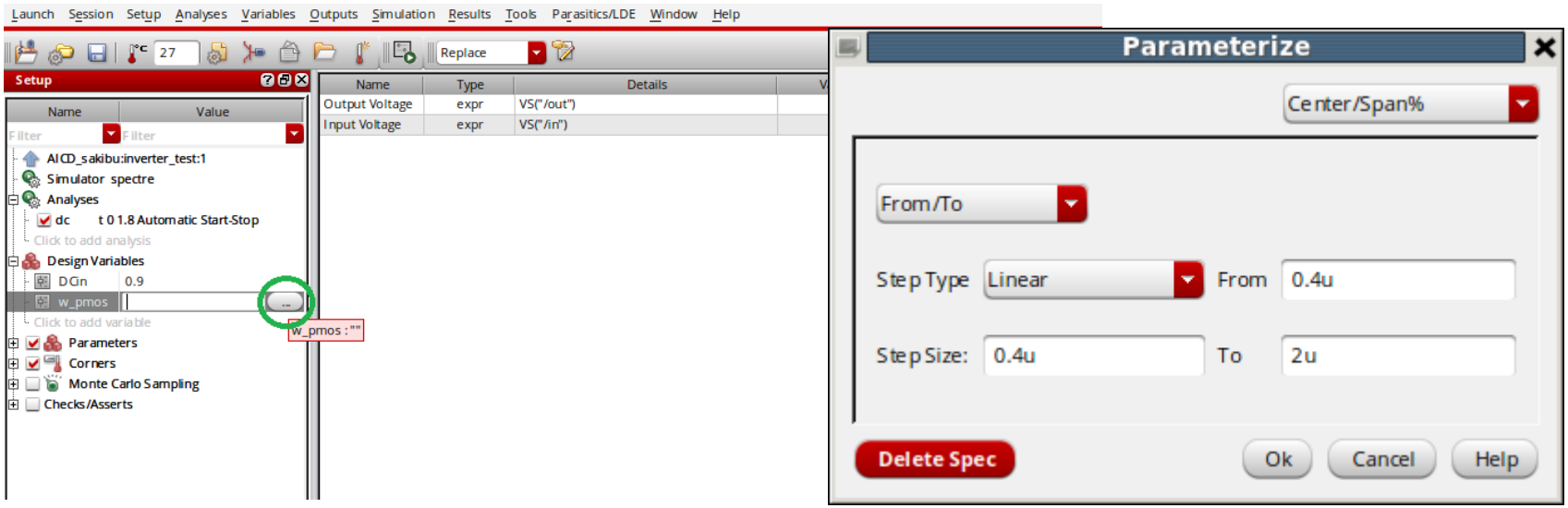
Simulation– ADE Explorer Setup

- The design will then look like the picture on the right, showing the width of pmos as *w_pmos*
- Now check and save your design and go to your ADE Explorer window.
- On *Design Variables* section, add the variable *w_pmos* (the same way as we added *DCin* as variable on page 21).



Simulation– ADE Explorer Setup

- To vary the width of the pmos, we want to sweep the *w_pmos* variable from 0.4um to 2um. For this, we will use the Parameterize option. Click *Design Variables* on ADE window. There you will find a button (marked green) from where you can access the Parameterize option. There you can sweep the input variables as per your requirements.
- We want a *Linear* type plot and lets say each *Step Size* is 0.4um, starting from 0.4um to 2um. Set the parameters under *From/To* option and after setting everything click ok. Now our setup for the plotting of DC response while varying the pmos width is done. We can now run the simulation again by clicking the *run* button.



Simulation– ADE Explorer Setup

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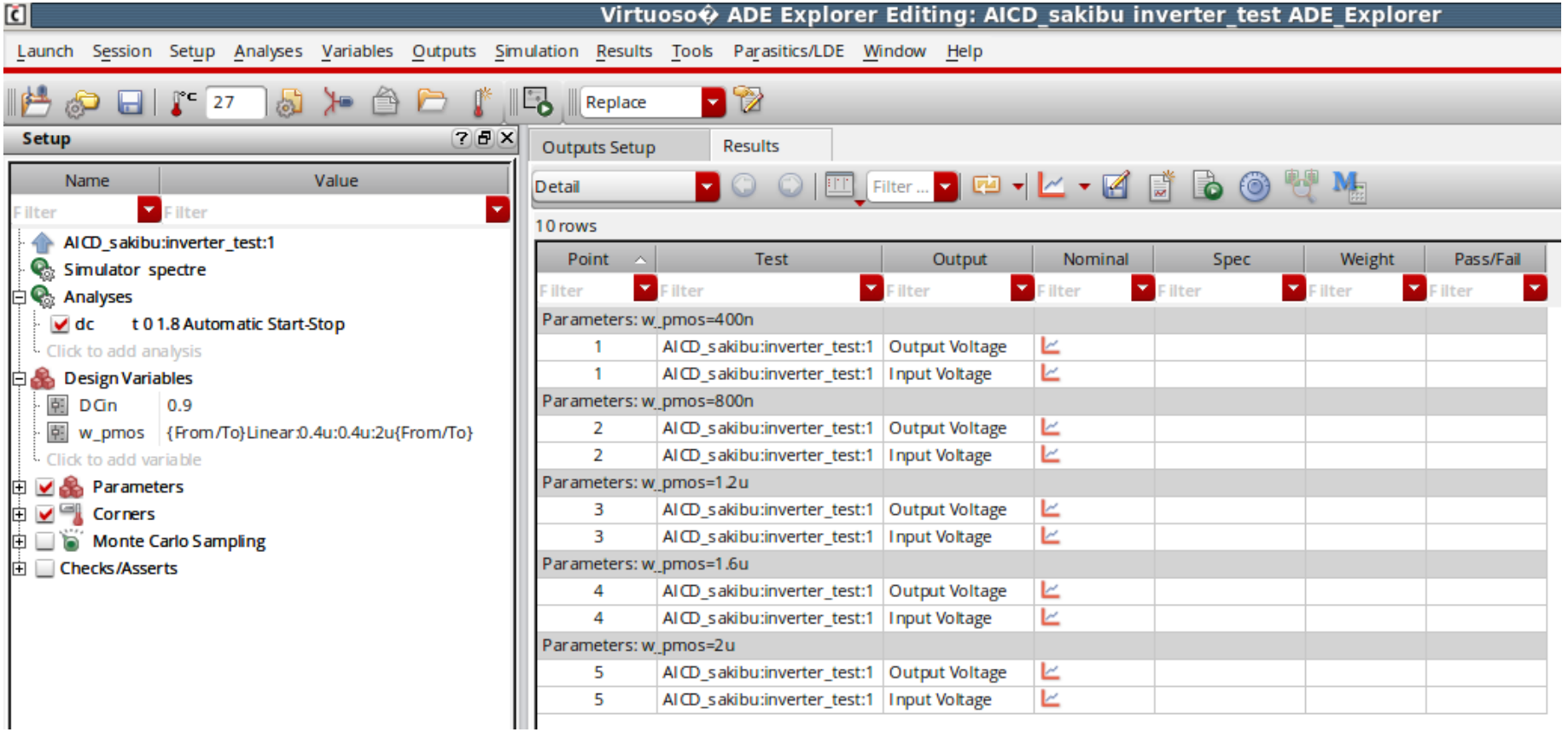
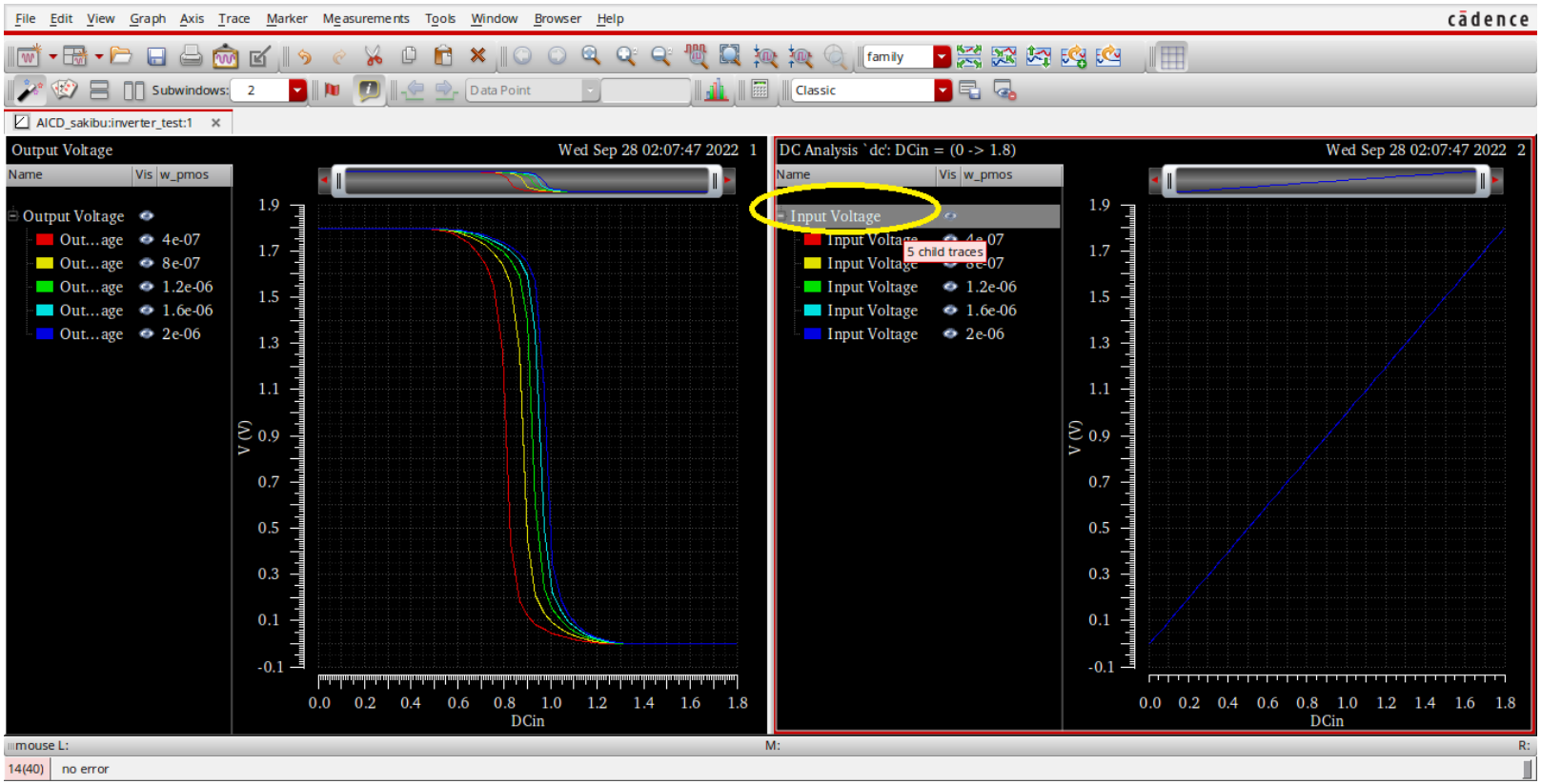
- After the simulation, the result window of the ADE Explorer will look like below:



Simulation– ADE Explorer Setup

- You will also get a plot like the below; which has output and input curves on separate sub-plot. To view it on a same plot, drag the input voltage plot(right sub-plot, marked yellow) and drop it on top of output voltage(left sub-plot).



Simulation– ADE Explorer Setup

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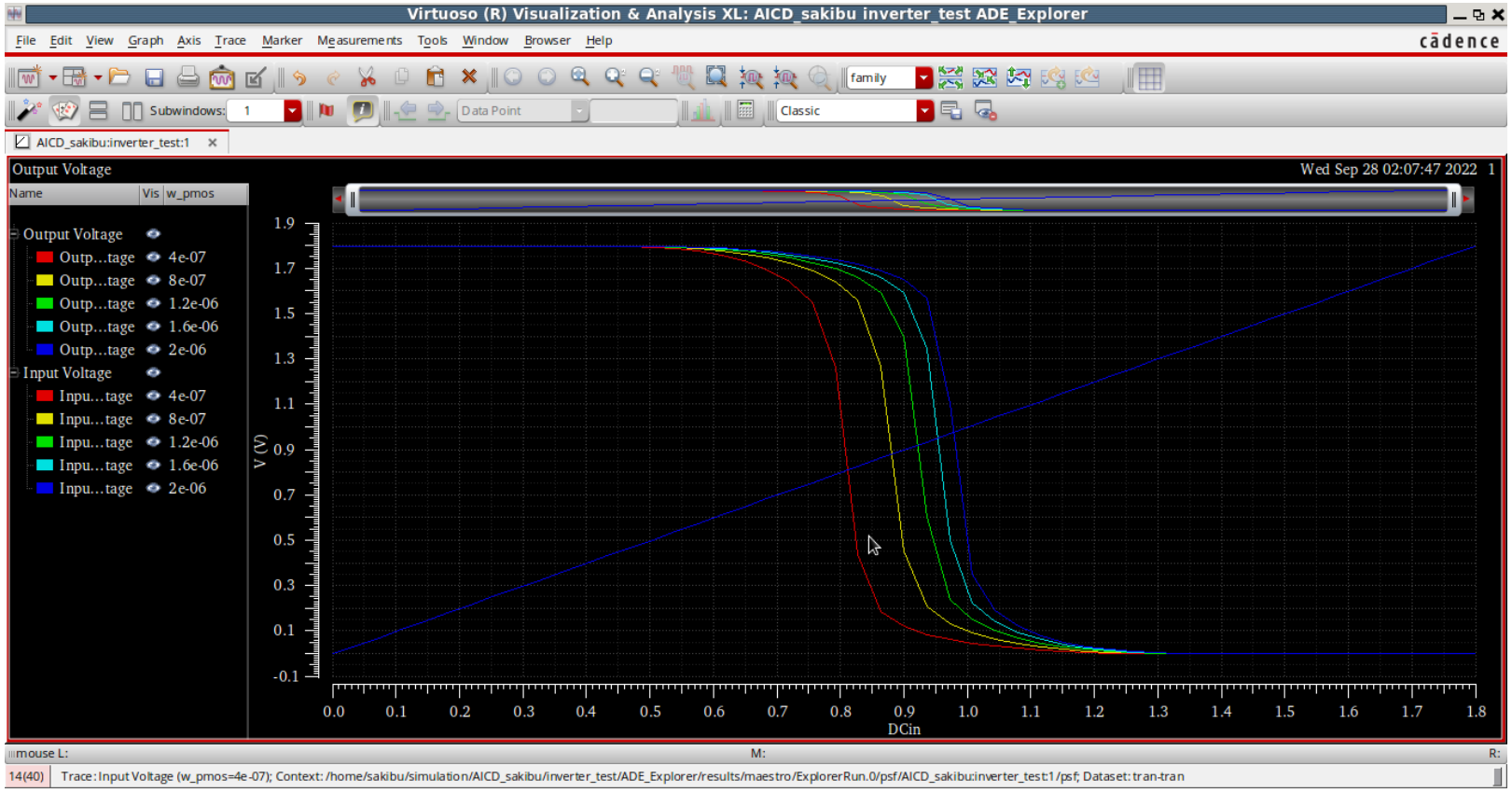
- After moving the input plot, both input and output will be together in a same plot. Now we can see exactly how the output voltages vary once we change the width of the pmos. Note that, the input voltage is same for all the cases, so it is overlapping with each other and showing as a single linear curve.



Simulation– ADE Explorer Setup

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- Now we have finished setting up the simulation state. Note that we have setup a DC analysis for the inverter testbench. In general, there are more analysis available. The important types of analyses which you will use during your design lab are:
  - DC Analysis:
    - DC operating point
    - DC transfer curves
  - AC Analysis:
    - Frequency response
    - Small-signal transfer functions
  - Transient:
    - Time (i.e. transient) response

- Attention: For the lab each group has to save their ADE Explorer sessions for all simulations, as described here! The saved sessions will be used by the lab tutor or supervisor to check the simulations and your design submissions.
- If you haven't saved the ADE Explorer sessions, your design will be deemed incomplete and will not be checked by the tutor/supervisor.

Finished!

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- You have finished the schematic and schematic level simulation tutorial now. This will be sufficient for the time being. We will continue with part 2 of the tutorial (which concentrates on the layout and post-layout simulations part of the design flow) after you have completed the schematic level design and simulations of the circuit you are designing

- To start with your own design, have a look at the OPAMP Design&Simulation.pdf in moodle. It guides you through the initial handcalculations and helps setting up the testbench for the Operational Amplifier