

Post Layout Simulation

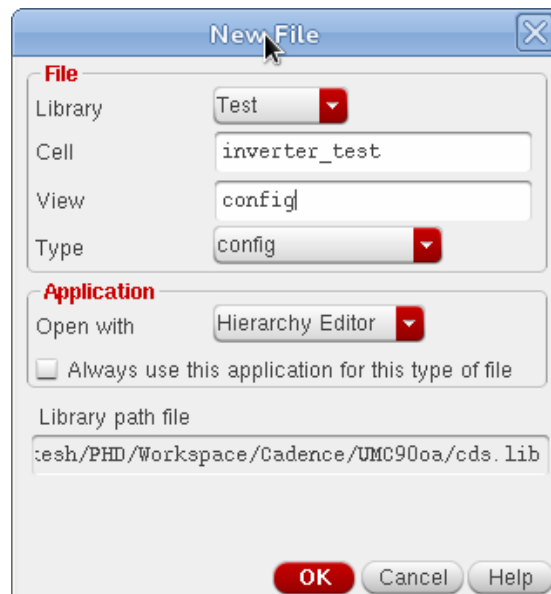
This document illustrates the approach to perform post layout simulations. Before starting with these steps, you are expected to have completed the schematic and layout for the block (in this tutorial we use an inverter), successfully created the parasitic extracted version and created the testbench (inverter_test).

Note: this document was created for the UMC 90nm technology. However, all the steps that are mentioned here are also valid for umc65ll technology node that you are using. Please ignore the references to UMC90oa.

Step 1

Create a new cell view (**config**) for inverter_test as follows:

File -> New -> Cell View and in the window that opens up select **config** as Type and click ok:



Step 2

In the new configuration window that opens up, select **schematic** in View and click on **Use Template** and select **AMS** as the template and click **ok**.

New Configuration

Top Cell

Library: Test

Cell: inverter_test

View: schematic

Global Bindings

Library List: ...

View List: ...

Stop List: ...

Constraint List: ...

Description

OK Cancel Use Template Help

Use Template

Template

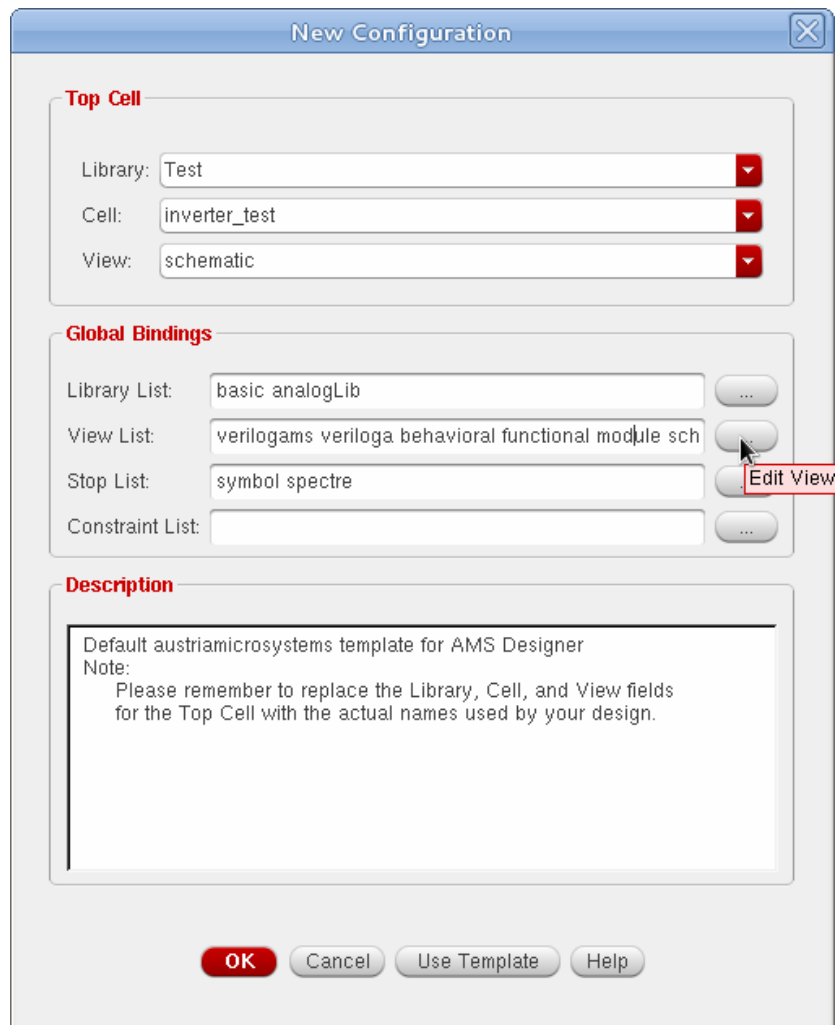
Name: AMS

From File: /home/sreelesh/hierEditor/templates/AMS

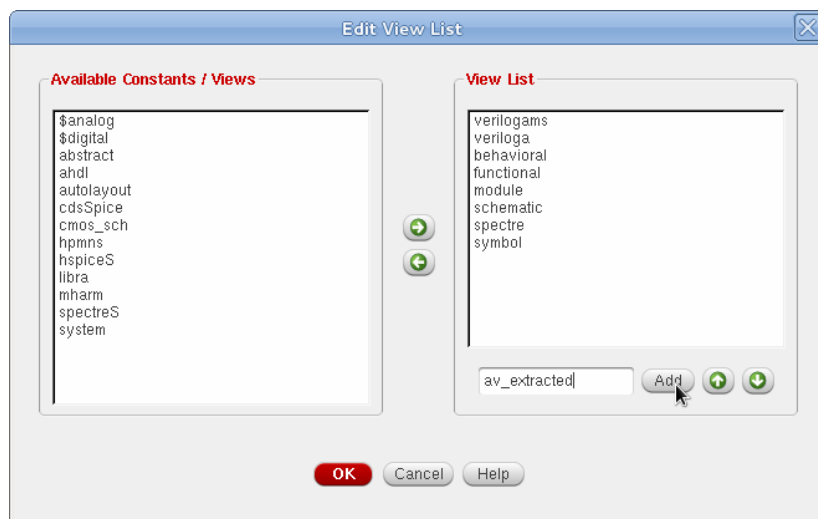
OK Cancel Apply Help

Step 3

After step 2, the New Configuration window looks as follows:

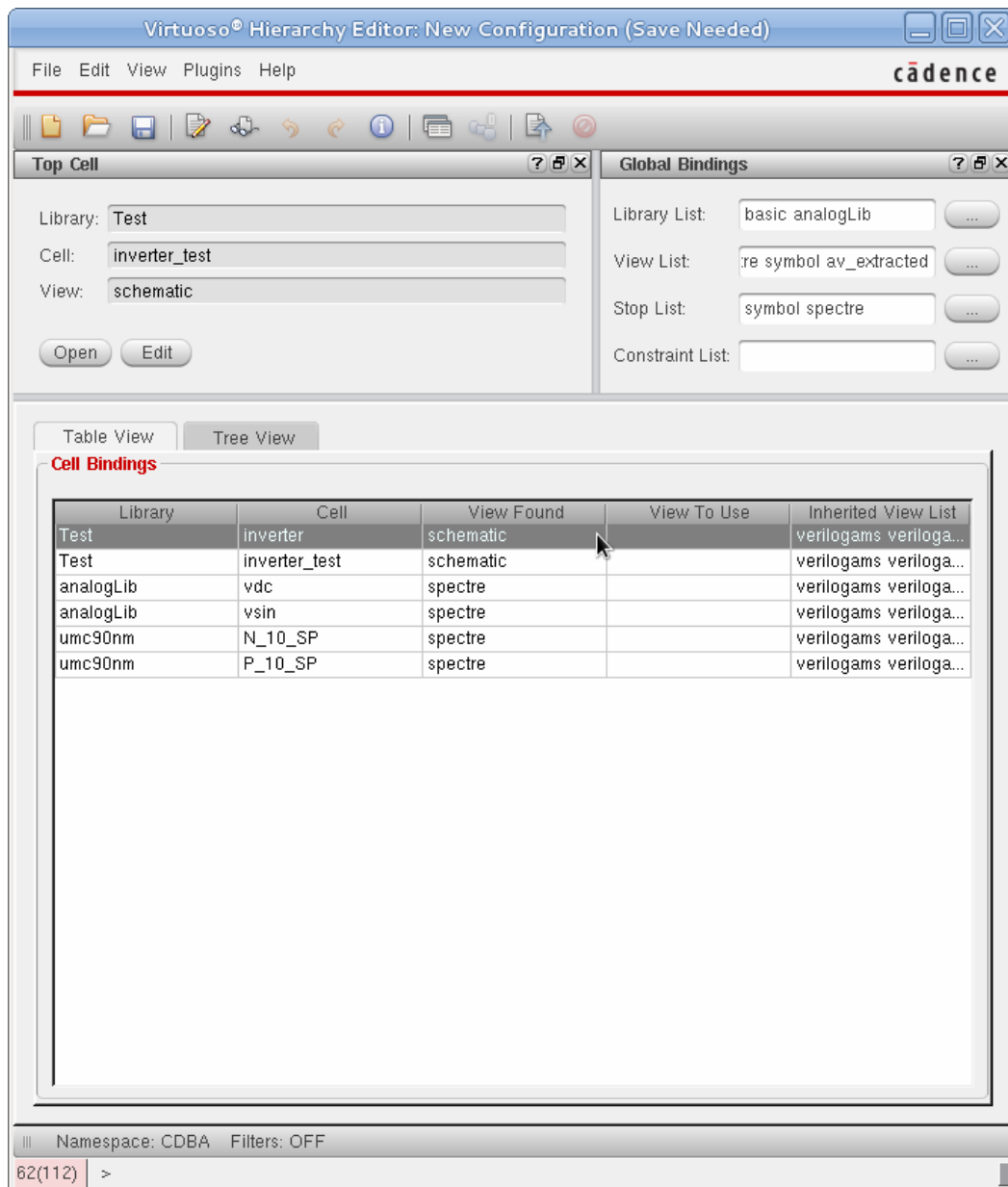


Click on **...** button at the end of View List option. A new window opens up. In this Edit View List window, type **av_extracted** and click on **Add** button as shown in below figure. Now click **ok**.



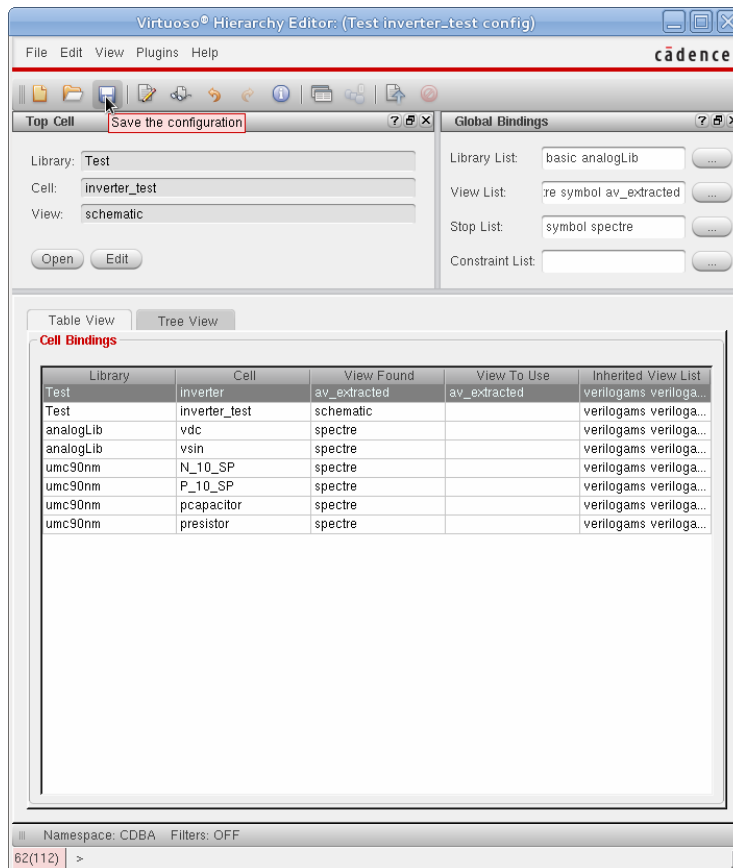
Step 4

After step 3, the following window opens up:

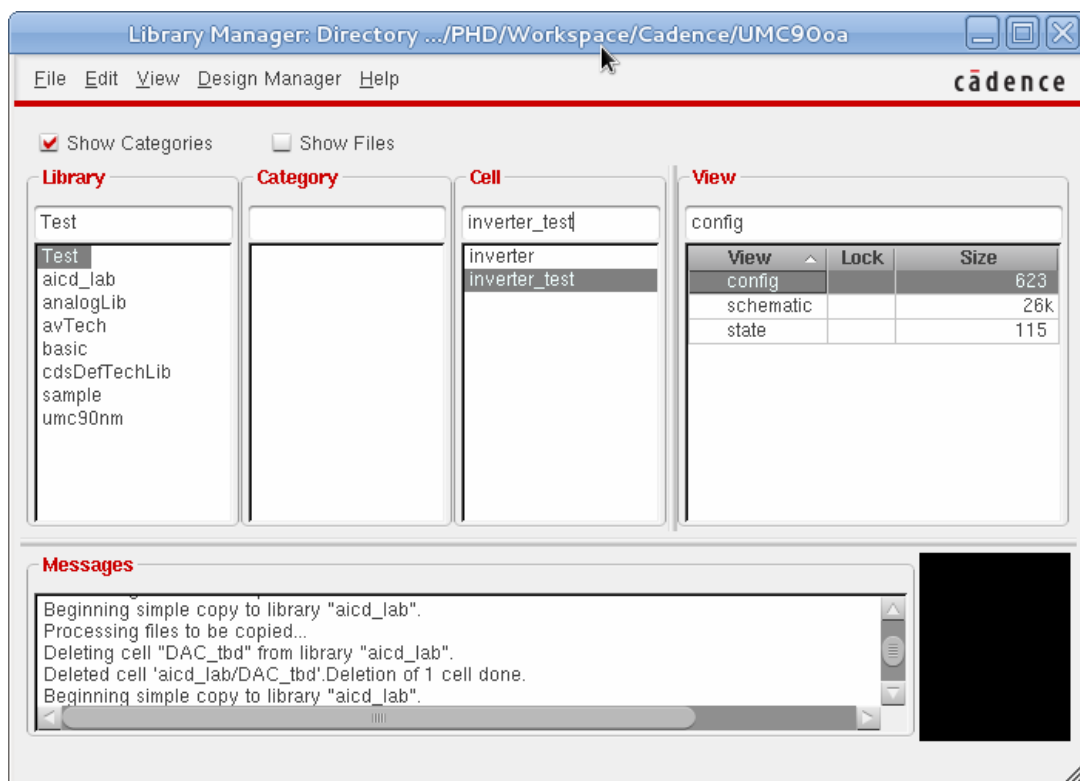


Right click on the cell inverter -> **Select Cell View** -> now you can see the different cell views for the cell inverter. It will show the option **av_extracted** if the inverter has been successfully extracted. It will also show the option **schematic**. Click on **av_extracted** for post layout simulation. (You can switch anytime between schematic and post layout simulation by selecting the appropriate option).

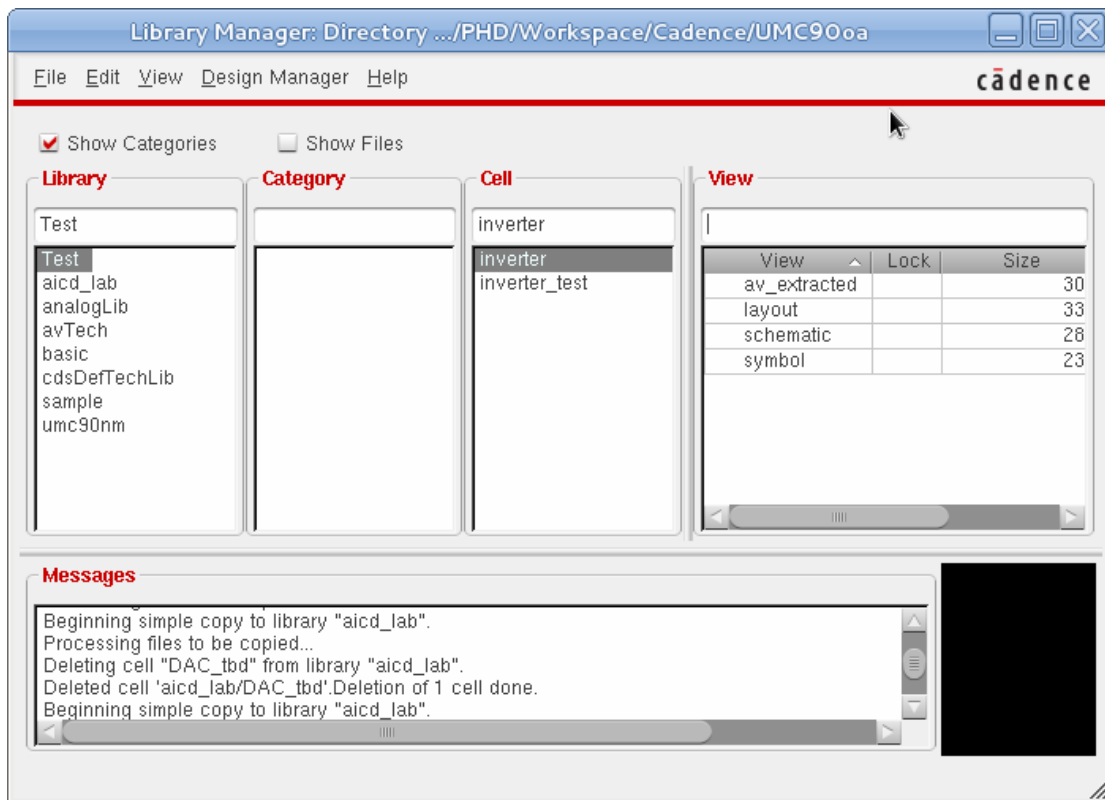
Save the configuration by clicking on **File** -> **Save**. Now the configuration has been successfully setup. The configuration will look as follows:



The inverter_test Cell would look as follows:



The inverter cell would look as follows:



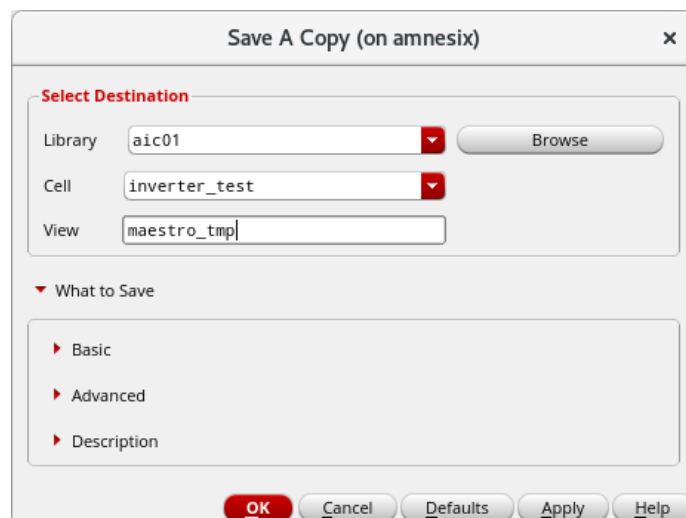
Step 5

The Analog Design Environment (ADE Explorer/Maestro) needs to use the config instead of the schematic. Since the ADE Explorer/Maestro resets itself when changing the design, we need to save it before and restore it afterwards.

Step 5.1

First save your current simulation setup as maestro_tmp.

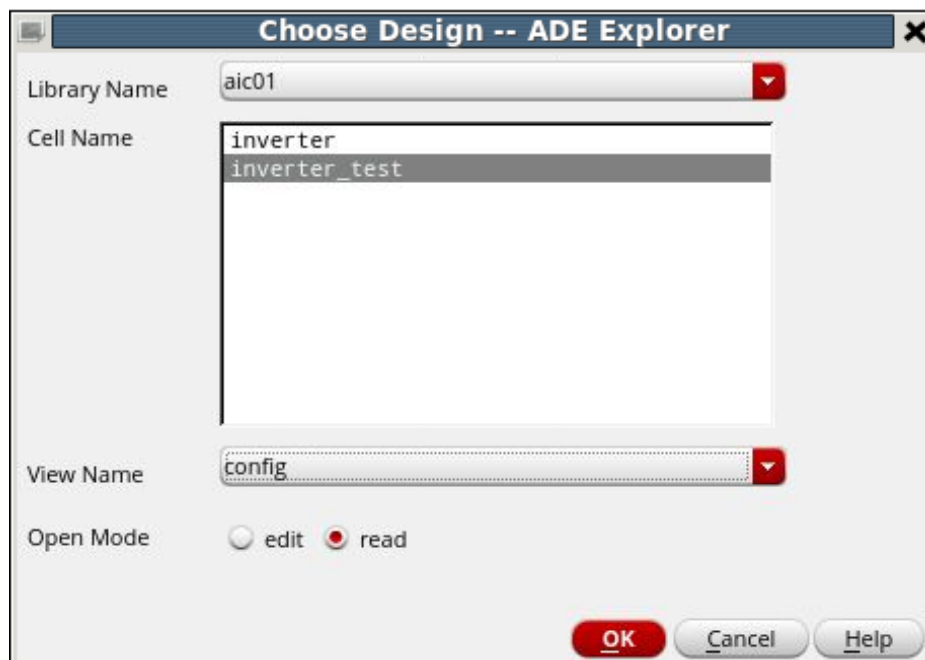
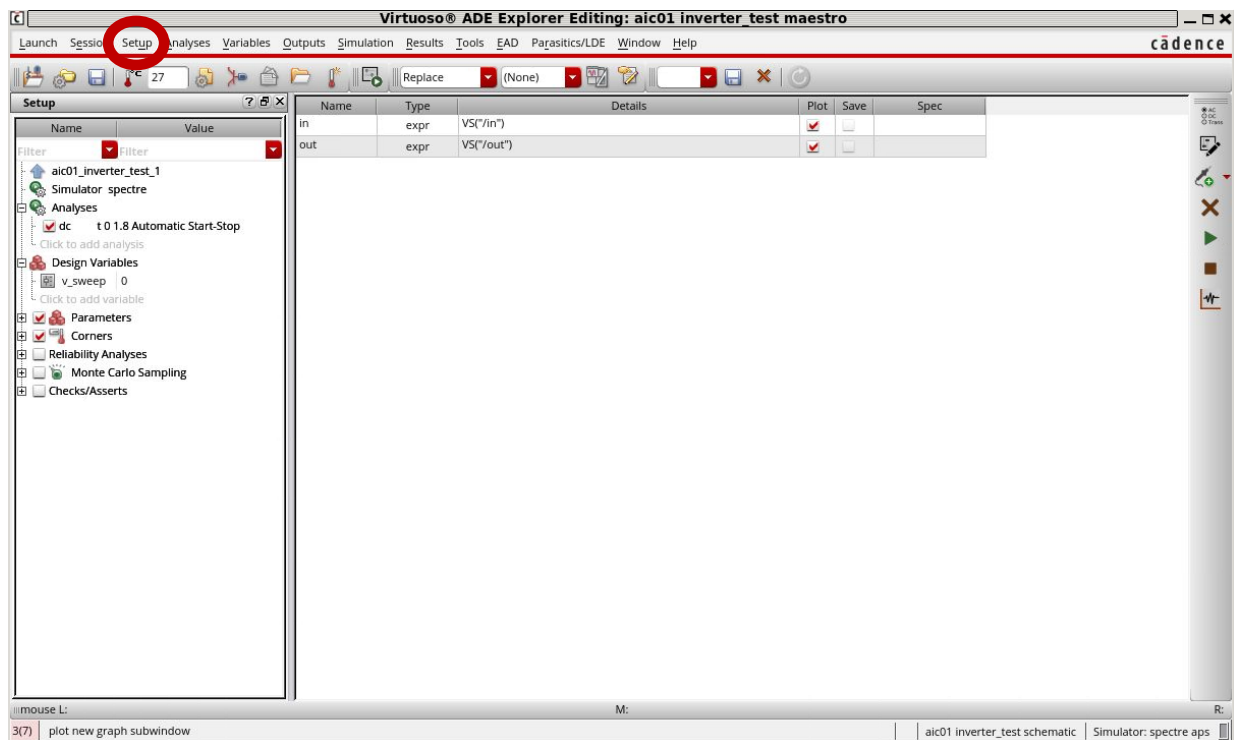
Go to **Session -> Save A Copy ...**



Step 5.2

Setup the simulation to use the newly created config.

Setup -> **Design** -> in the view name field **Config** -> click **ok**.



Step 5.3

Restore your old simulation setup. Go to **Session → Import ...** and choose your temporary copy from step 5.1 as shown below



The image shows a dialog box titled "Import Setup (on amnesix)". It is divided into two main sections: "Select View" and "What to Import".

Select View

- Library: aic01
- Cell: inverter_test
- View: maestro_tmp
- History: Active
- Test: aic01_inverter_test_1

What to Import

Basic

- ☒ Analyses
- ☒ Simulation Files
- ☒ High-Performance Simulation
- ☐ Specifications
- ☒ Outputs
- ☒ Simulator Options
- ☒ Variables
- ☒ Corners
- ☒ Model Setup
- ☒ Device Checking Setup
- ☐ Parameters

Advanced

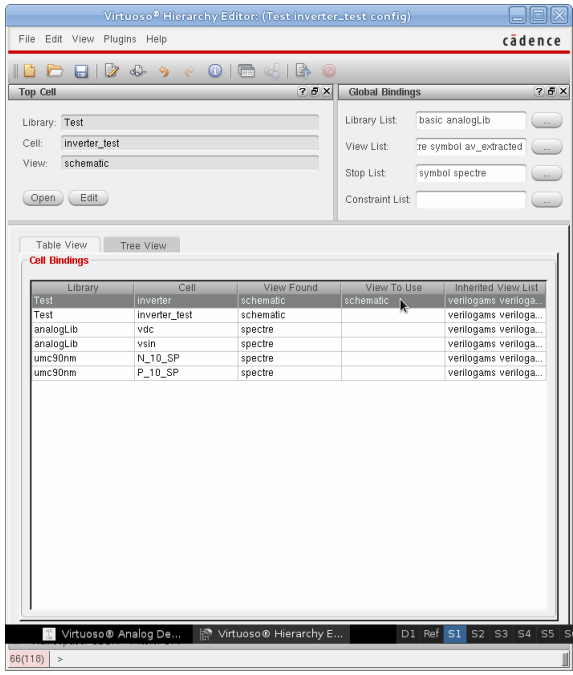
Description

Buttons: OK, Cancel, Defaults, Apply, Help

Step 6

The required setup for post layout simulation is now complete. Now you can run the simulations. To switch between the Schematic and post layout simulation, just change the selected cell view in the configuration window as follows:

Schematic Simulation



Virtuoso® Hierarchy Editor: (Test inverter_test config)

File Edit View Plugins Help

Top Cell: ? ? X Global Bindings: ? ? X

Library: Test
Cell: inverter_test
View: schematic

Open Edit

Library List: basic analogLib
View List: re symbol av_extracted
Stop List: symbol spectre
Constraint List:

Table View Tree View

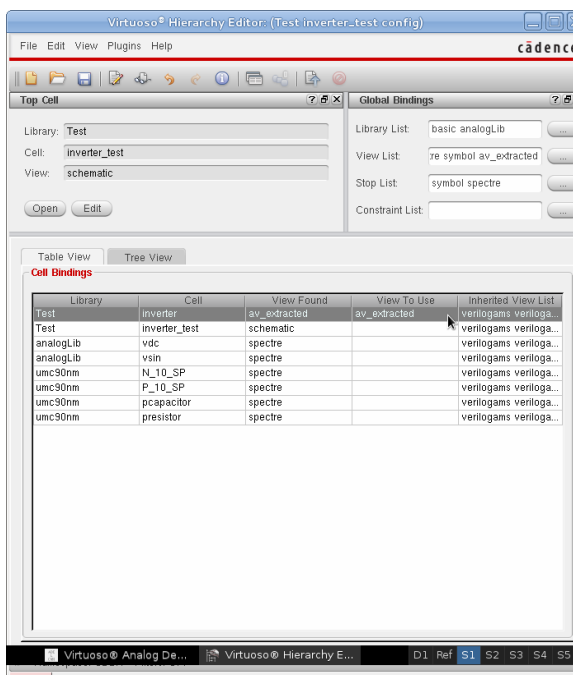
Cell Bindings

| Library | Cell | View Found | View To Use | Inherited View List |
|-----------|---------------|------------|-------------|--------------------------|
| Test | inverter | schematic | schematic | verilogams verilogams... |
| Test | inverter_test | schematic | schematic | verilogams verilogams... |
| analogLib | vdc | spectre | | verilogams verilogams... |
| analogLib | vsin | spectre | | verilogams verilogams... |
| umc90nm | N_10_SP | spectre | | verilogams verilogams... |
| umc90nm | P_10_SP | spectre | | verilogams verilogams... |

Virtuoso® Analog De... Virtuoso® Hierarchy E... D1 Ref S1 S2 S3 S4 S5 S

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Post Layout Simulation



Virtuoso® Hierarchy Editor: (Test inverter_test config)

File Edit View Plugins Help

Top Cell: ? ? X Global Bindings: ? ? X

Library: Test
Cell: inverter_test
View: schematic

Open Edit

Library List: basic analogLib
View List: re symbol av_extracted
Stop List: symbol spectre
Constraint List:

Table View Tree View

Cell Bindings

| Library | Cell | View Found | View To Use | Inherited View List |
|-----------|---------------|--------------|--------------|--------------------------|
| Test | inverter | av_extracted | av_extracted | verilogams verilogams... |
| Test | inverter_test | schematic | av_extracted | verilogams verilogams... |
| analogLib | vdc | spectre | | verilogams verilogams... |
| analogLib | vsin | spectre | | verilogams verilogams... |
| umc90nm | N_10_SP | spectre | | verilogams verilogams... |
| umc90nm | P_10_SP | spectre | | verilogams verilogams... |
| umc90nm | pcapactor | spectre | | verilogams verilogams... |
| umc90nm | presistor | spectre | | verilogams verilogams... |

Virtuoso® Analog De... Virtuoso® Hierarchy E... D1 Ref S1 S2 S3 S4 S5 S

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