Advanced Integrated Circuit Design Lab

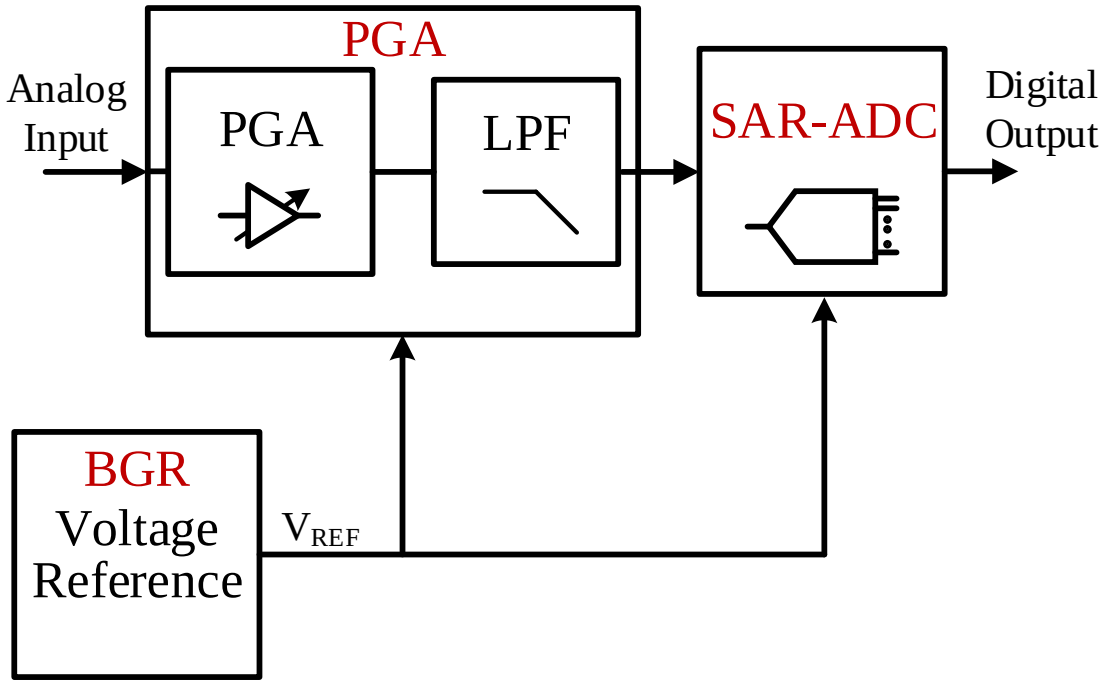
Project Description - Overview

TECHNISCHE UNIVERSITÄT DARMSTADT

System Overview

In this lab you will design a circuit part of an analog frontend.

A simplified block diagram of the analog frontend is shown below:



Design Tasks - Overview

TECHNISCHE UNIVERSITÄT DARMSTADT

This year, we will focus on the Bandgap Reference:

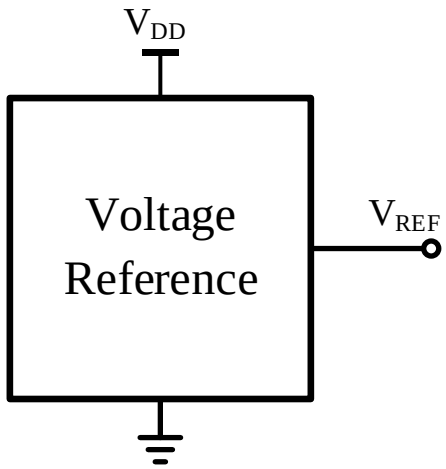
- Voltage reference using bandgap reference (BGR).
  - Refer *Task_Description_BGR.pdf*

Design Task - BGR

TECHNISCHE UNIVERSITÄT DARMSTADT

Bandgap Reference based Voltage Reference (BGR)

Voltage references are used to produce constant voltages for other circuits in a system. In case of the audio amplifier IC which we are considering in this lab, the voltage reference is used to produce a common-mode reference voltage (V_{REF}) for the 8-Bit Successive-Approximation-Register-ADC (SAR-ADC) and the programmable gain amplifier (PGA).



BGR - Architecture

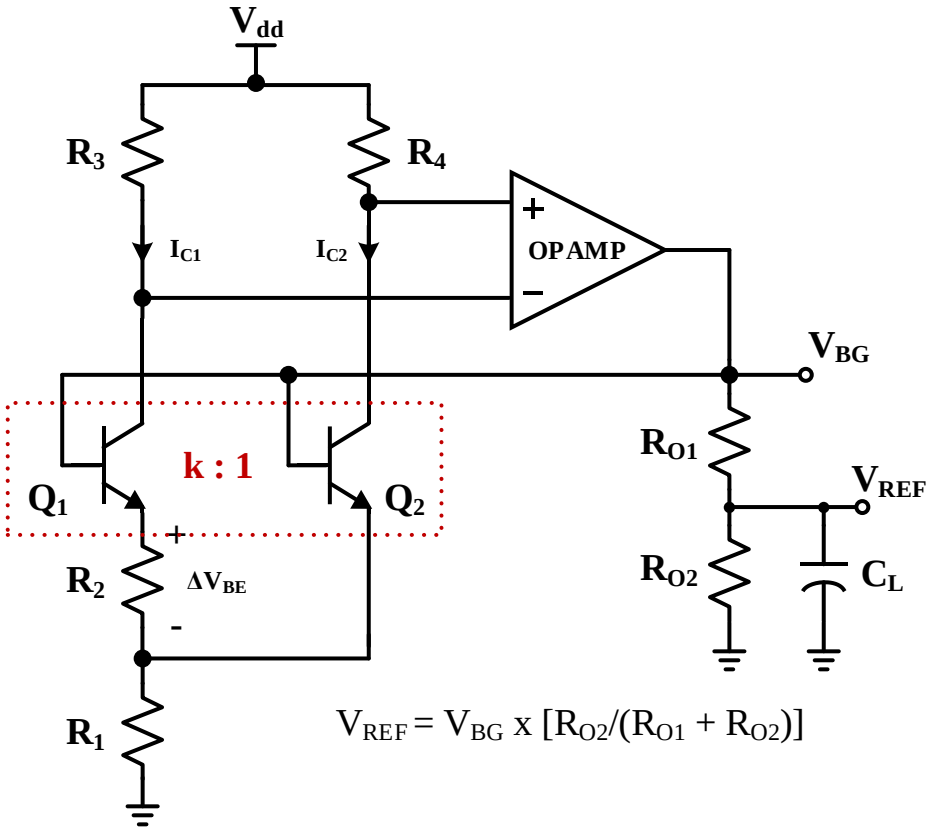
TECHNISCHE UNIVERSITÄT DARMSTADT

- The BGR circuit uses a Brokaw cell implementation to generate a reference voltage that is less sensitive to supply voltage, temperature and process variations.
- The circuit is based on the bandgap voltage of silicon to generate 1.205 V.
- This bandgap voltage can then be scaled to generate the reference voltage required for PGA and SAR_ADC.

The internal structure is depicted on the next slide.

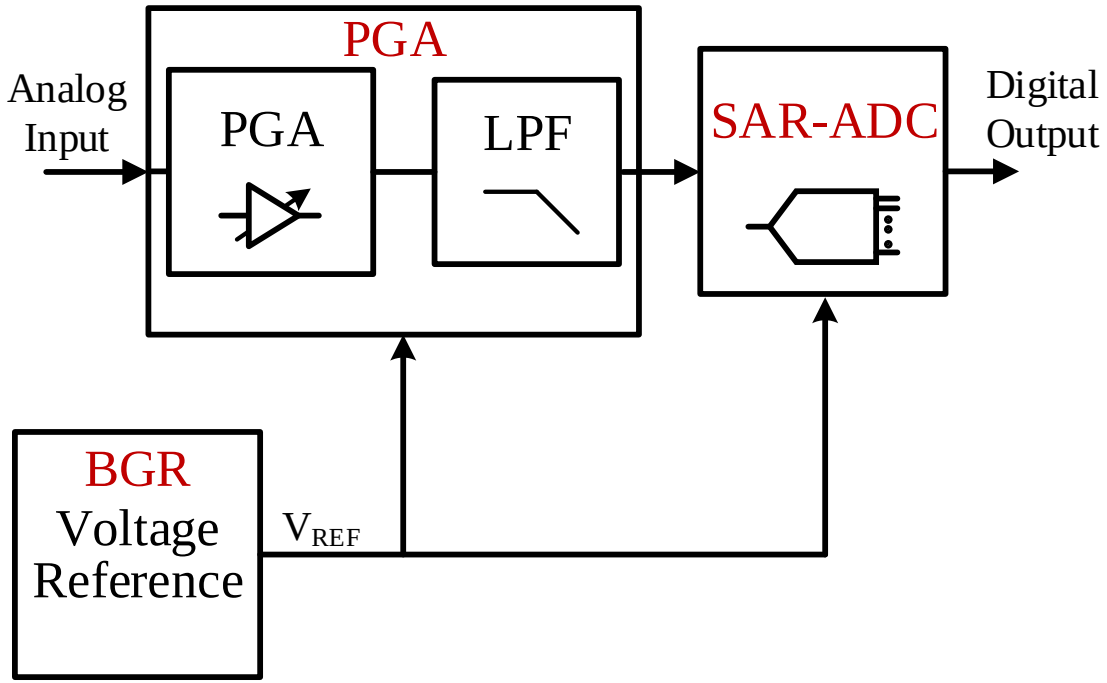
BGR - Brokaw Cell

- Use Brokaw cell configuration to generate the bandgap reference voltage and from that in turn generate the 0.9 V reference voltage required for the PGA and SAR-ADC.



System Overview

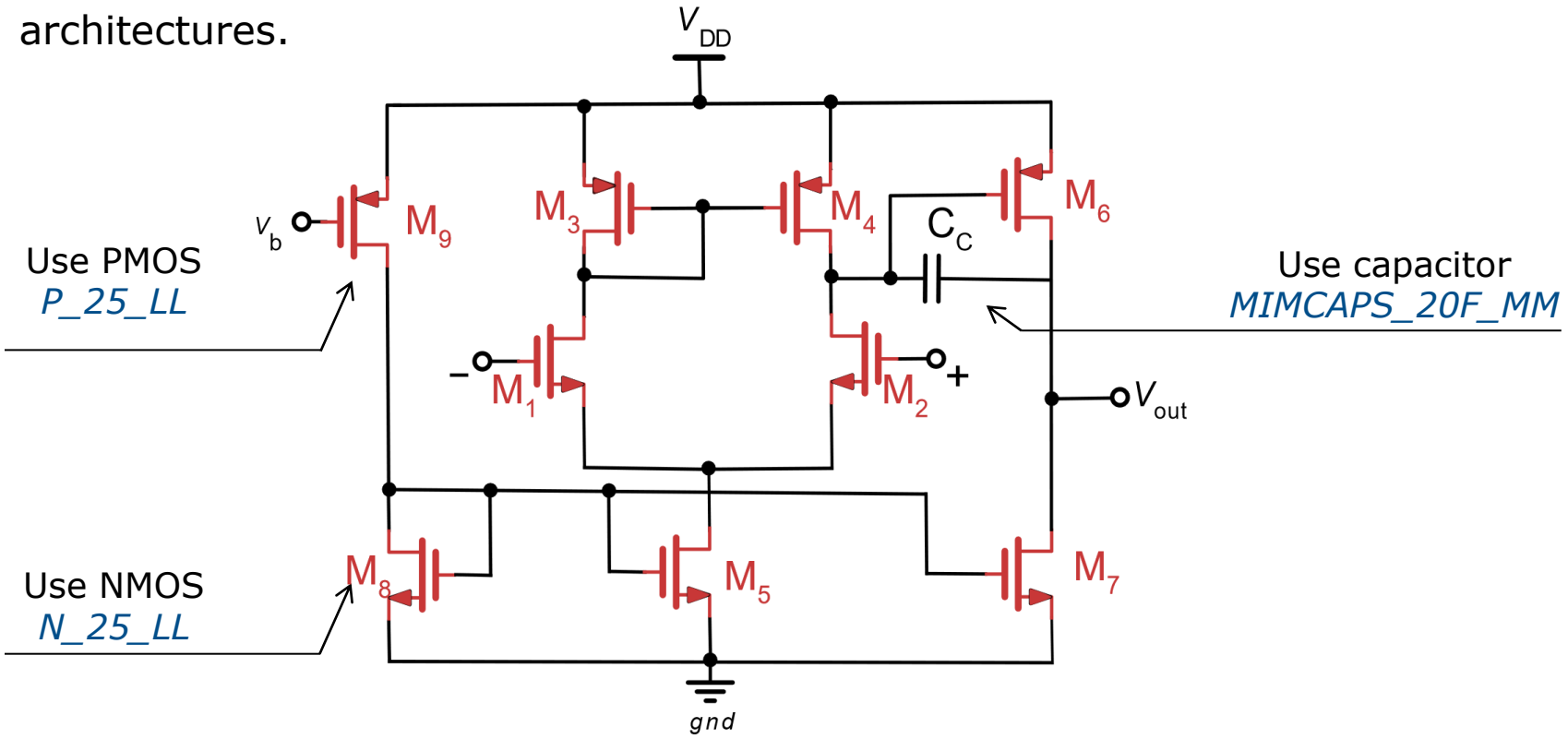
- Common feature amongst all the circuits is the OPAMP!



- We will consider a 2-stage Miller OPAMP design in this lab!

Two-Stage Miller OPAMP

- If you have prior design experience, please feel free to try other OPAMP architectures.



Please have a look at the following documents:

- *OPAMP_Overview.pdf* for an introduction to the OPAMP.
- *OPAMP_Design&Simulation.pdf* for some hints on the design and simulation of the OPAMP!

OPAMP Specifications

TECHNISCHE UNIVERSITÄT DARMSTADT

Parameter	Abbr.	Unit	Specification
DC Gain	Av	[dB]	> 50
Gain Bandwidth	GBW	[MHz]	≥ 20
Phase Margin	PM	[°]	≥ 55
Common-Mode Rejection Ratio	CMRR	[dB]	> 60
Slew Rate (+ve, -ve)	SR+ , SR-	[V/µs]	≥ 15 , 15
Settling Time @ 5 % error (high, low)	ST_{high}, ST_{low}	[ns]	≤ 500 , 500
Input Common-Mode Range	ICMR	[V]	0.5 … 1.3
Output Voltage Swing	-	[V]	0.3 … 1.5
Input Offset Voltage	-	[mV]	≤ 5
Input Referred Noise @ 20 kHz	$V_{ni,rms}$	[nV/$\sqrt{Hz}$]	≤ 55
Power Dissipation	P_{DC}	[mW]	≤ 0.6
Load Capacitance	C_L	[pF]	≥ 2
Supply Voltage	V_{DD}	[V]	1.8

**The given specifications are absolute minimum for typical corner post-layout simulations.*

Your design will be evaluated based on:

- How optimized it is.
- How power & area efficient it is.
- How well the specifications for Corner and Monte-Carlo analysis are met.

Where to start?

TECHNISCHE UNIVERSITÄT DARMSTADT

- Start with the cadence virtuoso tutorial (Next Session!)
  - ➢ *Cadence_virtuoso_tutorial part 1.pdf*

- Focus on the OPAMP first
  - ➢ *OPAMP_Overview.pdf*
    - Start with the initial Design
    - Create the testbench
  - ➢ *OPAMP_Design&Simulation.pdf*

- When your OPAMP is working continue with the task (BGR)

Suggested Books and Materials

TECHNISCHE UNIVERSITÄT DARMSTADT

- **CMOS Analog Integrated Circuit Design** by Allen and Holberg
- **CMOS Circuit Design, Layout and Simulation** by Baker
- **The Art of Analog Layout** by Hastings
- AICD/Elektronik and ADICD lecture slides
- Microelectronic Circuit Design by Jaeger
- Analysis and Design of Analog Integrated Circuits by Gray
- Analog CMOS Integrated Circuit Design by Razawi