1. OPAMP DESIGN

This chapter discusses some aspects of the two-stage Miller OPAMP design. First, we need to calculate initial sizes for all transistors using "hand calculations". Based on this starting point the OPAMP Design will be optimized using simulations until it meets all specifications.

1.1 Initial Design using "Hand Calculations"

For the initial OPAMP design we will start with "hand calculations". These are based on simplified equations of the two-stage Miller OPAMP.

For an in-depth explanation of the equations, please refer to the exercise 6 as well as the script of the Analog Integrated Circuit Design lecture ("Design of a two-stage Miller OPAMP")! This design procedure and all the equations are taken from the book "CMOS Analog Circuit Design" by Allen and Holberg, so you might have a look at this book as well!

Please understand the theory behind it. This will be important when you have to make modifications and optimize the design to satisfy the specifications. From the past years we have seen that students who blindly follow the automated tools for their calculations without having understood the theory/derivations behind it find it difficult to optimize their design when the required specifications are not being met.

For the "hand calculations", we already prepared a MATLAB Live Script. It guides you step-by-step through the initial design using the simplified equations. Based on your inputs, it will output the width and length of the individual transistors.

Starting the Matlab Script

Please connect to our remote server using the x2go client. To start Matlab open a Terminal and run the following command (with ## as your group number):

cd /home/aic##/AICD_lab_project

./start_matlab.sh

After starting Matlab, expand the folder *opamp_sim* in the file explorer on the left side and double click on *opamp_design.mlx* (Figure 1).

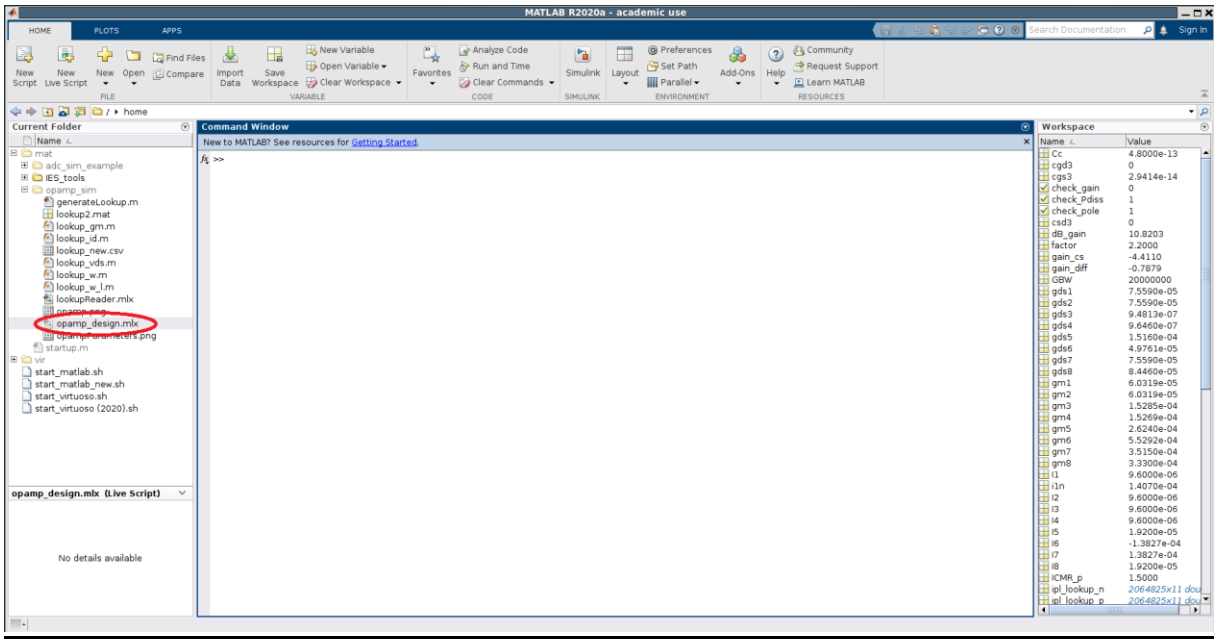


Figure 1: Matlab opening Window.

Run the Matlab Script

After loading the script, Matlab should look like Figure 2. For a better overview ensure that the Matlab code is hidden. You can change it on the top right in the Script window (Figure 2 red arrow). To run the script, you have to change a parameter, then the script will run automatically. To calculate your initial values for your OPAMP, just follow the steps in the script.

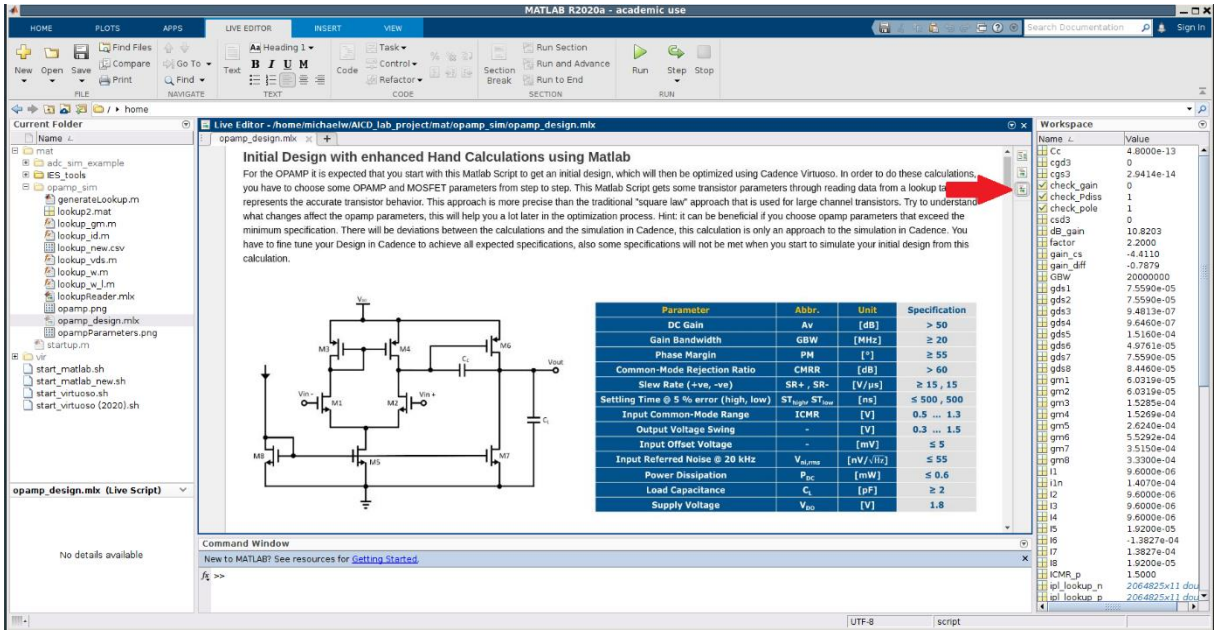


Figure 2: Matlab with loaded Script.

Attention: While designing the OPAMP using the Matlab Script, you might not be able to match all specifications initially. Do a few iterations, but please don't try to match all specifications simultaneously just by using "hand calculations" (with the help of Matlab Script in this case). That will not work in advanced technology nodes! The initial W/L values, which **satisfy most** of the OPAMP specifications should be sufficient to **get you started** with the Cadence Virtuoso simulations. From this starting point and the **knowledge** from the "hand calculations" you can then tweak the transistor sizes to optimize your design.

1.2 Adapted/Optimized Design using Cadence Virtuoso

Once you have your initial design from the hand calculations ready, you will use it as a starting point for working with Cadence Virtuoso. With the help of several simulations you will then be able to optimize and finalize the OPAMP design:

- DC analysis: offset voltage, power dissipation, ICMR, output swing,
- AC analysis: DC gain, gain bandwidth, phase margin, CMRR
- Transient analysis: Slew rate, Settling time
- Noise: noise

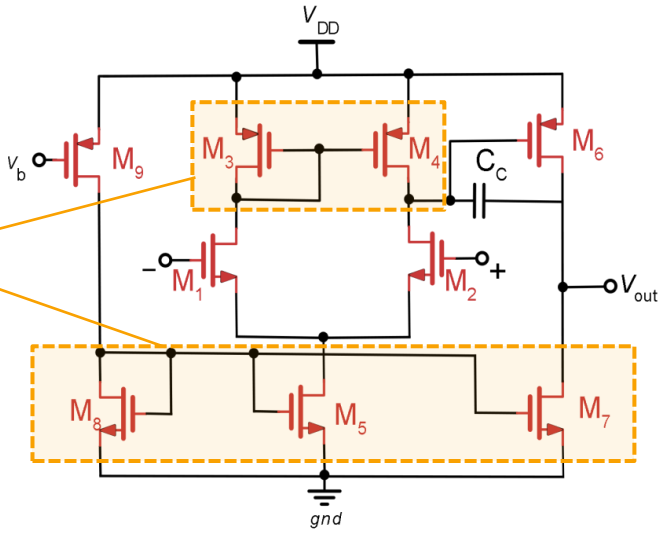
Chapter 2 will show you in detail how to simulate the OPAMP. Please use it as a guideline when simulating the OPAMP.

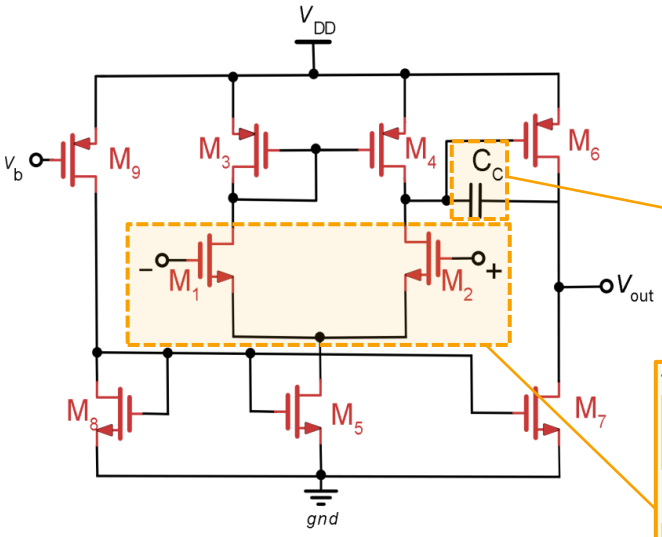
1.3 Some Hints on the Transistor Sizes and the Bias Voltage

Here are some hints on the W/L ratios for each transistor in the OPAMP. But be aware that these are only approximate suggestions and that you are free to modify and improve the design as you choose! As an example, the transistor lengths of the current mirrors need not necessarily be more than the minimum length as suggested below. It all depends on how you design your circuit!

High-strength current mirrors can be beneficial; if required use a length which is more than the minimum transistor length of 240nm.

Important: When you are no longer using L_{min} the threshold voltage will change!

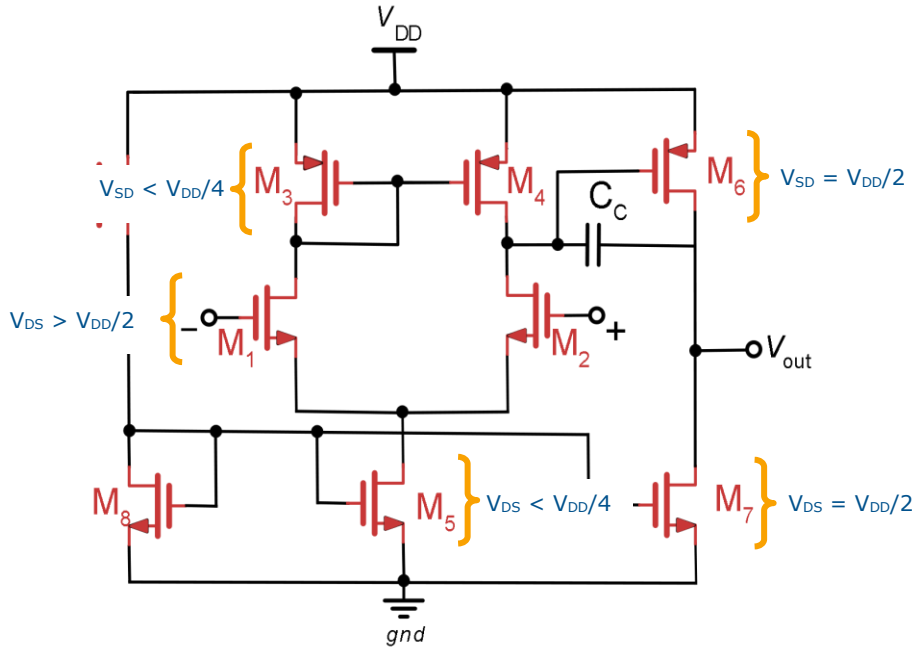




According to the equations, C_C should be larger than $0.22 \cdot C_L$. Use a C_C, which is say 2-3 times larger than $0.22 \cdot C_L$. In other words, assume a C_L that is larger than 2 pF, since this is only the absolute minimum load.

To achieve low noise and a low offset, the W/L ratio of the two input transistors should be rather large. If you get a very low value (W/L < 1) during the initial design, then readjust the parameters such that you get W/L >> 1. For example, if a bandwidth of 20 MHz gives W/L = 0.5, then increase the bandwidth until you get W/L >> 1.

Here are some hints on the V_{DS} voltages in the OPAMP to reduce the input offset voltage. The shown values refer to an OPAMP configured as a buffer and applied with a constant DC input voltage of 0.9 V relative to *gnd* (or 0 V relative to *gnda*). In other words, this configuration corresponds to the ICMR simulation test bench (see **Chapter 3**: OPAMP Simulation) with the only difference that there is no sweep, but a constant DC input voltage.



Tip: It is possible to display the DC operating points such as V_{DS}, I_{DS} or V_{GS} directly in your schematic view in Cadence Virtuoso. For this purpose, you have to set the

checkbox Save *DC Operating Point* in the DC analysis settings of the Analog Design Environment window. Then, after you ran the simulation, you can navigate to *Results → Annotate → DC Operating Points* and the values should show up in the schematic.

Remember, you also have to design a circuit that generates the bias voltage V_b for the OPAMP. The choice of the bias voltage depends on the size of the PMOS transistor M_9 and the current that is flowing through the current mirror below. You can balance transistor size against V_b to achieve the required current for the OPAMP. The circuit to generate the voltage V_b can be a simple resistive voltage divider or a transistor-based voltage reference. You are free to choose, which type of circuit you want to implement. You can even replace M9 with another circuit to achieve the desired biasing of your OPAMP. Keep in mind, that different supply voltages as well as temperatures and process will be tested by the corner simulation. Don't forget to discuss your decision and design in the written report!

2. OPAMP SIMULATION

This chapter will guide you through the simulation of the OPAMP. A testbench is used to apply stimuli for your device under test (the OPAMP). Then the simulator calculates its response. This is then analysed to check if the design fulfils all required specifications.

Before we start with the testbench and simulation, please start with general hints.

Plots & Expressions

After setting up the simulation, you will obtain the waveforms. You need to be able to read the characteristics e.g. ac gain, phase margin, gain bandwidth based on the plots. Furthermore, specific waveforms should be included in your written report.

ADE_explorer | testbench_opamp

Name	Type	Value	Plot	Save	Spec
DM Gain	expr	60	☑	☐	> 5C
ST+	expr	23.98n	☑	☐	< 500n
Output Noise	expr	9.992n	☑	☐	< 55n
Offset Voltage	expr	-2.37m	☑	☐	range -5m 5m
GBW	expr	21.88M	☑	☐	> 20M
CMRR	expr	80	☑	☐	> 6C
PM	expr	61.13	☑	☐	> 5S
SR+	expr	48.53M	☑	☐	> 15M
SR-	expr	48.41M	☑	☐	> 15M
input noise; V / sqrt(Hz)	expr	10n	☑	☐	< 55n

Figure 3: Example of an output window with numerical expressions for some important specifications.

While one can manually read the specifications (e.g. gain) from a few waveforms during the optimization phase, this is unfeasible for Corner or Monte Carlo runs. These require obtaining the performance for hundreds or thousands of simulations. So-called expressions are used to compute a numerical value from the waveform. They can be automatically checked against the specification. All passed specifications are highlighted in green as shown in figure 3. Failed specifications are highlighted in red. If the failed specification is close and just missed by 10% or less, it is highlighted in yellow.

Setting up expressions can be quite error-prone. When relying on faulty expression your design optimization can be flawed. To check if your expression is set up correctly you can simply compare its numerical value with a manual reading of the waveform.

The library *Demo_oamp_verilogA* contains a cell *opamp*. This is an idealized OPAMP based on verilogA code. Its performance resembles OPAMPs designed in this lab. Nevertheless, not all effects of real transistor circuits are included.
You can use this *opamp* for the development testbench. It allows you to start with the testbench, while your partner works on the OPAMP initial design and schematic entry.

Also, it is an easy way to verify your testbench. Since the performance of the verilogA OPAMP is known, just compare it with the result from your testbench.
For further details, please see chapter 3. The performance is listed in table 2.

2.1 Power Supply for the OPAMP Test Benches

While most digital circuits use a single power supply, i.e., *vdd* referenced to *gnd*, many analog circuits, especially OPAMPs are powered by a split power supply, i.e., *vdd* and *vss* referenced to *gnd*. In this document, we will use *vdd* and *vss* supplies and set *vdd* to 1.8 and *vss* to *gnd*.

The *umc65ll* technology supports a I/O supply of *vdd* = 1.8 V, 2.5 V or 3.3 V. For this lab we will use a supply of 1.8 V and a "negative" supply of 0 V (*vss=gnd*). In order to simulate the OPAMP characteristics we need to redefine the single supply using the analog ground concept, hereby making the single supply (0 V, 1.8 V) look as if it is a split supply (–0.9V, 0.9 V). This analog ground voltage can be defined by changing the DC bias point to half the supply range. That is, define a common-mode voltage *vcm*= 0.9 V. *Vdd* is positive relative to *vcm* (+0.9 V) and *vss* is negative with respect to *vcm* (–0.9 V).

Single Supply	
Vdd	+1.8 V
Vcm	+0.9 V
vss(= gnd)	0 V

Table 1

Use the following diagram for the power supply in OPAMP testbench schematics. Make sure all your stimuli signals are centred at *vcm*.

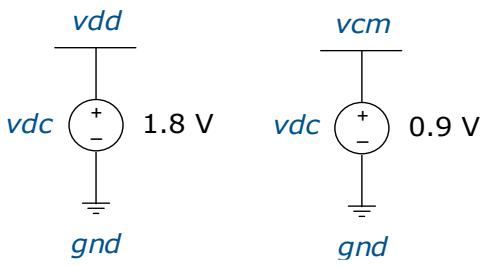


Figure 4: Setup for OPAMP's Power Supply.

Attention: Always tie the substrate to the most negative voltage in the circuit. In our case this is *vss* and not *vcm*.

2.2 Input Offset Voltage, Gain, Gain Bandwidth, Phase Margin and CMRR Measurements

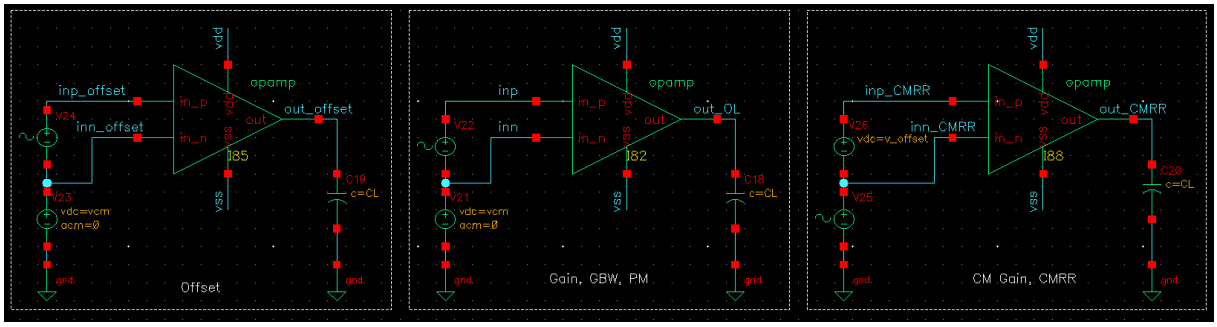


Figure 5: Testbench for all measurements in this section.

2.2.1. Offset Measurement

The value of the input offset voltage of the OPAMP will be needed for other measurements (for ex. CMRR), hence let's measure it first.

DC analysis:
v_offset: Voltage sweep from -0.05 V to +0.05 V

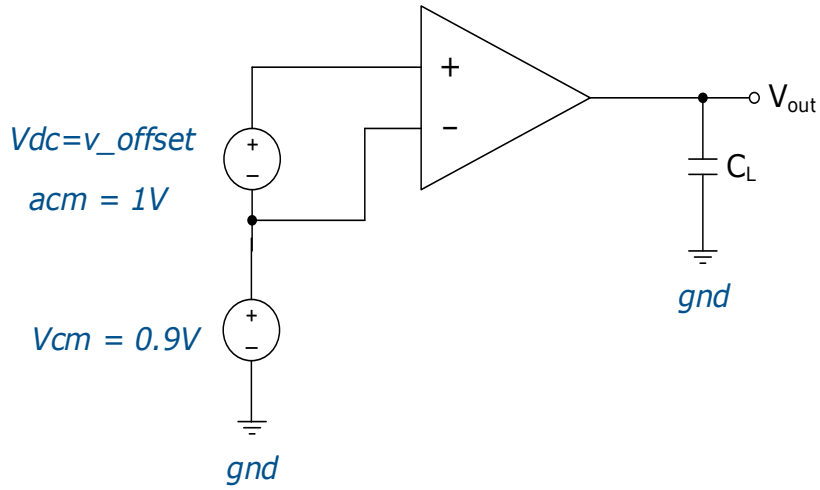


Figure 6: Setup for Offset Measurement.

Tie the negative input of the OPAMP to *vcm* and connect a DC voltage source to the positive input terminal, as depicted in Figure 6. We will perform a DC sweep of the input voltage (value = *v_offset*), while observing the output node. First, sweep *v_offset* from –0.9 V to +0.9 V. You will see the output voltage swing (refer Figure 7) between its minimum and maximum values (output voltage swing specification!).

Now concentrate on *v_offset* sweep over a very small voltage range. In other words, zoom in on the interesting part of the output voltage curve – the quick

transition from minimum to maximum output. Make sure you have used enough points in your simulation to observe this transition region in great detail! As an example, sweep from -50 mV to +50 mV and use step size of 100u (always use step size which are at least 100 times smaller than the total sweep range). The -50 mV to +50 mV range is just an example. Depending on your design, you might probably need to use a smaller/larger range than this to see the slope clearly.

From this simulation we can specify the input offset voltage of the OPAMP. The input offset voltage is the differential input voltage, which leads to an output voltage equal to zero. Ideally, this offset should be zero. What is the input offset voltage of your OPAMP? Calculate the point from your plot.

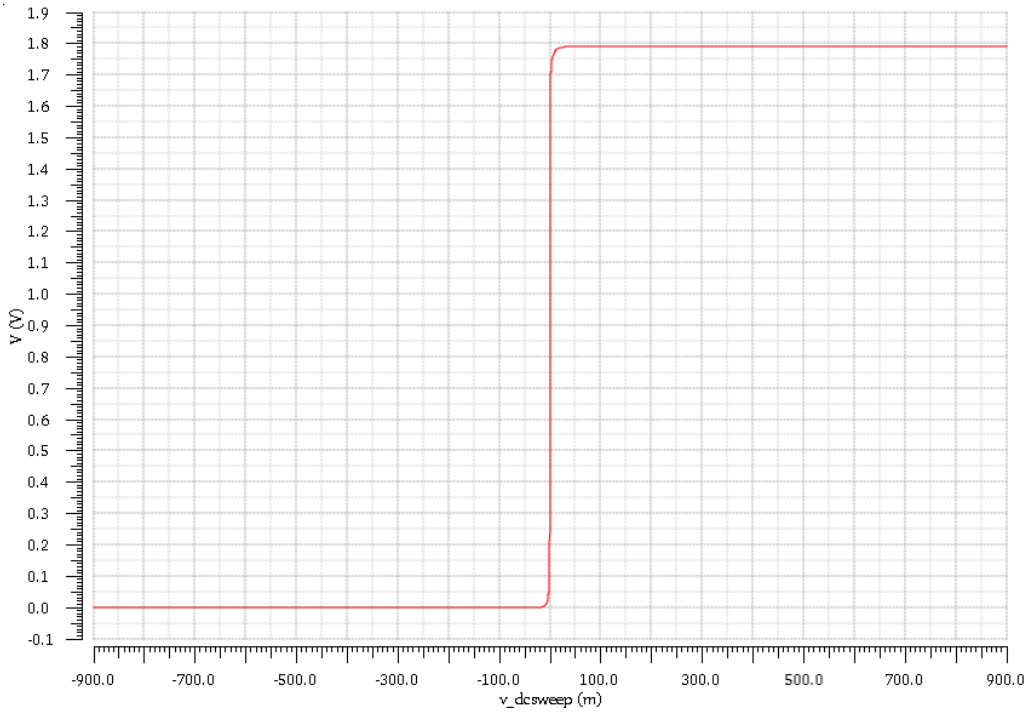


Figure 7: Exemplary waveform: Output Voltage Swing

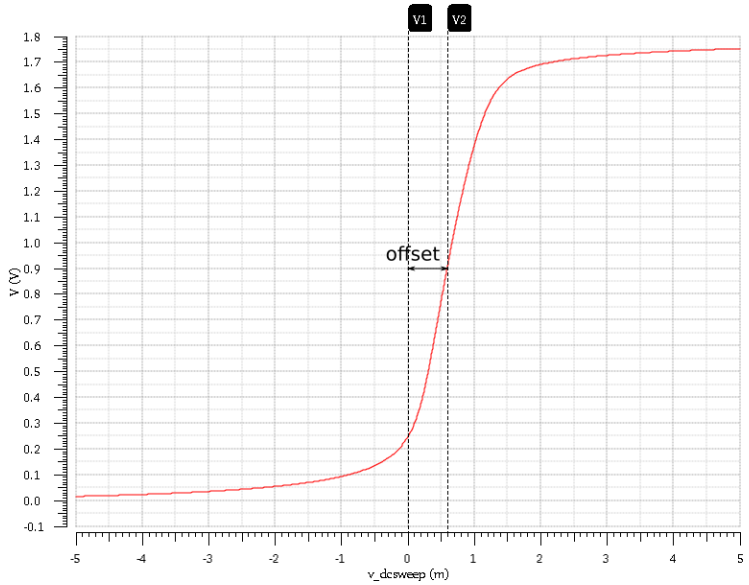


Figure 8: Waveform: Input Offset Voltage Measurement.

The input offset voltage measured in the previous problem is very useful for the measurements we are about to make. For these measurements, we want the DC level of V_{out} to be very close to zero, since this is the typical value the output will have in closed-loop circuits, assuming the input is centred at *vcm*. However, we need to make our measurements in the open-loop condition, so we have to balance the high-gain OPAMP very carefully to keep the DC of V_{out} at approximately *vcm*. We do this by adding a DC voltage source to the positive input of the OPAMP.

Run a DC simulation to verify that V_{out} is approximately equal to 0.9 V relative to *gnd* (or 0 V relative to *vcm*) before continuing with the following measurements.

Calculator Setup:

- Offset: Use cross function.

→ ***Include the plots and the measured offset voltage in your report.***

2.2.2. Gain, GBW & PM Measurements

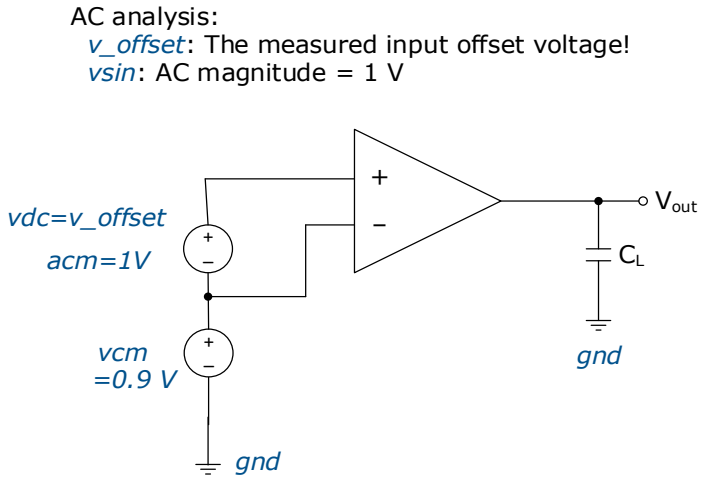


Figure 9: Setup for Gain, GBW and PM Measurement (Use schematic in Fig. 4)

Now we are ready to measure the open-loop gain and phase of the OPAMP as a function of frequency, i.e., the transfer function of the OPAMP. Add an AC voltage source *vsin* to the positive input terminal of the OPAMP (in series with *vdc* for the offset). We are going to sweep the frequency of this input sine wave and measure the amplitude and phase of the output voltage. What should the amplitude of this input voltage be? You might think that we would have to keep the input voltage amplitude very small. After all, the open-loop gain of our OPAMP is very high, so a large voltage at the input would surely saturate the output at the limits you measured previously.

However, since we are going to perform an AC simulation, it actually doesn't matter what the amplitude is. When you perform an AC simulation, the simulator first calculates the DC operating point (with all AC sources set to zero), which is why it's important to set the offset voltage correctly. From this DC operating point the simulator then constructs a linear, small-signal model of the circuit, just as you have done in some of your lectures. Since this small signal circuit is linear, it doesn't matter what the AC voltage levels are. If the OPAMP has an exemplary gain of 5000, you could use an AC signal with amplitude of 2 V and the simulation would tell you that the output is a sine wave with amplitude of 10000 V. This is of course completely unrealistic, but that's the way AC simulation works. Transient simulation is much more realistic, since it does not linearize the circuit. However, it is not the most convenient way to measure transfer functions. Indeed, the entire concept of a transfer function assumes that your circuit behaves linearly (if you put a sine wave in, you get a sine wave out) and only the amplitude and phase have changed.

To measure transfer functions, we need to plot $V_{out}(s)/V_{in}(s)$. If we make V_{in} have an amplitude of 1 V and zero phase, the transfer function or gain becomes $V_{out}(s)/V_{in}(s) = V_{out}(s)$, which makes the post processing of the data a bit easier.

Plot the magnitude (in dB) and phase (in °) of the transfer function of the OPAMP over the frequency range 1 Hz to 1 GHz. Plot at least 80 points per decade of

frequency for a good resolution. Turn in this plot. What is the low-frequency (DC) gain of the OPAMP? Does this value agree with the open-loop gain measured previously?

To measure the phase margin, first find the unity gain frequency (or the gain bandwidth) of the amplifier (the frequency at which the gain drops to 1, or 0 dB). Now find the phase at this frequency. The phase margin equals 180° plus the phase at the unity gain frequency. For example, if the gain drops to 0 dB at 40 MHz, and the phase at 40 MHz is −130°, then the phase margin equals +50°. Graphically, the phase margin is the distance between the phase and the -180° line, where phases above this line are reported as positive numbers.

Note: Don't be fooled, if the phase plot suddenly jumps from -180° to +180°. Most simulations restrict phase angles within this range, since -181° is mathematically equivalent to +179°. However, for measuring the phase margin, you should unwrap the phase for your calculations. In other words, if the phase has just jumped from -180° to +180°, begin subtracting 360° from the phase angle to preserve the continuity of the phase lag vs. frequency. Real circuits exhibit smooth, continuous phase changes with frequency. The sudden 360° jumps can be considered as numerical artefacts.

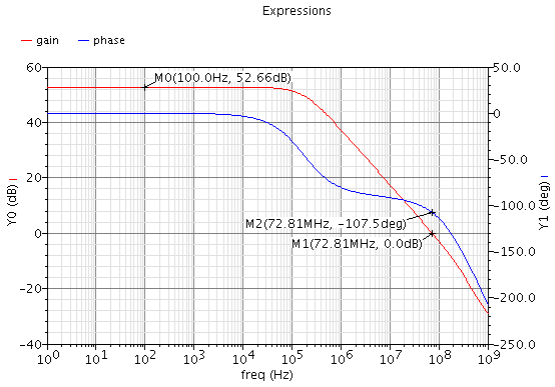


Figure 10: Exemplary waveform: Transfer function (DC gain, gain bandwidth, phase margin)

Calculator Setup:

- DC Gain: Use ymax and dB20 functions.
- GBW: Use cross and dB20 functions.
- PM: Use PhaseMargin function.

→ Include the plots and the measured values for the parameters in your report.

2.2.3. CMRR Measurement

The Common-mode gain measures how much the output changes in response to a change in the common-mode input level. Ideally, the common-mode gain of an OPAMP is zero (−∞ dB), meaning the amplifier should ignore the common-mode level and amplify only the differential-mode signal. Let's measure the common-

mode gain of our OPAMP. In order to measure the common-mode gain in the open-loop condition, we have to once again balance our high-gain OPAMP very carefully to keep the DC of V_{out} around 0.9 V (relative to *gnd*), just like we did in the transfer function simulation. Remember, we do this by adding a DC voltage source in series with one of the inputs, in this example the positive one. This voltage source is set to the input offset voltage so that if no other signal is present, the output voltage will be approximately zero (relative to *vcm*). Now, with this adjustment in place, we tie the two inputs together and apply an AC signal source *vsin* as shown below.

AC analysis:
vdc: The measured input offset voltage!
vsin: AC magnitude = 1 V

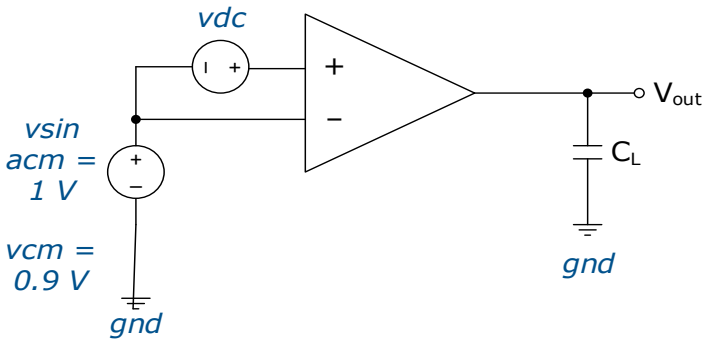


Figure 11: Setup for CMRR Measurement (Use schematic in Fig. 4)

Plot the common-mode gain (in dB) of the OPAMP over the frequency range 1 Hz to 1 GHz. Plot at least 80 points per decade of frequency for good resolution. Turn in this plot.

An important figure of merit in OPAMP design is the common-mode rejection ratio (CMRR). The CMRR is defined as the differential-mode gain (already specified in the transfer function simulation) divided by the common-mode gain. Remember, if you express your gains in the logarithmic units of dB, subtraction is equivalent to division. For example, if a particular amplifier has a differential gain of 80 dB at 100 Hz and a common-mode gain of 10 dB at the same frequency, then the amplifiers CMRR at 100 Hz is 70 dB. Ideally, an amplifier should have infinite CMRR. Practically, most designers try to get CMRR > 60 dB, though some applications may require much higher values. Please measure the CMRR and include it in the written report.

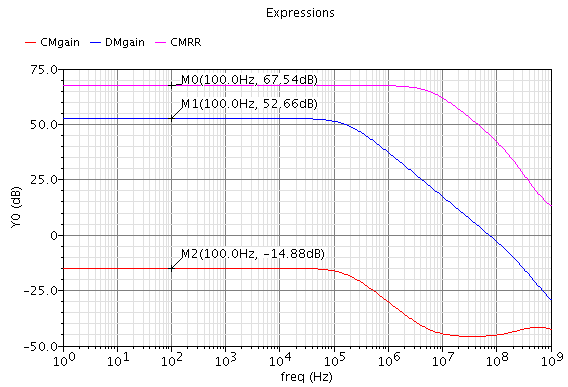


Figure 12: Exemplary waveform: CMRR

Calculator Setup:

- Diff Gain: Use value and dB20 functions.
- CM Gain: Use value and dB20 functions.

→ Include the plots and the measured value of CMRR in your report.

2.3 Unity-Gain Buffer: ICMR and Output Voltage Swing Measurements

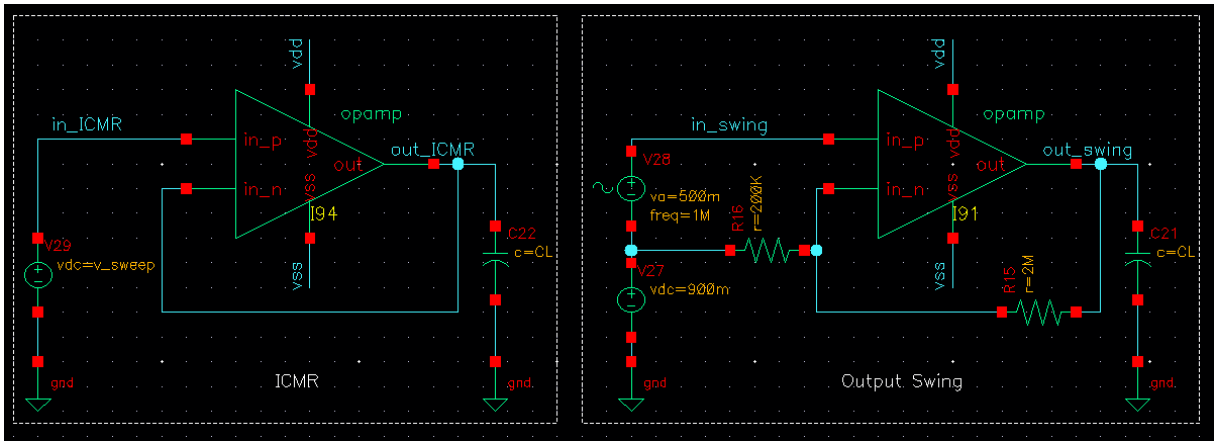
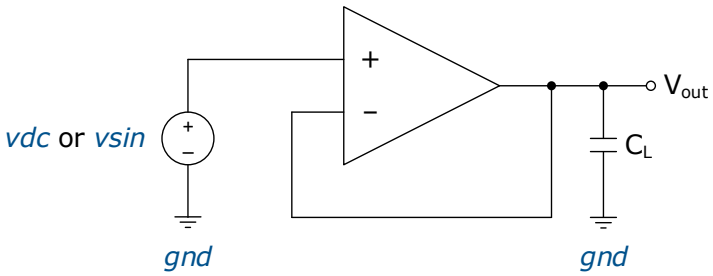


Figure 13: Testbench for all measurements in this section

Let's verify that the OPAMP can function as a basic unity-gain buffer. Connect the negative input to the output and apply a sine wave (0.5 V amplitude, 1 MHz frequency, centred at *vcm*) to the positive input. Run a transient simulation that captures at least 2-3 complete cycles of the sine wave and plot the output and input waveforms, i.e., V_{out} vs. V_{in}. The output should follow the input closely like shown in figure 15. Add this plot to the written report.

Transient analysis:
vsin: Amplitude = 0.5 V, DC voltage = 0.9 V , Frequency = 1 MHz

DC analysis:
vdc: Voltage sweep from 0 V to +1.8 V



Although you might have designed your OPAMP/DAC for load capacitances > 2 pF, please use that minimum C_L in all the simulations you are doing for the written report!

You can then additionally provide some information and/or exemplary waveforms for the maximal load that is supported by your design.

Figure 14: Setup for ICMR Measurement

Now let's measure the OPAMP's input common-mode range. Ideally, an OPAMP should work the same regardless of the DC levels of the input voltages (only the difference in voltages between the two inputs should affect the output). Of course, real circuits never behave this well. With the OPAMP still configured as a unity-gain buffer, run a DC analysis, in which the input voltage is swept from 0V to +1.8 V, with step size sufficiently small (for ex. 25 mV). Plot again V_{out} vs. V_{in} and determine the input common-mode range (the range of input voltage, at which the circuit has a gain of approximately one. Include this plot in your report.

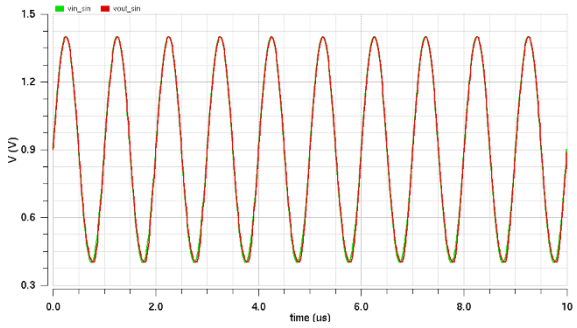


Figure 15: Example waveform: Voltage swing

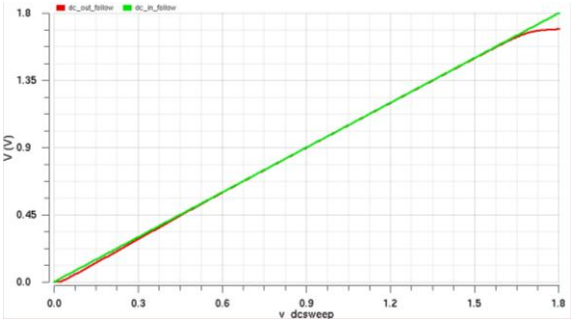


Figure 16: Example waveform: ICMR

Note: The OPAMP simulation setup needs two DC sweeps: The offset (range -0.05V to +0.05 V) and the ICMR/Output swing (range 0 to +1.8 V). However, the Explorer supports only a single DC sweep with a fixed range. To use two different sweeps, there are to methods: **A)** You can setup a new Explorer setup just for the ICMR/Output swing. **B)** You set up one variable and scale the other accordingly. E.g. you sweep your variable vdc from (-0.05 V to +0.05 V) and enter a scaled version 0.9/0.05*vdc+0.9 for the ICMR/Output swing. Be aware, that this x-axis still shows the non-scaled values when plotted!

→ Include the plots and the measured values for the parameters in your report.

2.4 Slew Rate and Settling Time Measurements

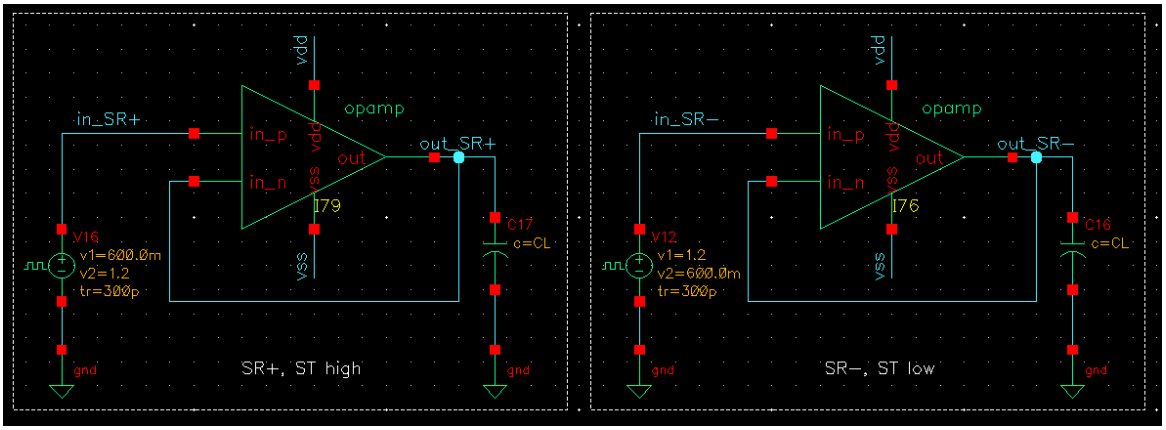


Figure 17: Testbench for all measurements in this section

In the previous assignment we used an AC analysis to determine the small-signal bandwidth of the OPAMP. The speed of amplifiers is however often limited by large-signal effects such as the slew rate, i.e., the maximum speed, at which an OPAMP can charge and discharge its load. To measure the slew rate, configure the OPAMP again as a unity-gain buffer, as shown below.

Positive SlewRate (Rising Edge)

vpulse: V_1 = 0.6 V , V_2 = 1.2 V , $t_{rise/fall}$ = 300 ps

Pulse Width = 0.497 us , Period = 1 us

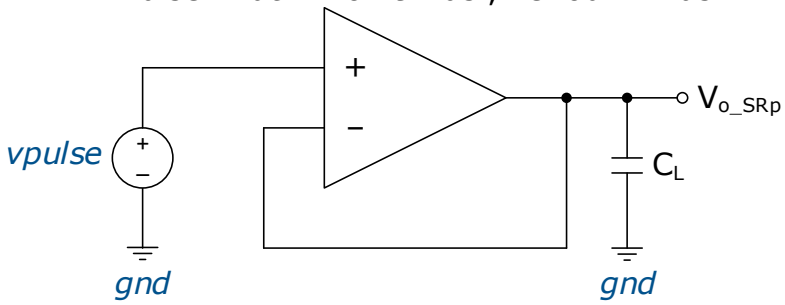


Figure 18: Setup for Slew Rate(+) Measurement

Run a transient simulation where the input signal is a square wave going from 600 mV to 1.2 V ("large-signal") with the remaining parameters specified as in the figure above. Look at the output waveform. Does it look like a nice square wave or do you see significant slewing (a slope less than infinity) on the 600 mV to 1.2 V transitions? Make sure that the slewing is not too strong. The output should still reach 600 mV and 1.2 V during each cycle. If it does not, your square wave is too fast (and the OPAMP too slow). Make sure your maximum time step is at least 200 times smaller than your simulation time to get a high resolution.

Select two points on the rising slope and from these calculate the positive slew rate in units of V/µs. Now select two points on the falling slope and calculate the respective negative slew rate in units of V/µs.

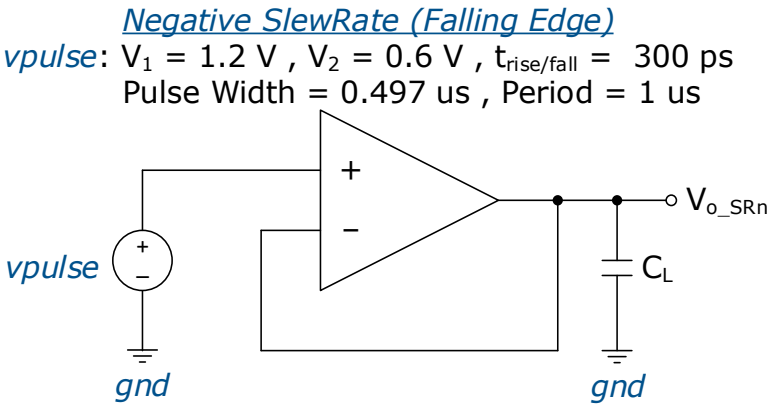


Figure 19: Setup for Slew Rate(-) Measurement

Hint: Use the slewRate function from the Calculator to save the expression for Slew Rate in the output setup in ADE. To measure the positive and negative slew rates, you could create two test setups in the same testbench and setup one input as square wave going from 600 mV to 1.2 V and the other as going from 1.2 V to 600 mV (Refer figures above).

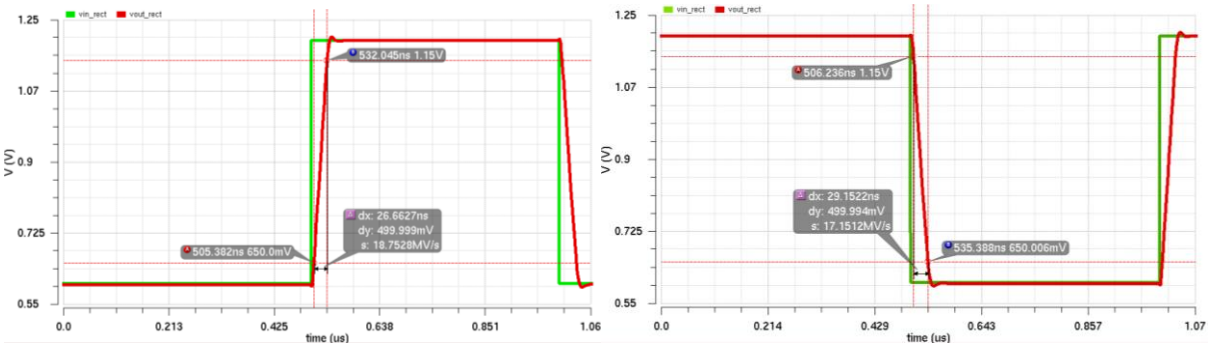


Figure 20: Exemplary waveform: Rising and Falling Slew Rate

Calculator Setup:

- Slew Rate: Use slewRate function.
- SettlingTime: Use settlingTime function.

When setting up the functions, you can click on the "Help" button in the calculator. It provides documentation of the function. Furthermore, we have answers to common issues in the troubleshooting guide.

→ Include the plots and the measured values for the parameters in your report.

2.5 DC Power Measurement

The DC Power measurement is indicative of how much DC current and DC power the OPAMP consumes. Setup a dc simulation for the OPAMP schematic and select 'Save DC Operating Point'. After the simulation runs, use the calculator to measure the total dc current that flows into the OPAMP (the two stages and the bias network). This will give you the overall current consumption of the OPAMP. The same can also be used to calculate the total dc power consumption.

→ Include the measured value for the parameter in your report.

2.6 Noise Measurement

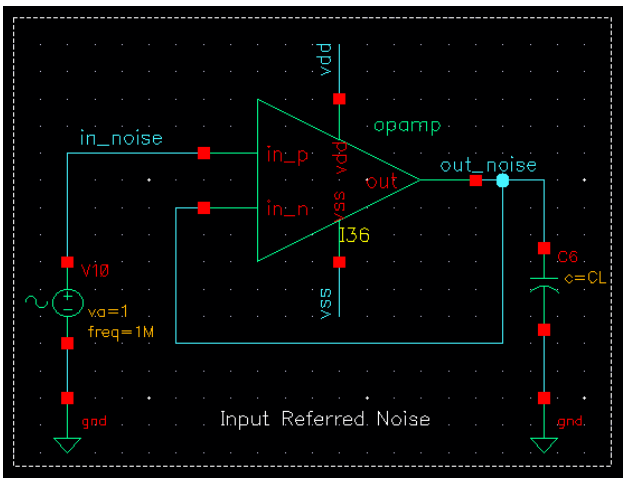


Figure 21: Testbench for measurement in this section

The noise contributions in the OPAMP could be mainly attributed to flicker noise, and thermal noise. Students are advised to go through the reference books to accustom themselves with noise theory of basic components of the OPAMP, namely the MOSFETs, resistors and capacitors.

To measure the input referred noise, configure the OPAMP again as a unity-gain buffer as shown below and run a noise simulation while sweeping the variable 'frequency' from 1 to 100 MHz. Use a logarithmic sweep with 50 points per decade. Furthermore, you need to specify the input and output of the noise simulation. Set the 'Output Noise' to mode 'voltage' and select the output net of the OPAMP as 'Positive Output Node'. The 'negative output Node' can be left empty, gnd will be used as default internally. Since noise shall be calculated input referred, set 'Input Noise' to 'voltage' and select the voltage source driving the non-inverting input.

Input Referred Noise

vsin: Amplitude = 1 V, DC voltage = 0.9 V ,
Frequency = 1 MHz

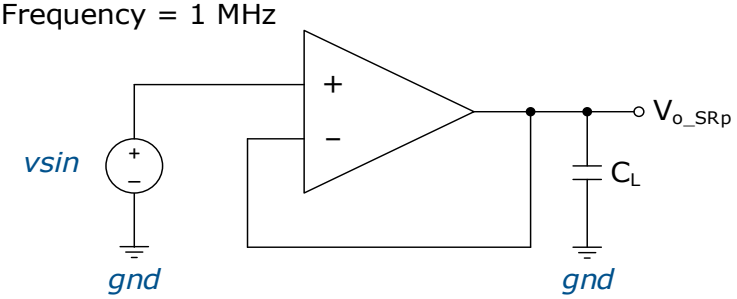


Figure 22: Setup for Input Referred Noise Measurement (Use schematic in Fig. 18)

Hint: After running the noise simulation use Results->Direct Plot->Mainform from the ADE Explorer window to view the simulation results. Since we specified the noise at 20kHz, you can use the value() function to get the noise at a specific frequency.

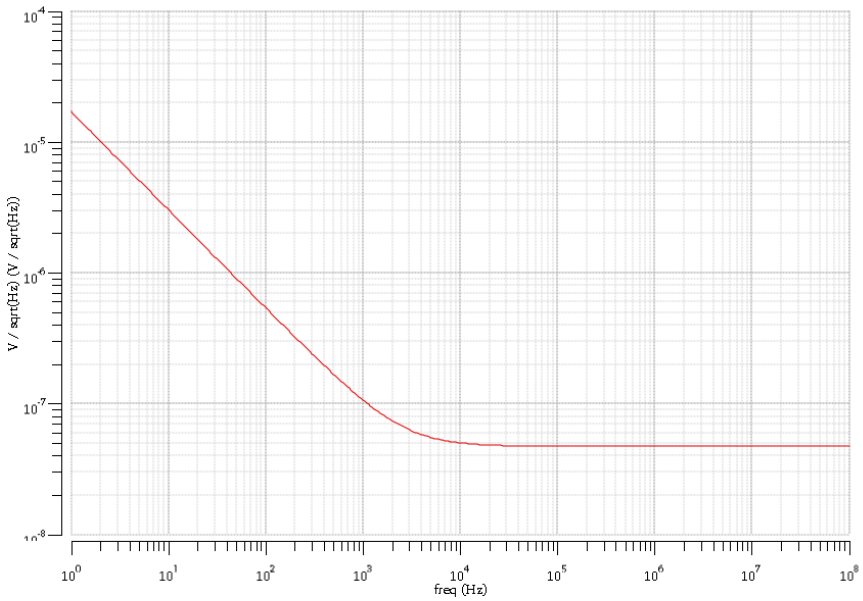


Figure 23: Example waveform: Input Referred Noise

Be aware: The y-axis is plotted logarithmic. Right click on the y-axis to change between linear and logarithmic.

→ Include the plots and the measured values for the parameters in your report.

2.7 Test Bench for All Simulations

Please combine all the required measurements and analysis (DC, AC, trans, etc) into one single testbench. This will help you to simultaneously simulate multiple OPAMP parameters and would in effect allow you to understand what impact increasing or decreasing one parameter has on all the other parameters. Do the following for this:

1. Create multiple instances of the OPAMP for the various simulation setups mentioned above. Label the input and output voltages accordingly using the option Create -> Wire Name in virtuoso schematic editor window.
2. Setup multiple analyses in the setup state for the testbench (Analysis -> Choose -> DC/AC/Trans etc).
3. Activate the analyses under consideration and run the simulation. You could choose to activate or deactivate individual analysis as per your convenience and the measurement being carried out.

Sample Testbench schematic:

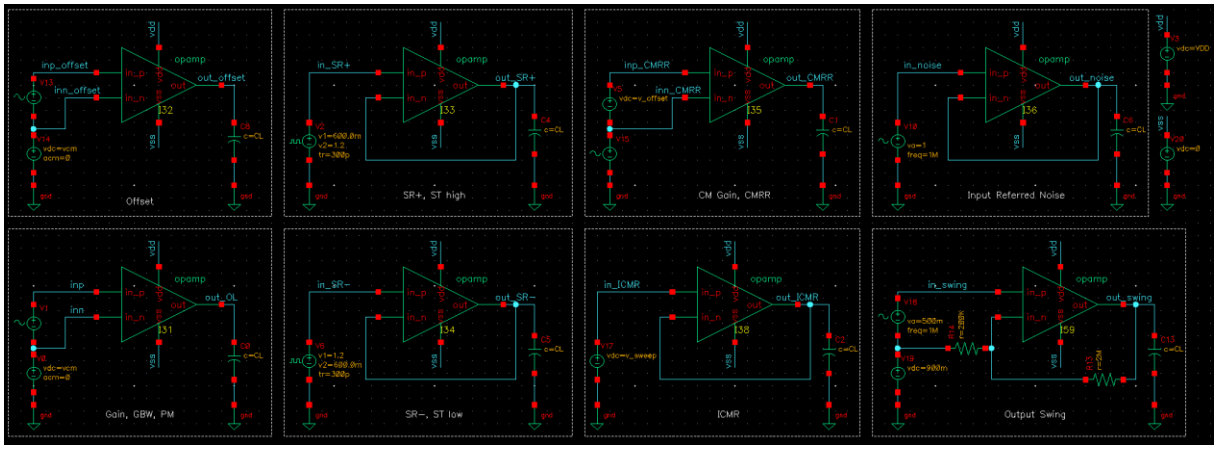


Figure 24: Testbench for all measurement schematics combined

Sample Testbench ADE state:

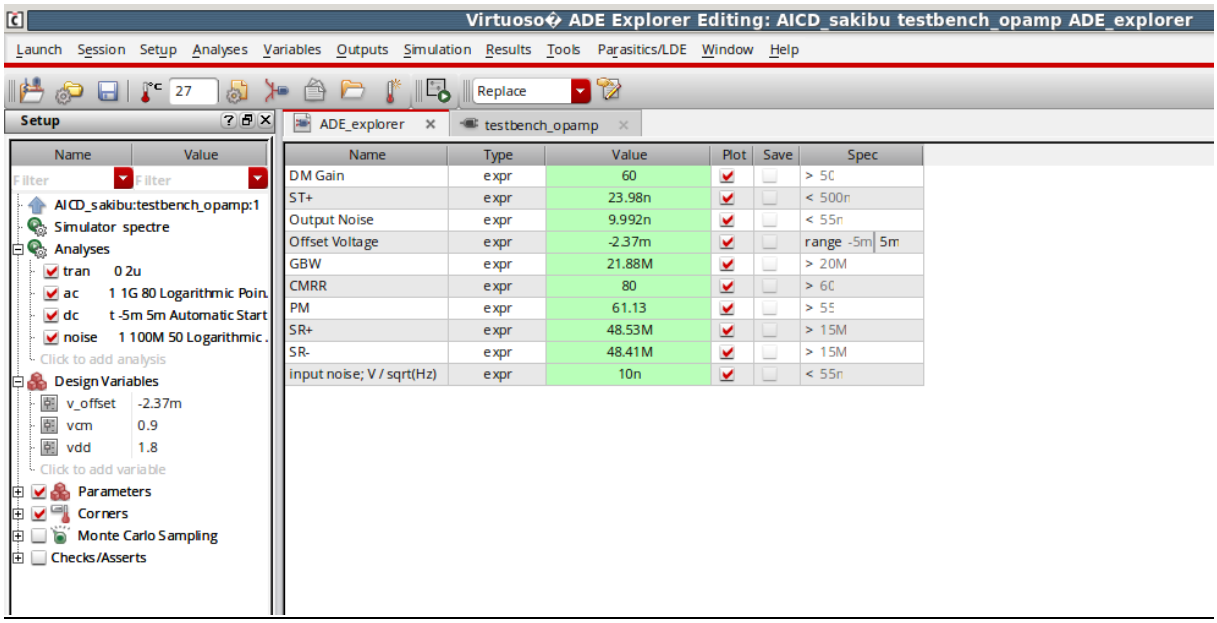


Figure 25: Testbench for some of the ADE states combined(using verilogA Opamp)

3. Testbench Verification

To check your Testbench a VerilogA based OPAMP is provided. You can find the VerilogA OPAMP in the Demo_opamp_verilogA library. The VerilogA OPAMP can be very helpful to differentiate whether your Testbench or your OPAMP design is faulty. To check your Testbench just replace your OPAMP with the VerilogA OPAMP, the connections should be the same. If your Testbench is correct, the parameters in Table 2 should be approximately the result from your Testbench. Small deviations might occur.

Verilog OPAMP Parameters	
Offset	-2.59 mV
DC Gain	60 dB
GBW	21.9 MHz
PM	61.1 °
CMRR	80 dB
SR+	47.9 V/us
SR-	47.7 V/us
ST+	26.8 ns
ST-	26.6 ns
power	250 µW
noise	10 nV/$\sqrt{(Hz)}$

Table 2: Performance of the VerilogA OPAMP

Please Note: Even with a correctly setup testbench you might obtain slightly small variations. Different settings like simulation accuracy, step size as well as slight difference of expression definition will lead to variances. Differences in the third significant figure are expected. Some parameters tend to be more sensitive to variations than others.