Advanced Integrated Circuit Design Lab

Analog Layout Introduction

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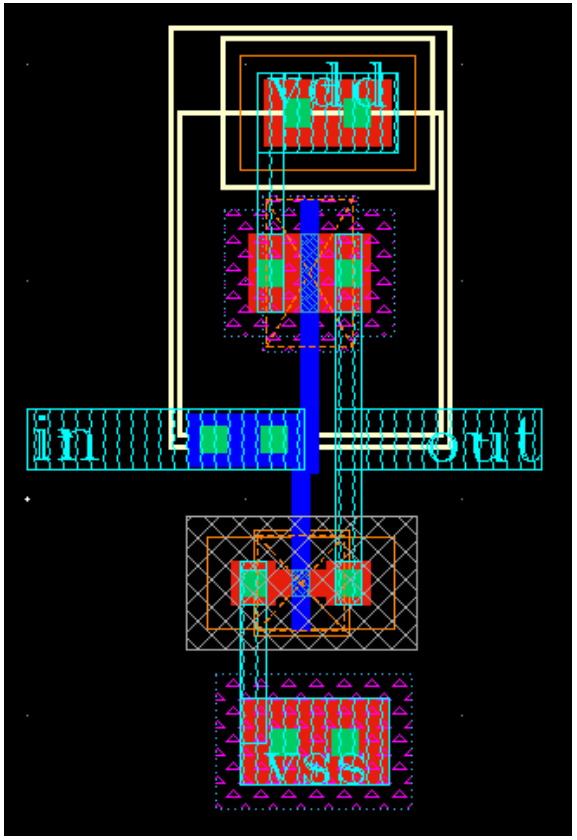
General Information on Layout

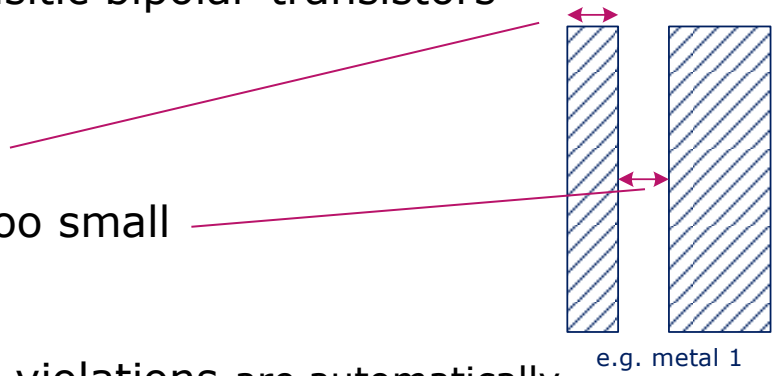
- Definition: "Layout is the representation of an integrated circuit in terms of planar geometric shapes, which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit." (source: Wikipedia)
- As a layout designer, the integrated circuit is viewed from the top (see on the right).
  - Different layers (well, active, poly, metal, via, …) are indicated by different colors.
  - The background (black color) marks the layer of the global substrate.
  - The thicknesses of the layers are fixed by the semiconductor foundry.



CMOS inverter layout
in *umc65ll* technology

Design Rules & Physical Verification

- The layout has to be designed according to specific design rules, which are fixed by the foundry for each technology.
- The purpose of design rules is as follows:
  - Warranty of dimensional precision in micro fabrication
  - Warranty of precision on electrical characteristics
  - Prevention of latch-up triggered by parasitic bipolar-transistors
- Exemplary design rule violations:
  - Width of a metal interconnect too small
  - Distance between metal interconnects too small
- Physical Verification steps:
  - Design Rule Check (DRC) → Design rule violations are automatically detected and reported
  - Layout Versus Schematic (LVS) → Equivalence of layout and schematic



Layout Steps

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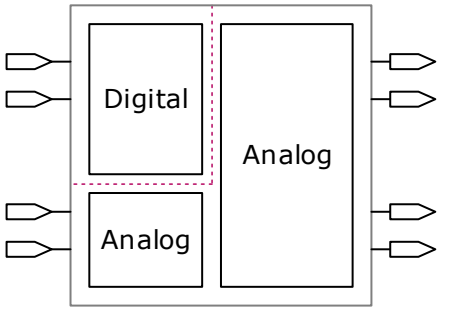
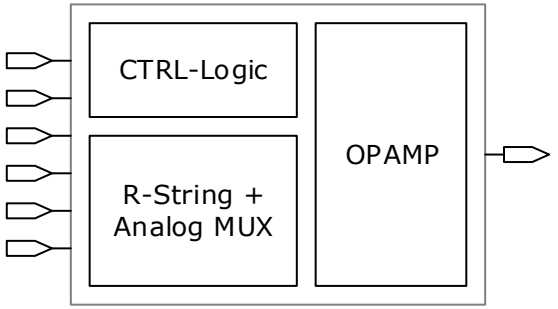
Floorplanning:

- Division of the entire die area among major functional sub-blocks to facilitate interconnection and effectively utilize the available area.
  - Digital blocks* (e.g. CTRL-Logic)
  - Analog blocks (e.g. OPAMP, R-String, MUX)
- Some of the aspects to be considered:
  - Power supply nets/grid
  - I/O signal pins
  - Sizes of transistors and passives
  - Shielding/guarding*



Exemplary floorplan for a PGA (yours can look different!)



*Shielding or guarding is a common practice in analog layout. The clock signal of any digital blocks could for example add unwanted noise to analog blocks, which might require shielding or guarding techniques! More information can be found in "The Art of Analog Layout", by Hastings.

Layout Steps

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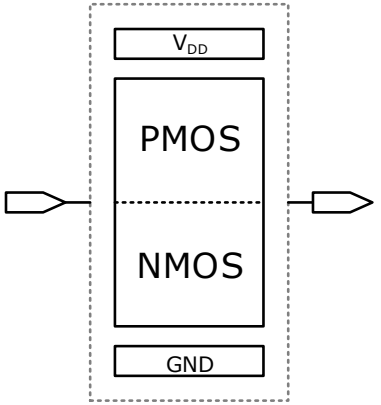
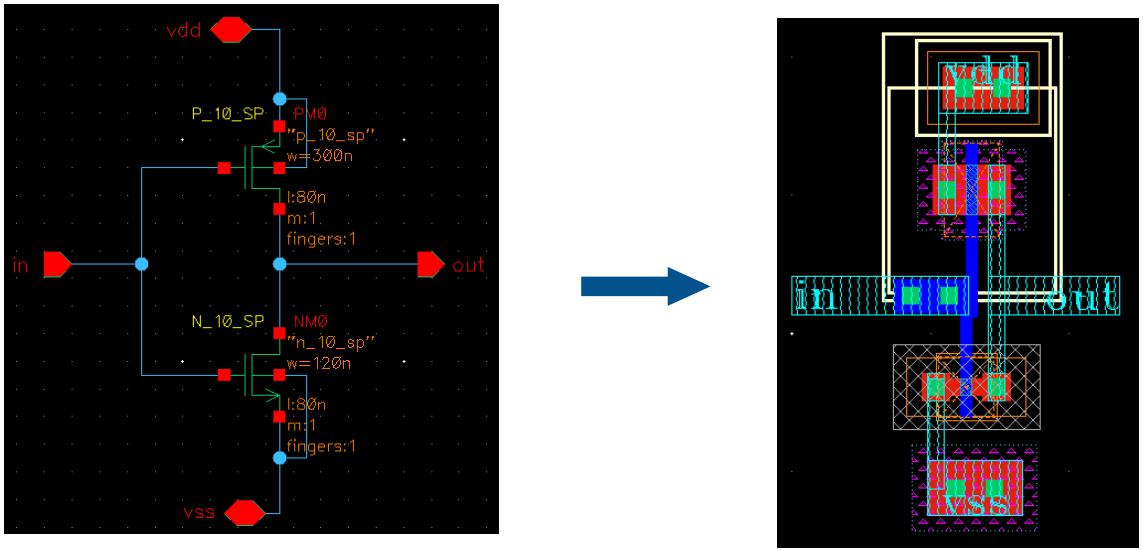
Placement:

- Placing the instances/sub-blocks in the layout
- Layout design can be "schematic-driven"
  - Layout oriented towards or "following" the schematics
  - Example: Schematic-driven CMOS inverter layout





Attention: You are free to design the layout as you choose! This means your layout does not necessarily have to be "schematic-driven". Another style can be better suited for your design and might lead to a more compact and robust layout. It is your decision!

Layout Steps

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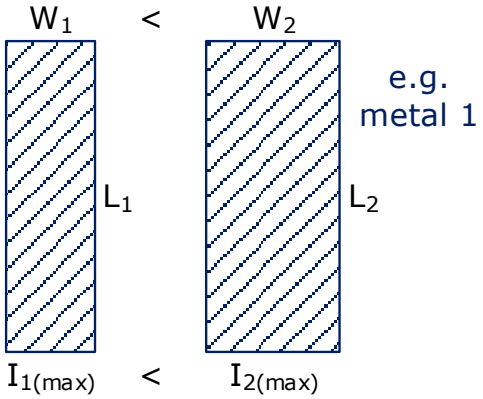
Routing:

- Connecting the instances/sub-blocks with different metal layers
- Routing introduces parasitics, which may deteriorate the performance
  - Parasitic resistances, capacitances or even inductances
  - E.g.: The parallel placement of interconnects raises a crosstalk of signals
- To minimize the effect of electromigration, the foundry specifies maximal currents for metal interconnects:
  - Simplified rule for the lab:
    - Metal: I_{max} = 1 mA/µm (W = 1 µm → 1 mA)
    - Vias: I_{max} = 0.2 mA/via (1 Via → 0.2 mA)
  - Example: For I = 300 µA use at least W = 300 nm and 2 Vias in parallel.
  - Rule of thumb: Add as many contacts/vias as the design allows to achieve reliability



Layout Techniques

Multisegment resistors:

- Can be used to create more compact layouts

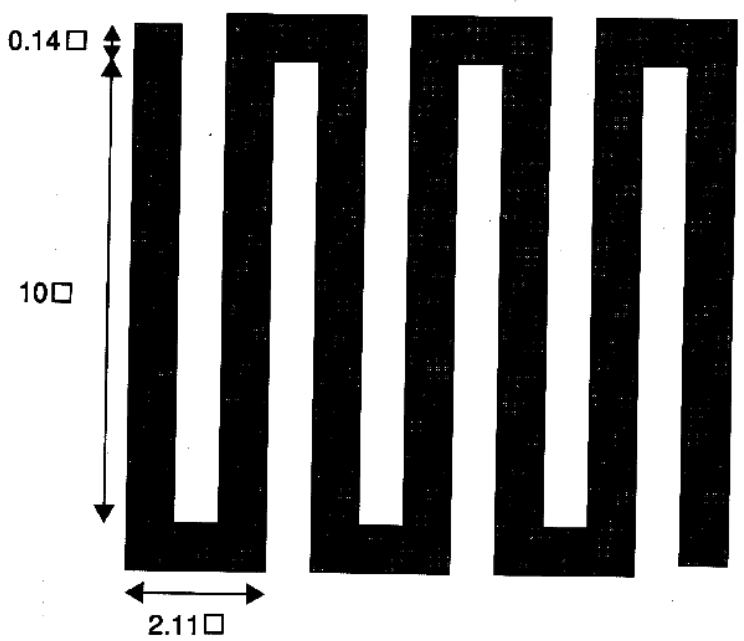
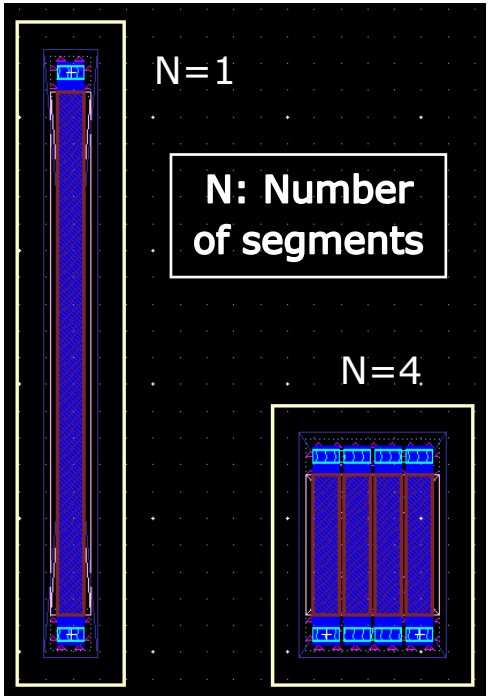


Fig. 2.23 A typical layout for an integrated resistor.



Layout Techniques

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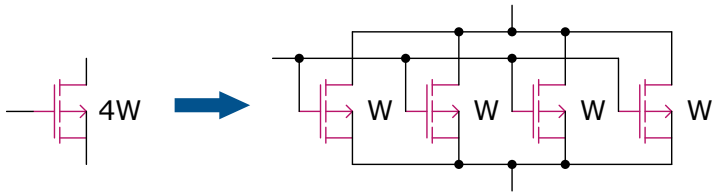
Multifinger MOSFETs:

- Can be used to create more compact layouts
- Reduce the series resistances



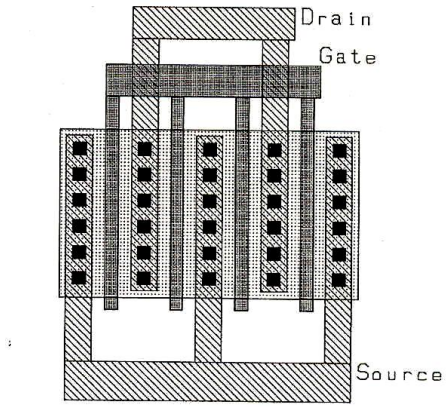
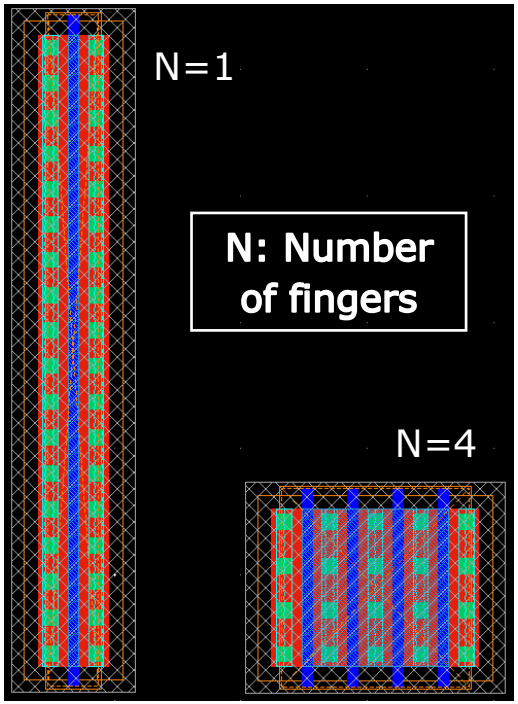


Figure 5.16 Layout of a large (width) MOSFET.



Layout Techniques

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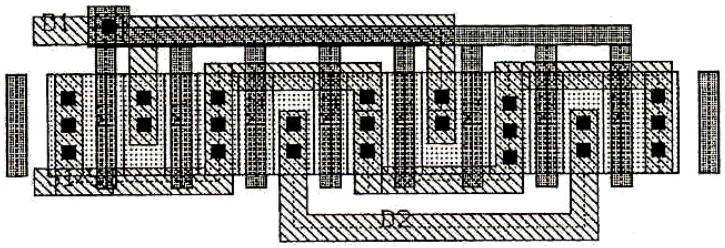
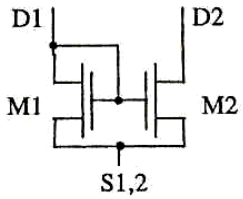
Interdigitated layout:

- Area savings
- Effects of process variation and mismatch can be reduced
- Applicable for current mirrors, resistive networks,…



(a)



(b)

Figure 20.18 (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

Note: The two MOSFET instances in the schematic are realized by one multifinger MOSFET in the layout and the respective wiring.

Layout Techniques

Common centroid layout:

- Effects of process variation and mismatch can be reduced
- Applicable for differential pairs, single transistors, passives,…

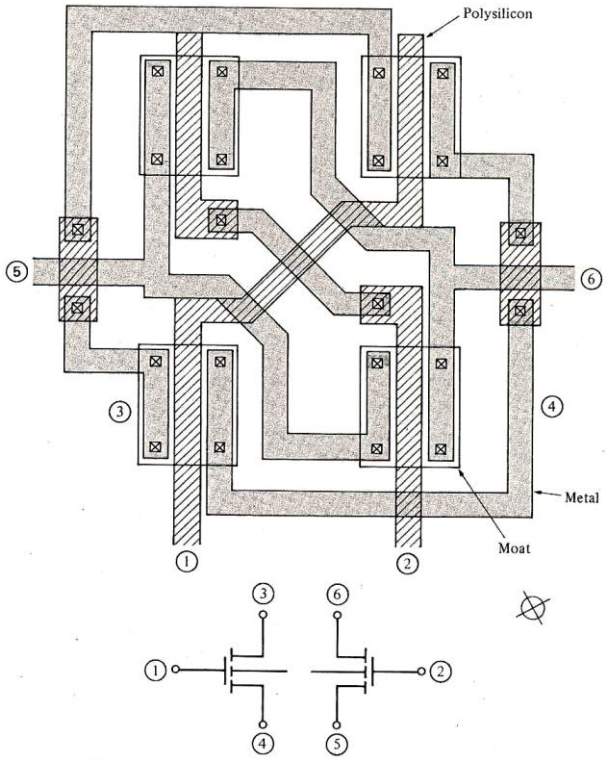
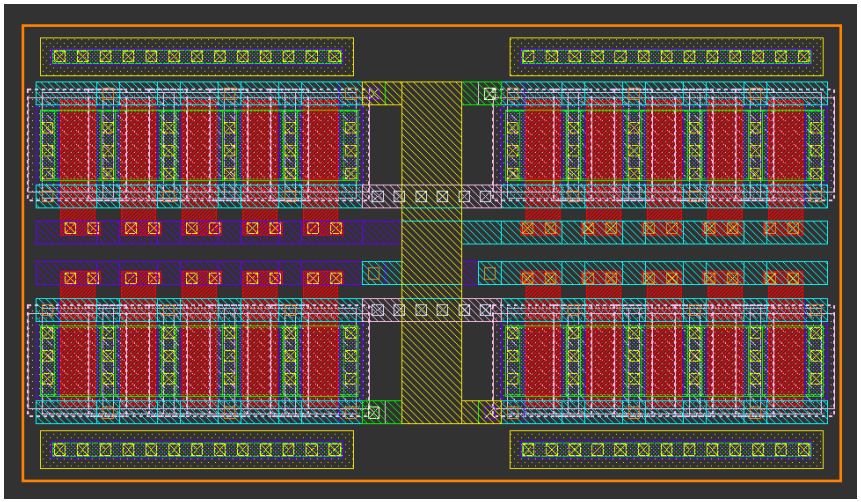
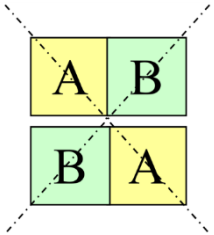


Figure 7.2-5 Layout of a cross-coupled transistor pair.

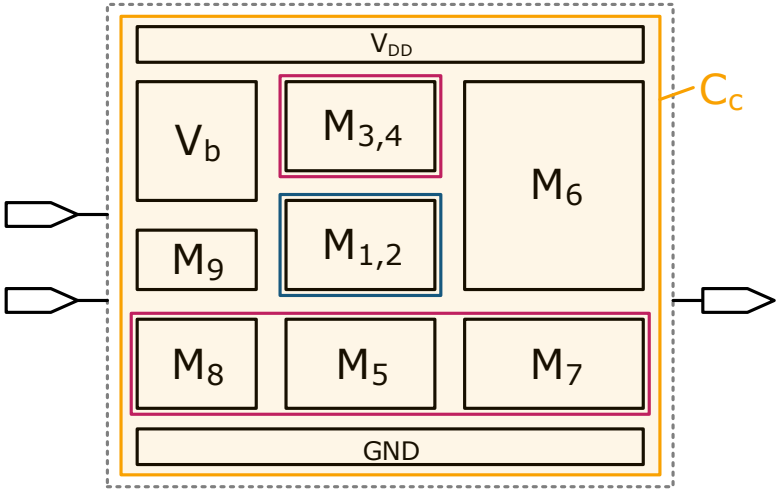




Note: The array should be symmetrical around both the x and y-axis.

Example: OPAMP Layout Techniques

- Interdigitated layout possible for the active load ($M_{3,4}$) and the biasing current mirror (M_8, M_5 and M_7)
- Common centroid layout possible for the differential pair ($M_{1,2}$)
  - Don’t split W to pieces smaller than 3 µm!
- The coupling capacitor (C_c) can be placed next to the OPAMP (in some technologies even on top of the whole circuit to save area)
  - On top not possible in *umc65ll*

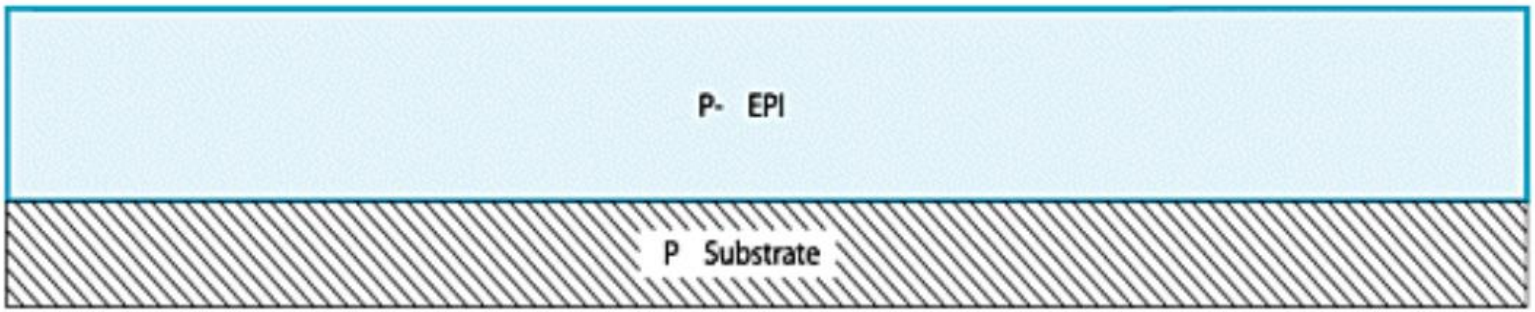


Again, it is up to you, if you want to implement specific techniques in the layout. The floorplan for your OPAMP layout can also differ from the example on the left!

Substrate and Wells

Base Material: p-doped substrate

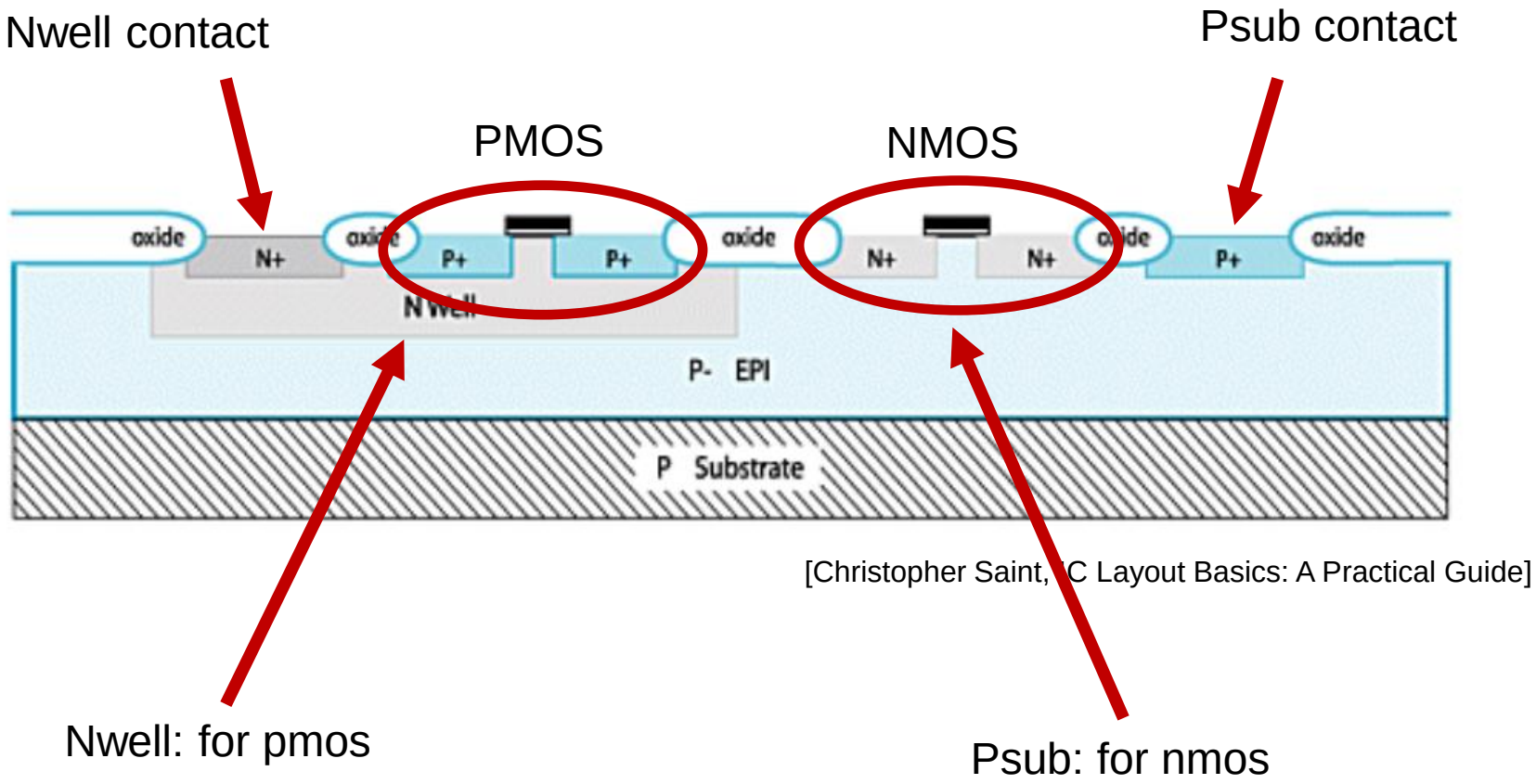
- Nmos: directly implemented on p substrate
- Pmos: require additional n-well



[Christopher Saint, IC Layout Basics: A Practical Guide]

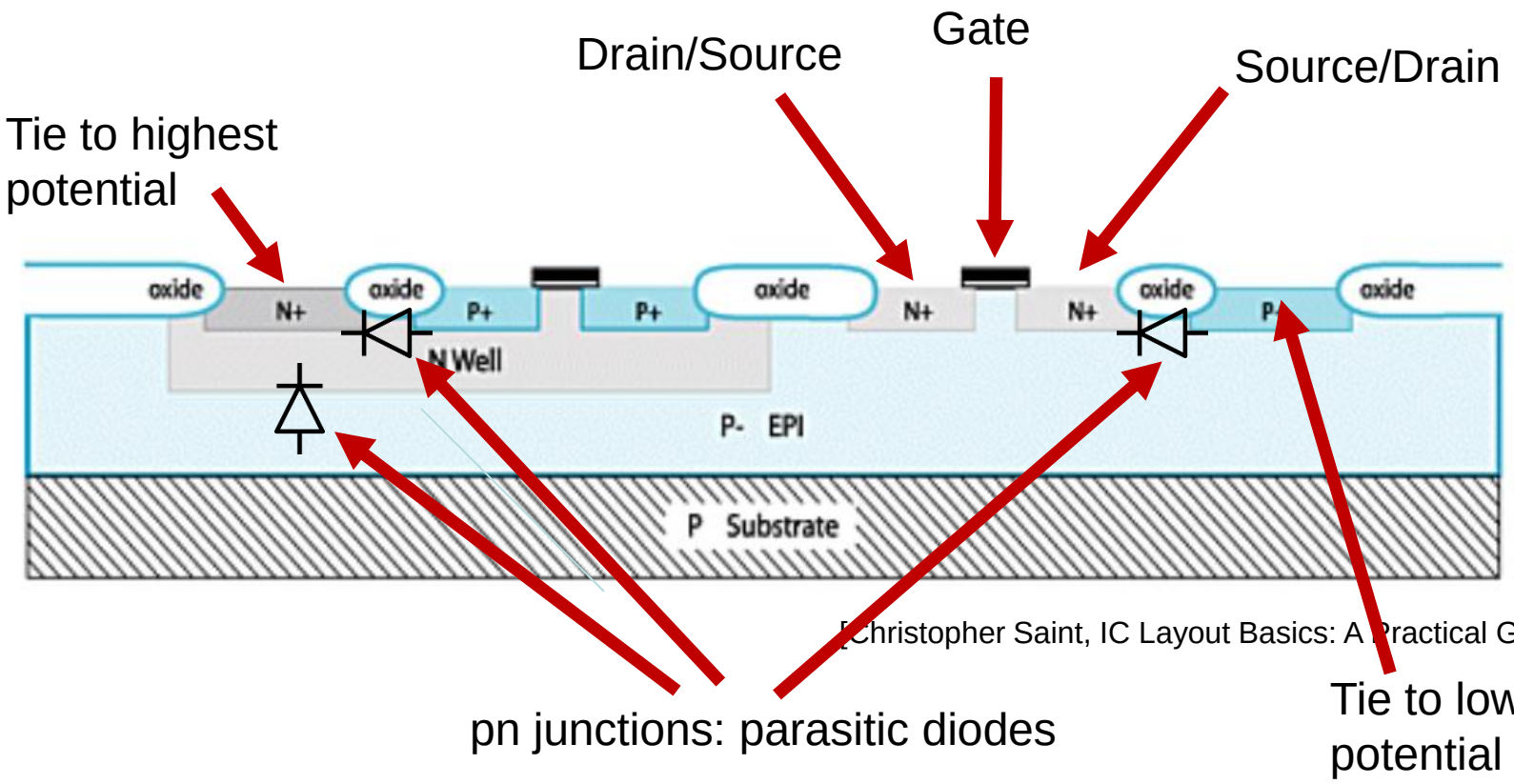
- the p-doped substrate is a poorly conductive
  - Provide enough substrate contacts for good conectivity
  - All substrate contacts **must** be the same electrical net

Substrate and Wells



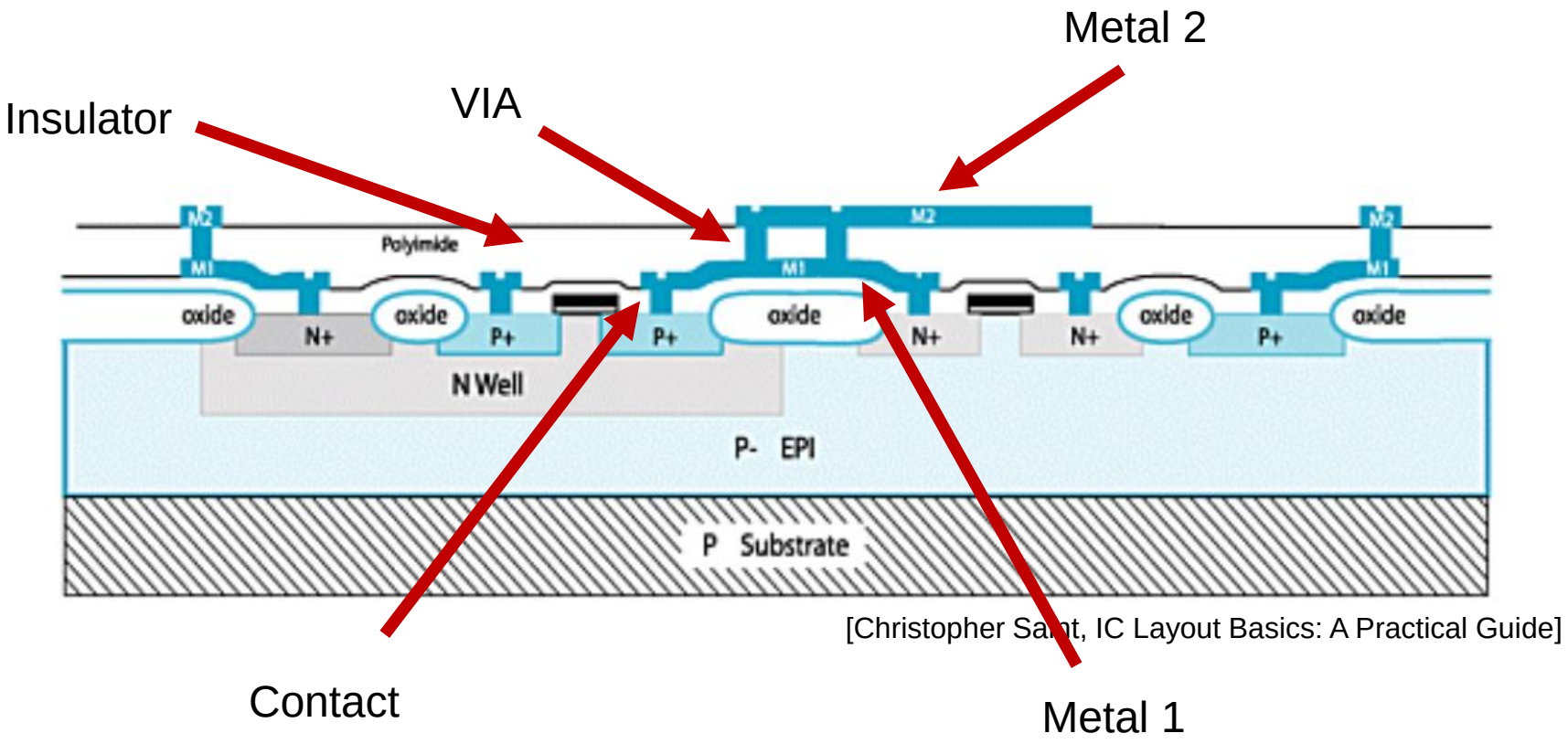
[Christopher Saint, IC Layout Basics: A Practical Guide]

Substrate and Wells



- pn junctions act as parasitic diode. Make sure to always reverse bias these!

Substrate and Wells



[Christopher Saint, IC Layout Basics: A Practical Guide]

- Establish the circuitry by connecting the semicondutor elements using contacts, VIA‘s and Metal

PCELLs in *umc65ll* Technology

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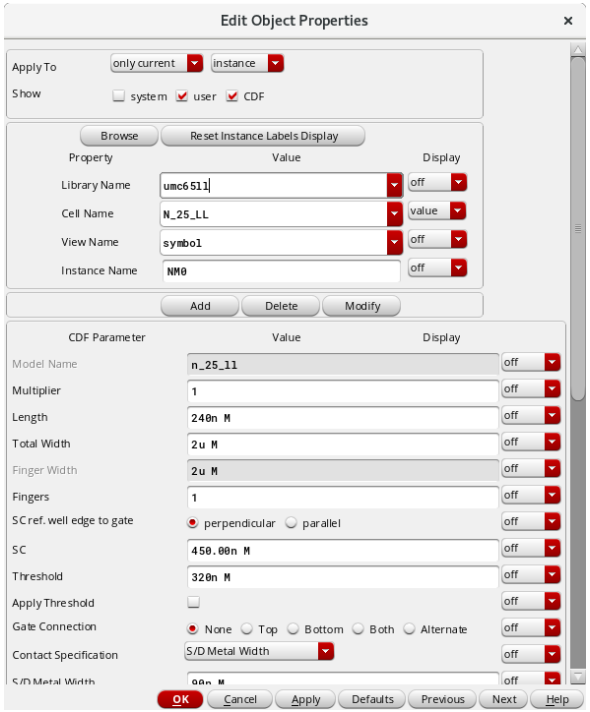
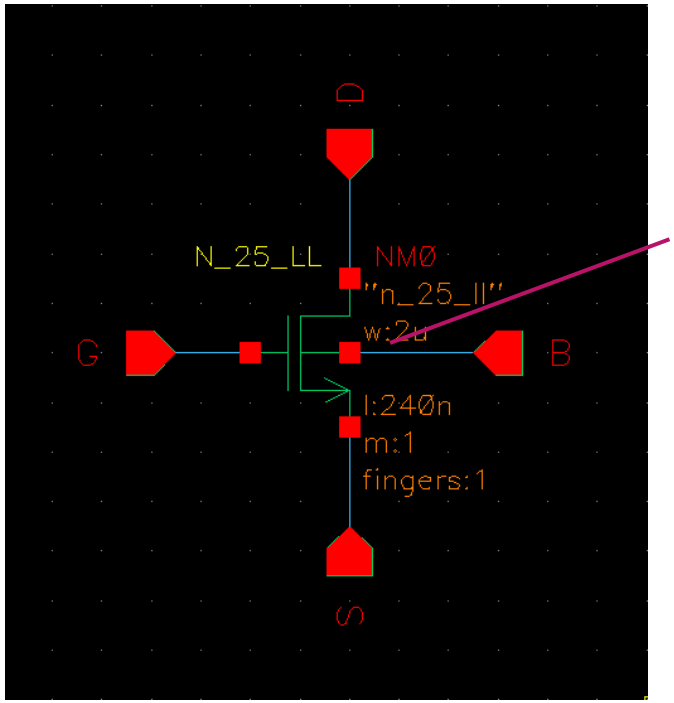
- UMC offers parameterized cells for all the components/devices present in their 65 nm foundry design kit.
- These PCELLs allow the user to create schematics and layouts at a higher level of abstraction.
- For the layout you do not have to worry about the internal structure of the transistors, resistors, etc., you simply have to place them.

PCELLs in *umc65ll* Technology

NMOS in schematic:

- Cell: *N_25_ll*
- View: *symbol*





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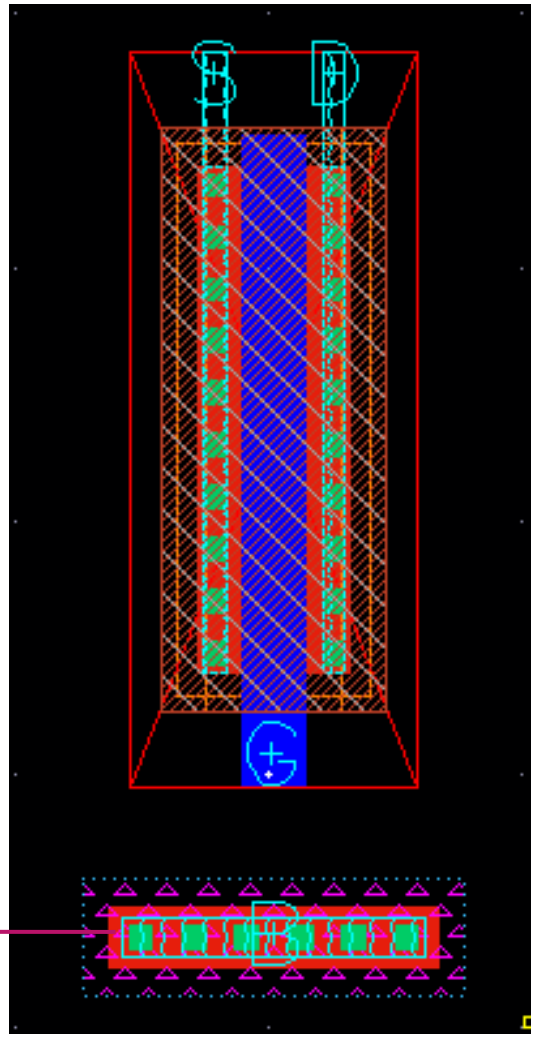
NMOS in layout:

- Cell: *N_25_LL*
- View: *layout*

Note: Depending on the length and width as well as the number of fingers, your transistor will appear differently.

Note: The device is symmetric. Source and Drain can be interchanged and are defined by your connections.



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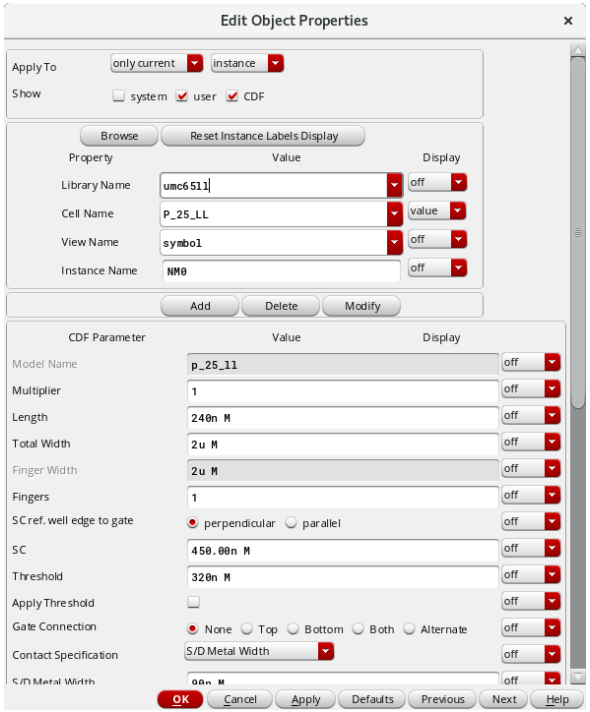
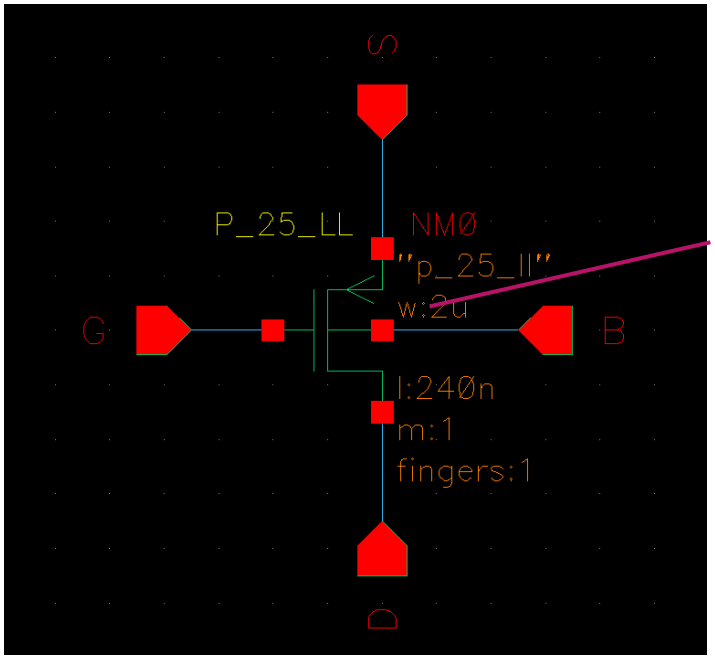
PMOS in schematic:

- Cell: *P_25_ll*
- View: *symbol*





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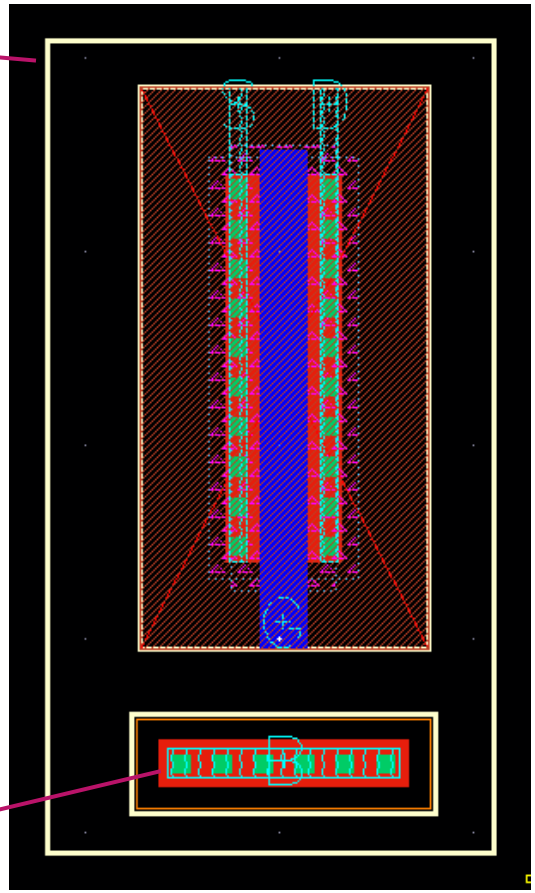
PMOS in layout:

- Cell: *P_25_LL*
- View: *layout*

nwell outline
(*Layer NWEL*)
Enclosed area is a nwell



nwell contact
(*M1_NWEL via*)

Note: Depending on the length and width as well as the number of fingers, your transistor will appear differently.

Note: The device is symmetric. Source and Drain can be interchanged and are defined by your connections.

Note: The enclosed area of the nwell outline will be an nwell. The nwell contact must be in the same well as the transistor itself. To save area, you can place multiple devices inside the same nwell.

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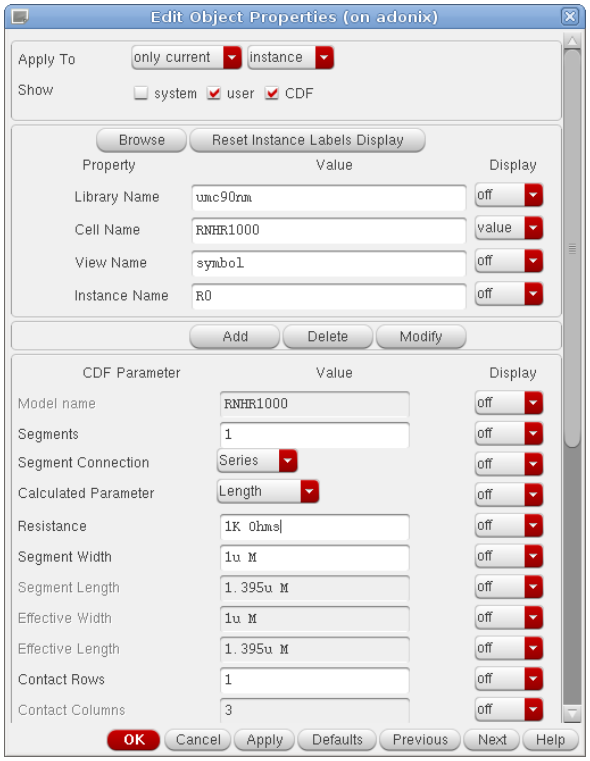
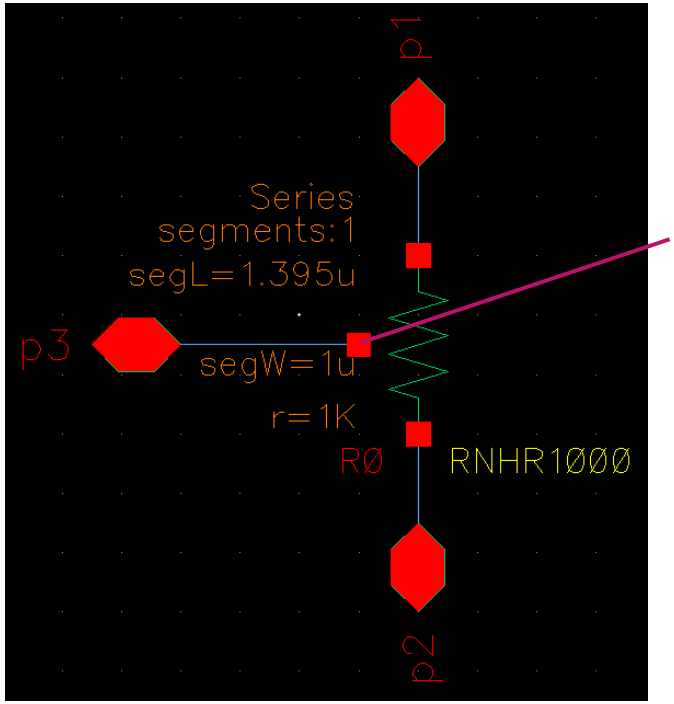
Resistor in schematic:

- Cell: *RNHR_LL* (high resistance poly resistor)
- View: *symbol*

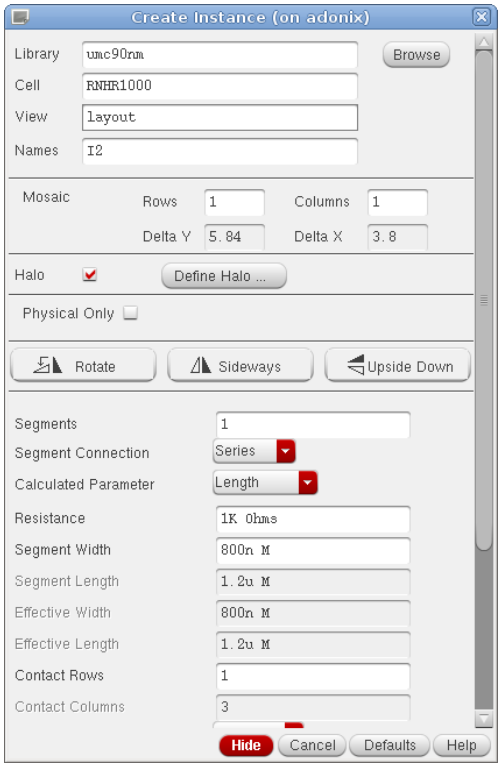




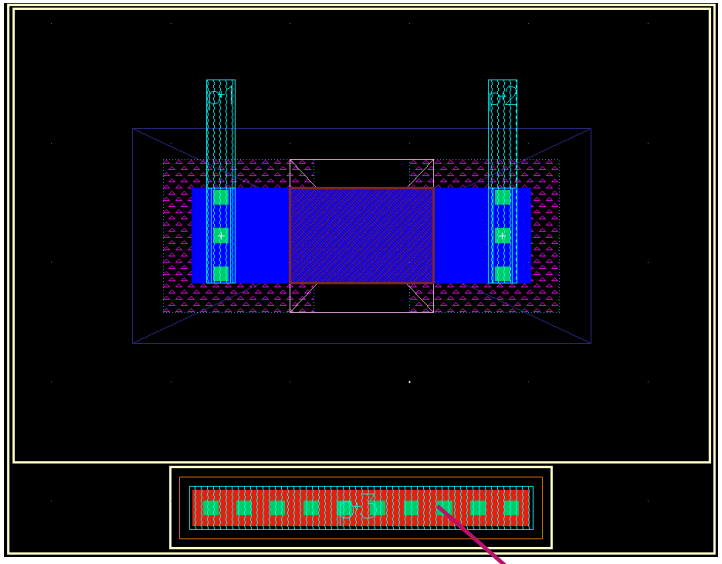
PCELLs in *umc65ll* Technology

Resistor in layout:

- Cell: *RNHR_LL* (high resistance poly resistor)
- View: *layout*



Note: Your layout of the resistor might look different than shown here. It varies with the chosen number of segments.



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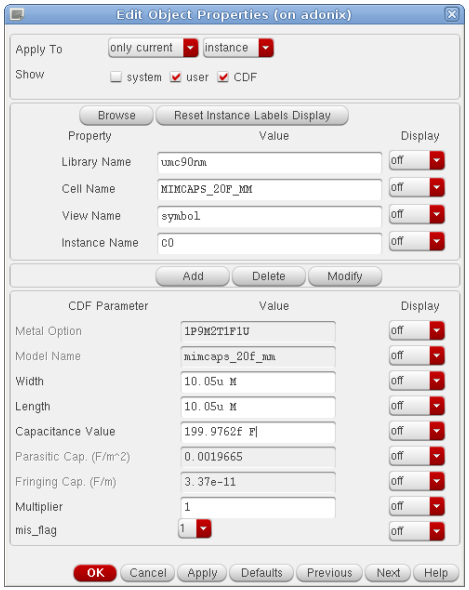
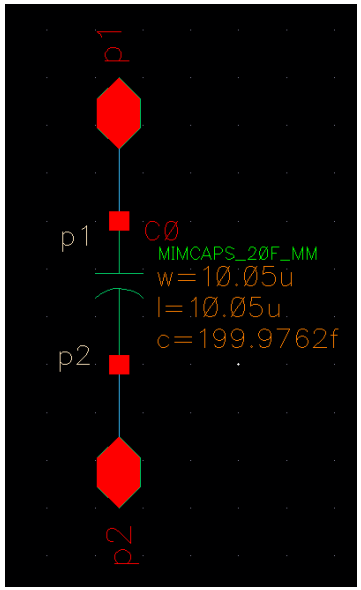
Capacitor in schematic:

- Option 1:
  - Cell: *MIMCAPS_20F_MM*

    (metal-insulator-metal capacitor).
  - View: *symbol*
- Option 2:
  - Cell: *MOMCAPS_AS_MMKF*

    (metal-insulator-metal capacitor).
  - View: *symbol*





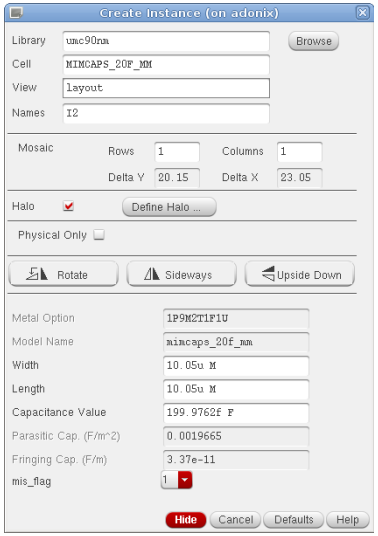
PCELLs in *umc65ll* Technology

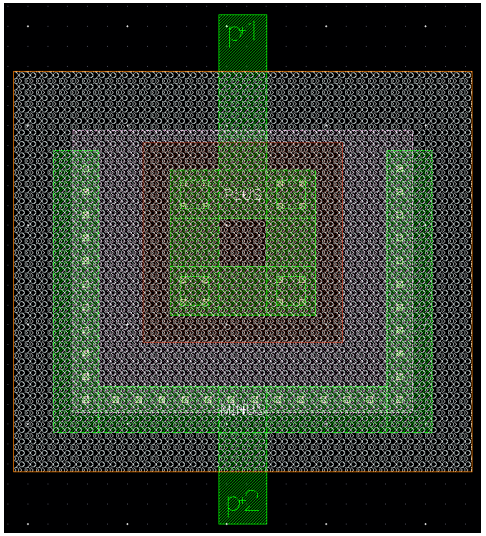
Capacitor in layout:

- Option 1:
  - Cell: *MIMCAPS_20F_MM*

    (metal-insulator-metal capacitor).
  - View: *layout*
- Option 2:
  - Cell: *MOMCAPS_AS_MMKF*

    (metal-oxide-metal capacitor).
  - View: *layout*





PCELLs in *umc65ll* Technology

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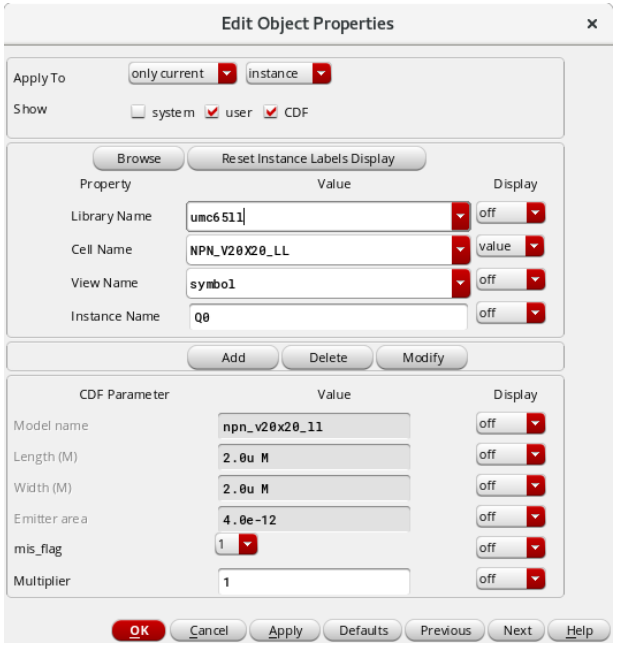
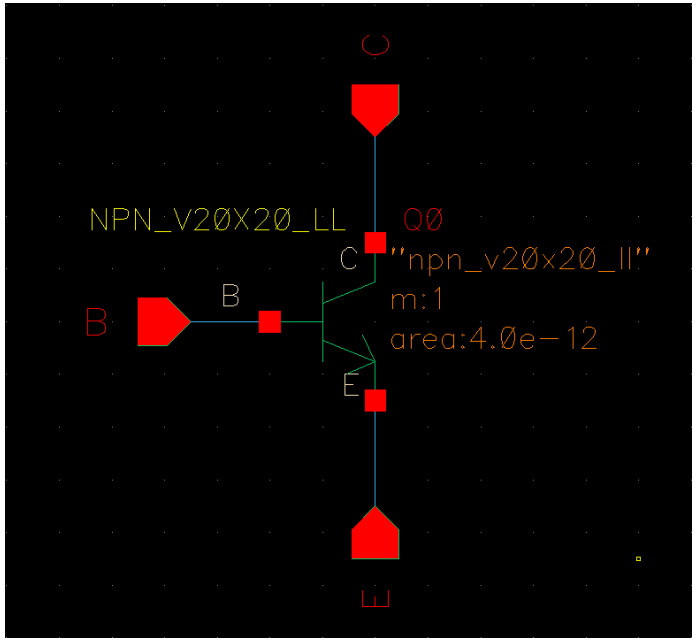
BJT in schematic: (BGR Task Only)

- Cell: *NPN_V20x20_LL* (as example)

  equivalent: *V32x32, V50x50, V100x100*
- View: *symbol*





PCELLs in *umc65ll* Technology

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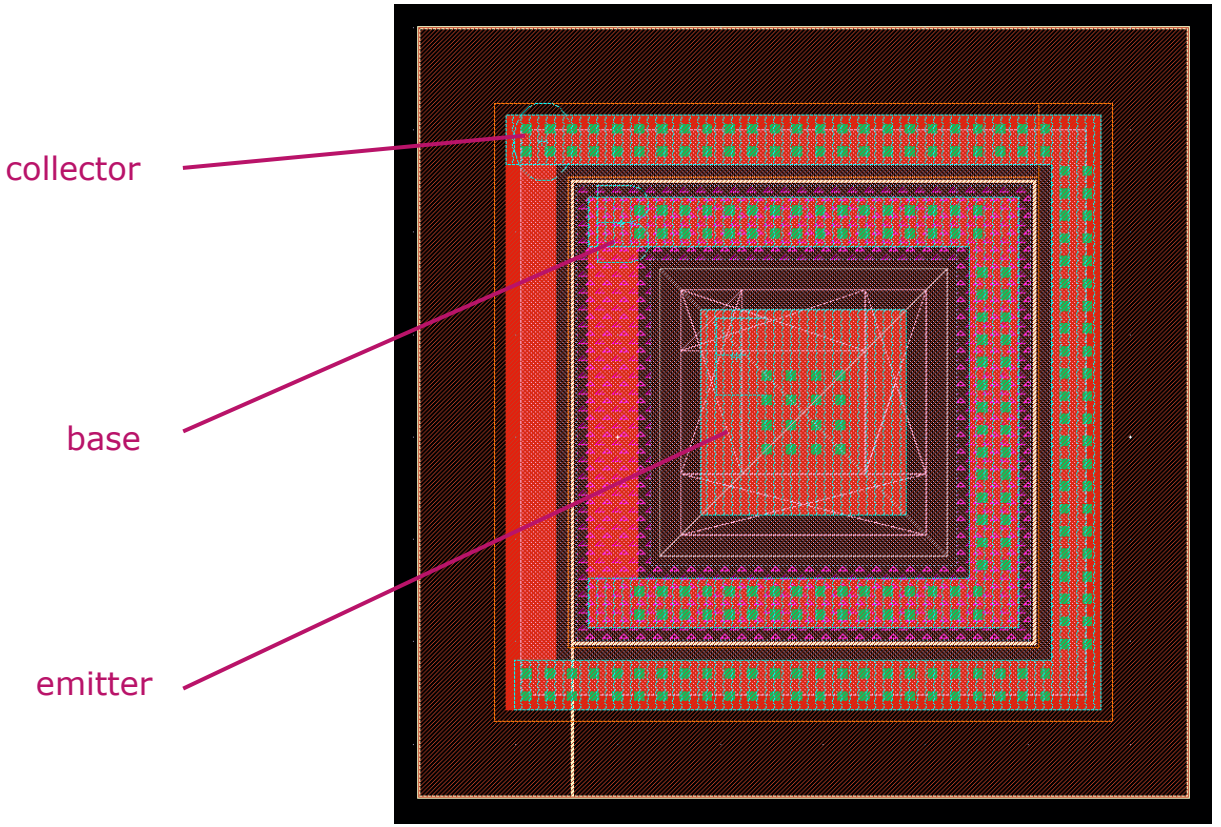
BJT in layout: (BGR Task Only)

- Cell: *NPN_V20x20_LL* (as example)
- View: *layout*



Additional Hints

- The *M1_NWEL* (local n-well) and *M1_PSUB* (global p-substrate) contacts/vias should always be placed close to the corresponding device(s).
- Remember: For this lab the *NWEL* contact should always be connected to the highest and the *PSUB* contact to the lowest potential of the circuit, i.e., *vdd* and *gnd*!
- You can place more than one of the resistors/p-transistors in a common n-well, but consider the hints above.

Summary

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- Matching
  - Between multiple instances of components, differential pairs, resistive dividers etc.
  - Between multiple instances of same circuit block
  - Common-centroid, multi-fingering, interdigitation, multi-segmenting
- Current Densities
  - Interconnects, Metal paths etc
- Dimensioning & Area
  - Keep area requirement in mind when dimensioning components
  - For example, which width should be chosen for the resistor to keep area requirement minimum
- Compact Layout
  - Placement
  - Routing
  - Less vacant area
  - Remember, the larger the area, the higher the fabrication costs
- Reference Book → The Art of Analog Layout by Hastings