Monte Carlo Analysis

This document discusses the Monte Carlo analysis of integrated circuits and will guide you through the respective simulations you have to do for your OPAMP.

1. The Monte Carlo Method

The Monte Carlo method is a way of statistically calculating results of equations with multiple random variables. The method relies on repeated random sampling with specifically distributed fluctuations of input variables to calculate the results. The individual sample results are then aggregated to a final result, which is an approximation of the actual output. The accuracy of the approximation will be poor with only a few samples, but it will improve as more samples are introduced.

In electronic design Monte Carlo is for example used to receive information on how many percent of your chips will meet the requirements in the presence of a statistical variation in the technology parameters (process variation). For example, if you size your circuit, e.g. an amplifier, with a tolerable value for the offset, you will be interested to know if you have a systematic offset and it's maximum deviation. After a Monte Carlo run you can plot a histogram for the values of the offset vs. the number of samples. In this way you get an idea of the robustness of your design against statistical process variation.

Note: This kind of simulation should not be confused with corner simulations, where all identical elements will be influenced in the same way, e.g. all NMOS transistors or all resistors are set to the same "process state".

2. Process Variation and Mismatch

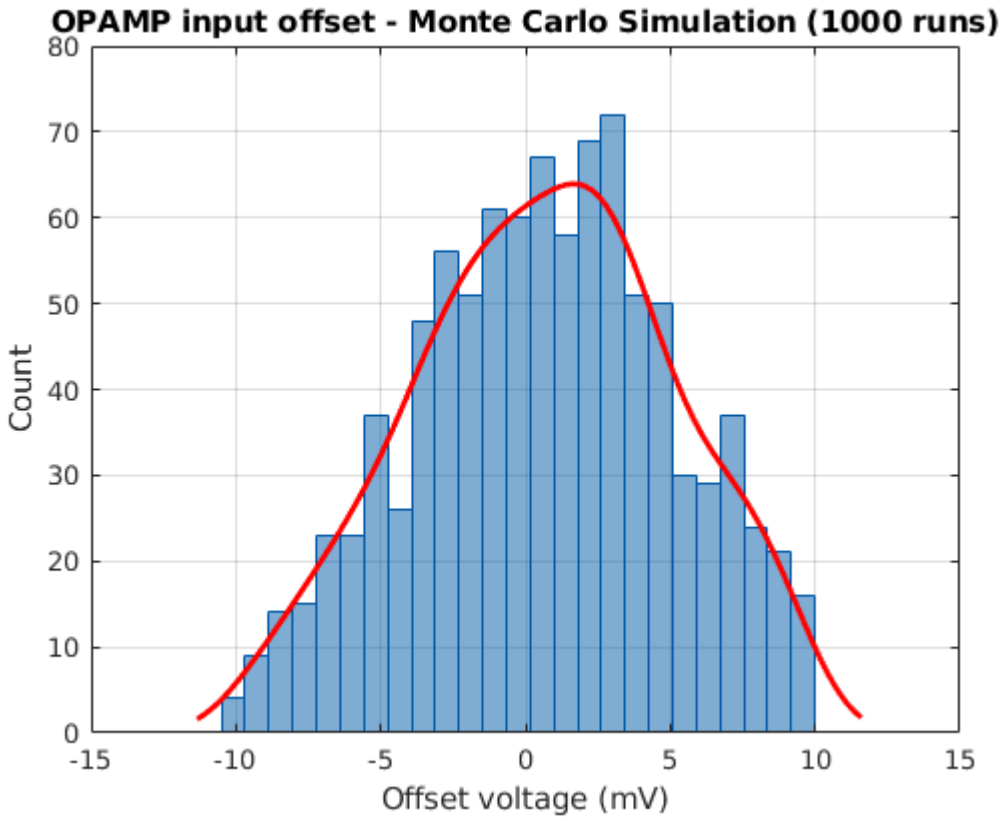
Process variation describes the naturally occurring variation in the attributes of device parameters such as the width and length of transistors, when integrated circuits are fabricated. The variations become particularly important at smaller process nodes. That is because the variation can become a large percentage of the full length or width of the devices. Particularly in analog circuits, process variation causes variance in the circuit performance due to mismatch (see below). Based on the statistical behavior of the fabricated devices, the expected distribution of the system performance can be simulated.

Process variation Monte Carlo analysis considers the variations of the process, not only of all the chips on one single wafer, but also the variations on different wafers and even on different lots. The parameter spreading is provided by the fab and dedicated to the individual process. The spread usually ranges between ±1σ and 3σ (sigma) mean deviations.

Two identically designed devices on an integrated circuit have random differences in their behaviour and hence show a certain level of random **mismatch** in the parameters, which model the behaviour. This mismatch is due to the stochastic nature of physical processes that are used to fabricate the device.

The local mismatch Monte Carlo analysis considers the mismatch of devices, which are located close to each other (adjacent), and which should match as closely as possible. The mismatch is calculated depending on the W & L sizes and a (or a few) parameter(s) dedicated to the process and provided by the fab.

To illustrate the impact on the circuit, the figure below shows the histogram of the input offset of an operational amplifier design. Typical conditions (25°C, 1.8 V supply) with 1000 individual runs are shown. The offset varies between -9.985 mV to 9.924 mV, with a mean of 634 µV and standard deviation of 4.45 mV. Due to the high number of 1000 runs, the input offset of the fabricated chips will have a similar distribution. If for example offset voltages less then 5 mV would be acceptable, then 70% of the fabricated chips would be useable.



3. Monte Carlo Simulation for AICD lab

So far, we have considered only an exemplary mismatch in the input stage of the OPAMP (see *OPAMP_Design/Simulation.pdf*) by manually manipulating the W and L values. However, this will not be representative for the performance of a fabricated chip. At the end of the course, a tape-out is scheduled, where a chip will be fabricated. There, an unavoidable and unknown mismatch will occur during manufacturing. To ensure having a fully functional chip, Monte Carlo Simulations are used to verify the performance under the expected variations and mismatch.

Since the OPAMP is the essential building block of all parts, it plays a major role for the overall performance. The Monte Carlo Simulation will provide insight of the distribution of its performance.
We still have other circuits capable of generating mismatch, which we might need to consider. The relevant factors depend on your chosen task, so ADC, BGR and PGA have different characteristics.

1. ADC:
   The matching of the caps is critical for the overall performance. If the cap ratios differ from the ideal values, the DNL and INL of the overall system are degraded. Also, variations of the switch transistor can affect the ADC performance.

2. BGR:
   Mismatch of the bipolar transistor and the used resistors will affect the output voltage as well as the temperature coefficient.

3. PGA:
   Variations of the resistor ratios/values will directly translate to the gain of the system. Also differences of the on-resistance as well as the leakage of the switches will introduce additional errors.

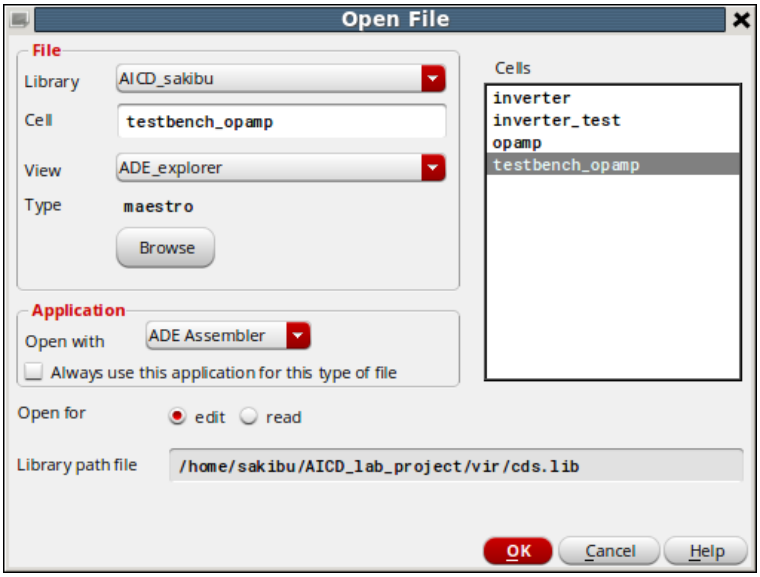
Before discussing how these effects should be investigated, some hints on the general design trade-offs are given. In general, you should find suitable values to reach offset, power, speed and area targets. Mismatch is typically inversely related to the area. So Large area → less mismatch. Small Area → higher mismatch. Besides the increase in area, lower speed and higher power consumption can be a consequence depending on the circuit. Special care must be taken for the design of the capacitor array for the ADC and the resistor string for the PGA.

4. Monte Carlo Analysis using Cadence Virtuoso ADE Explorer

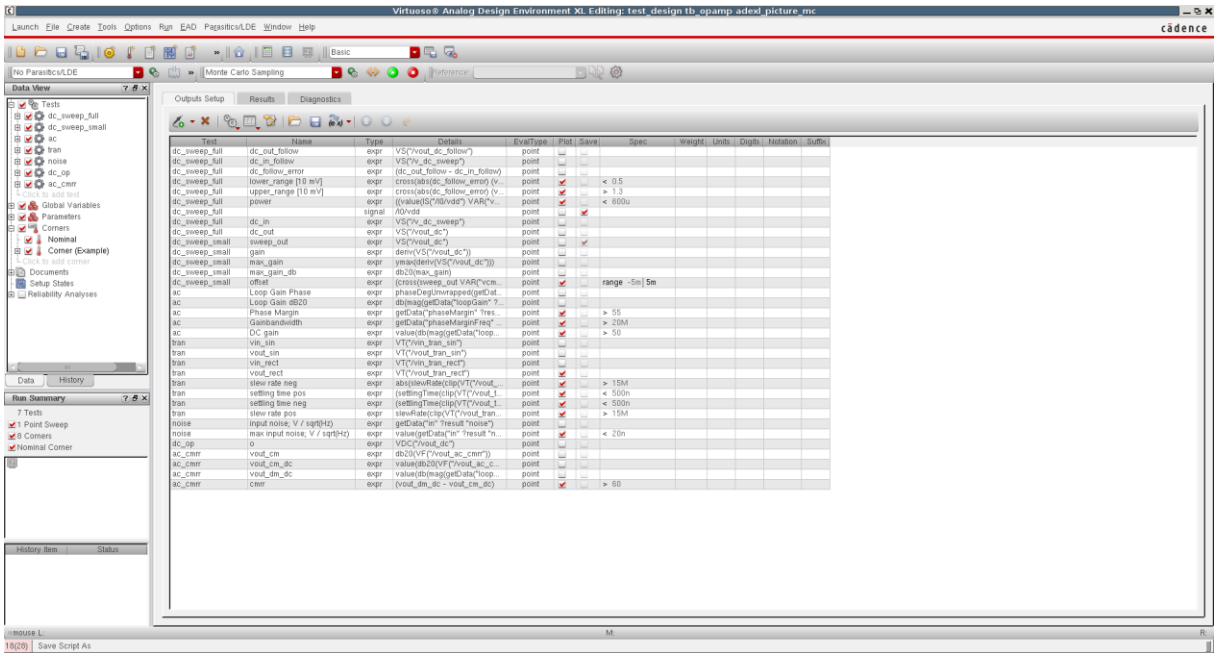
In order to perform a Monte Carlo analysis for the *umc65* technology in Cadence Virtuoso we have to use the ADE Explorer tool. The setup is very similar to the procedure of the corner simulation described in *corner_simulation.pdf.* Only the

model libraries need to be changed and the Monte Carlo Simulation type chosen. The test setup for the corner simulation and Monte Carlo simulation will be combined in one ADE Assembler Editing setup. Therefore, it is expected, that you have already set up the corner analysis. Otherwise refer to the *Corner_simulation.pdf* to do the ADE Explorer setup. Hints about the usage of the model files are also provided in the *Corner_simulation.pdf*.

First, open your ADE Explorer test setup from the Corner Simulation. You can either open this using the Library Manager or from your testbench using the *Launch* → *ADE Assembler* → *Open Existing View* → *ok* (the default values should be sufficient).



Your ADE Assembler Editing setup should look like the example below. Depending on your testbench/setup, the naming and number of tests, as well as the corner definition will vary.



Similar to the Corner simulations the model files have to be changed. Please refer to the *corner_simulation.pdf* for the usage and function of the model files. The path is slightly changed to

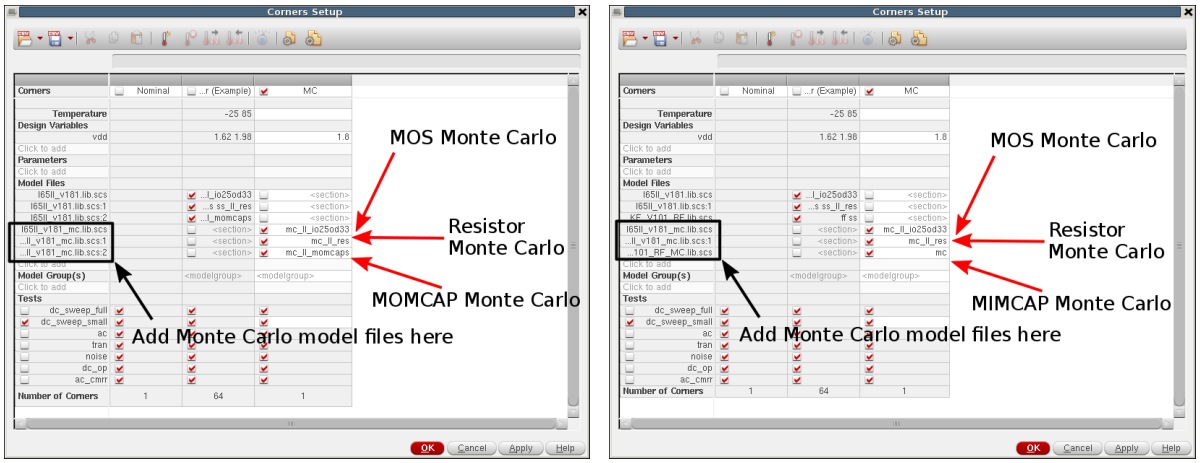
MOS/RES/MOMCAP

/cadstud/cds03/Cadence_Libraries/UMC_TECH/UMC_65/umc_65_ll_ver_B11PB/Models/Spectre/Monte_Carlo/l65ll_v181_mc.lib.scs

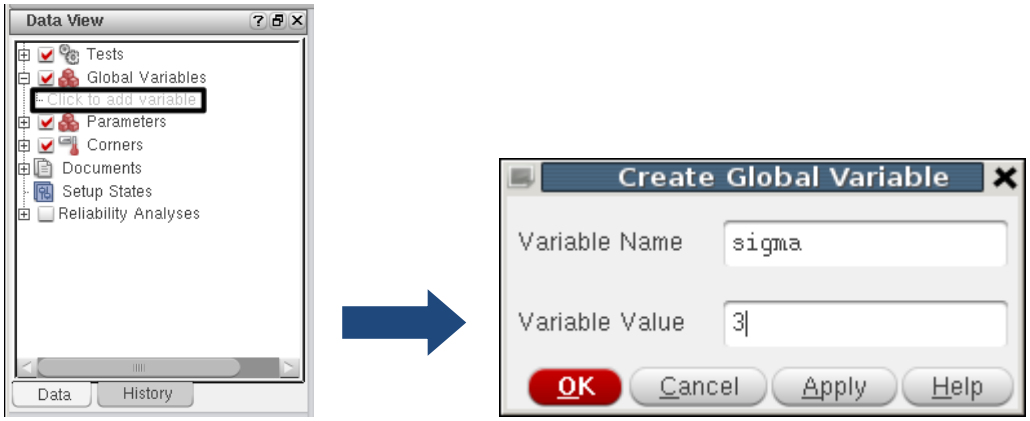
MIMCAP

/cadstud/cds03/Cadence_Libraries/UMC_TECH/UMC_65/umc_65_ll_ver_B11PB/Models/Spectre/Monte_Carlo/L65_MIMCAPS_20F_KF_V101_RF_MC.lib.scs

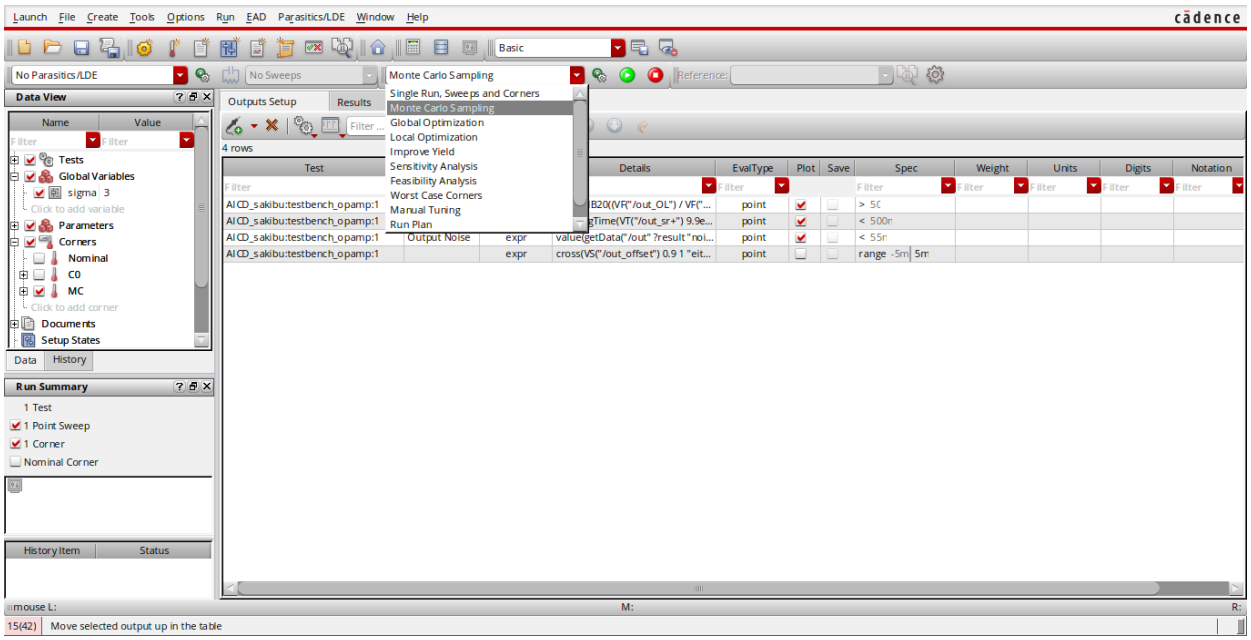
Here you have to use the following parameter names for the devices. For the MOSFETs "**mc_ll_io25od33**", for the resistor "**mc_ll_res**", for MOMCAPS "**mc_ll_momcaps**" and for MIMCAPS "**mc**". Now the Corners setup should look like below. Again, this varies with your choice of MOM (left) or MIMCAPs (right):



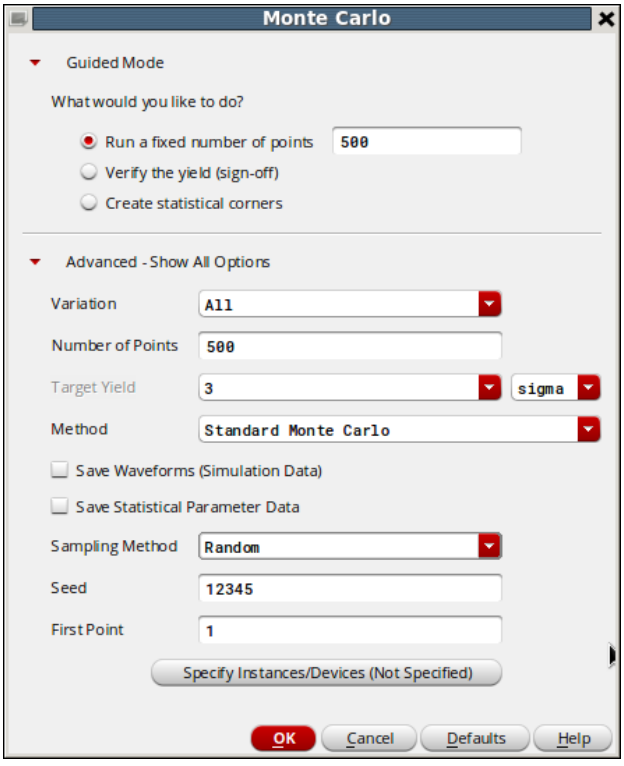
Furthermore, the Monte Carlo analysis requires an additional global variable *sigma*, which you have to add to the test (images below). Otherwise the simulation will stop with an error. The value of sigma will influence the variance of the internally used model parameters. According to the *umc65* process documents, a *sigma* of *3* is recommended. The variables from your test within *ADE explorer* will be listed under *Global Variables*, too.



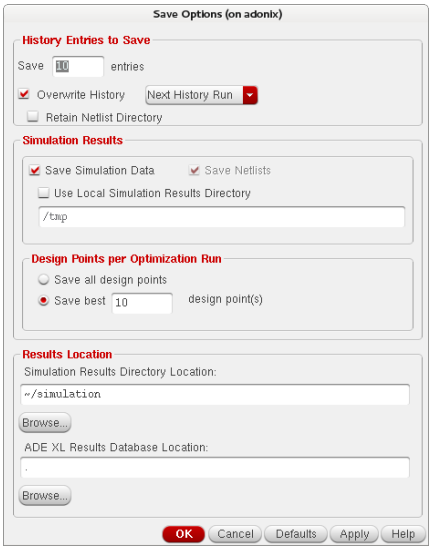
As soon as you have set up the "Corner" with just the Monte Carlo parameters, the Monte Carlo run can be configured. Choose *Monte Carlo Sampling* in the main *ADE explorer* window, as shown in the figure below. In this way *ADE explorer* is configured to perform a Monte Carlo Analysis. Before running the actual simulation, we have to configure the Monte Carlo run by clicking on the symbol right to the dropdown-menu, from which we selected *Monte Carlo Sampling*.



A small window appears. Here we can select, which statistical variations should be considered (only process variation, only mismatch or all). For the CMOS inverter we will consider both, but later for the resistor-string for example we will also perform a pure mismatch analysis. You can also explicitly specify which devices or sub-circuits in your design should be investigated in terms of mismatch. This can be done by clicking on *Specify Instances/Devices*. However, in this example this will not be done, during optimizing your design, this might be a useful function. The only setting that you have to change is the *Number of Points*, which you should set according to your task (see *part 5* and *6*)). This is simply the number of simulations with random parameters that will be performed in the Monte Carlo run.



If the Monte Carlo window does not pop up automatically, click on the highlighted button below:



Before you actually run the simulation, please go to *Options→Save* in the main *ADE explorer* window and select *Overwrite History* in the appearing window. In this way the results of each Monte Carlo run will be overwritten when you start a new run. This is important as it prevents disk quota problems with your AICD lab accounts! The generated data by the simulator will quickly eat up your available disk quota. If you experience disk quota issues, please refer to Point 3 of the *Troubleshooting.pdf*

Before starting the simulation, make sure that only the configuration with the Monte Carlo model files of the Corner setup is *checked*, *uncheck the remaining*. If non-Monte Carlo related setups are enabled, an error like below will occur. Now you are ready to start the run by clicking on the green play button. In the lower left corner of the main *ADE explorer* window you can then follow the progress of the simulation. Once the Monte Carlo run is finished, the results, i.e., your selected outputs to be plotted, are automatically displayed (see figure below).

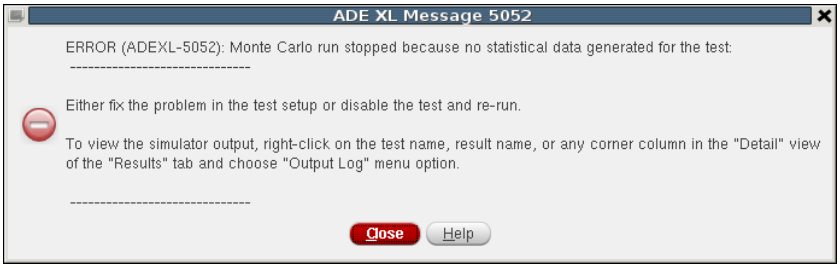
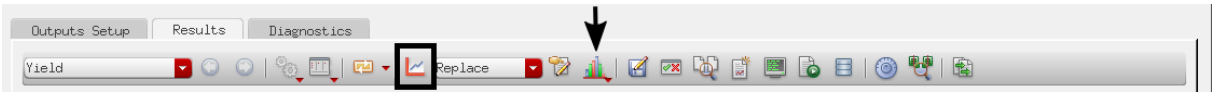


Figure 1 Error message, if a non Monte Carlo setup is run as Monte Carlo simulation.

As it can be seen in Figure 2, the Monte Carlo run reveals the statistic properties of the design values. In this example it is done for the opamp offset. While the mean offset of 615.6 µV is close to the ideal value of 0 V, the extreme values can vary between -16.93 mV and 17.05 mV, which is far outside the target of 5 mV. As a designer, one could now for example try to decrease the standard deviation

by increasing the transistor sizes, which might reduce the influence of mismatch. Of course, this is just for demonstration purpose, your design will have different results and you might face different challenges.

Figure 3 shows the respective histogram of the Monte Carlo run which can be plotted after the simulation finishes, using the following option. For an automated plot of the result use the button indicated with a square. The menu at the arrow can be used for detailed, specific plotting. For example, the correlation between different properties can be investigated.



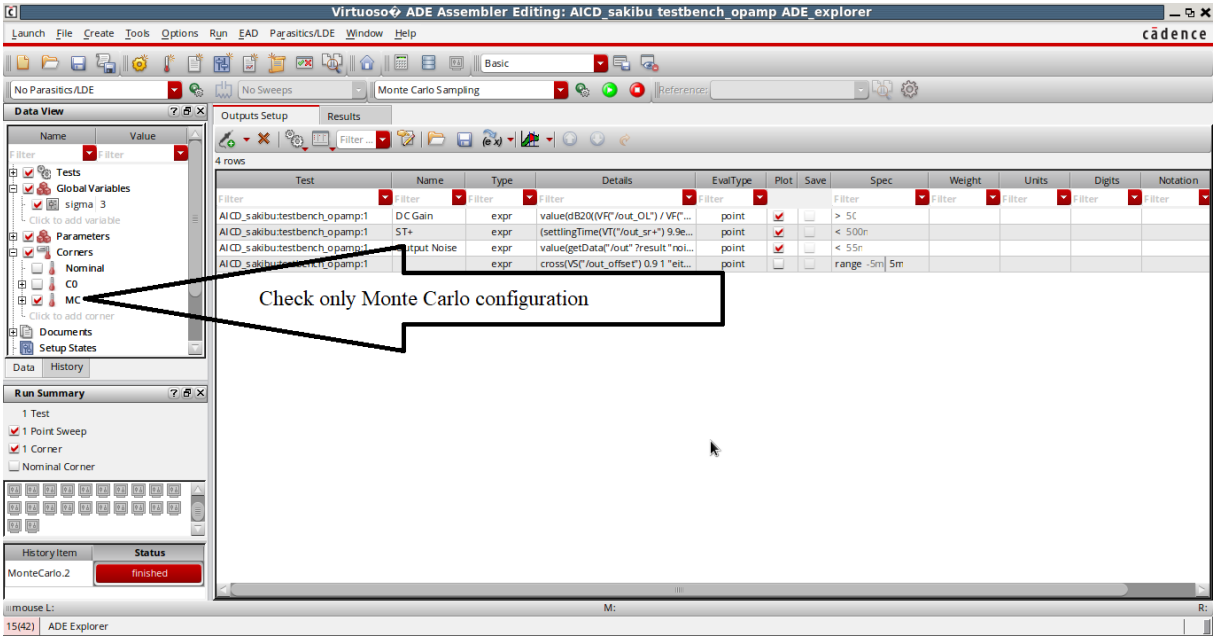


Figure 2 ADE XL after run of Monte Carlo simulation

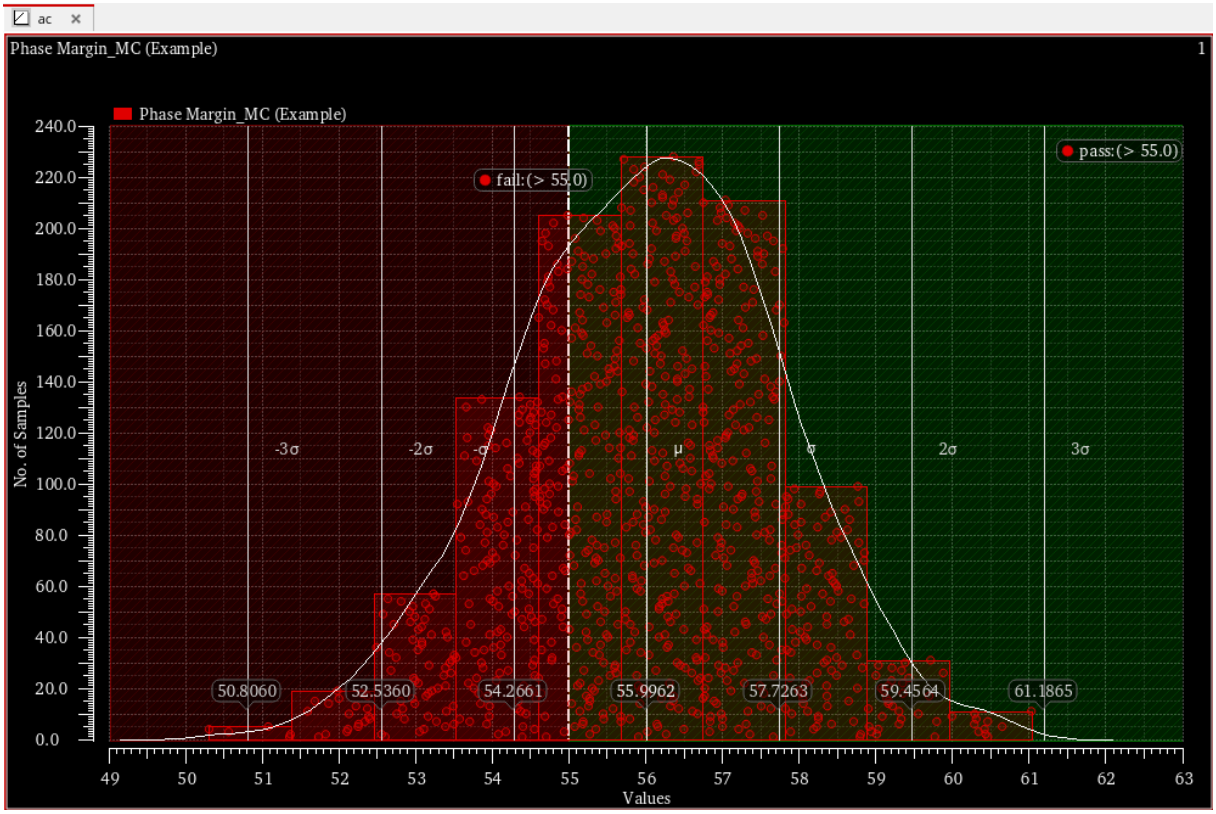


Figure 3 Exemplary plot of the Monte Carlo results

5. Monte Carlo Analysis of the OPAMP

Once the OPAMP layout design is complete, each group has to perform a Monte Carlo analysis of the OPAMP parameters mentioned below in order to investigate how mismatches and process variations in the components used in the OPAMP influence the performance of the OPAMP.

Settings for the Monte Carlo runs:

- Statistical Variation: Process and Mismatch! (All)
- Number of Points: 1000

Outputs to be calculated for the Monte Carlo runs:

- DC Gain
- Gain Bandwidth
- Phase Margin
- Slew Rate +ve
- Slew Rate –ve
- Settling Time (high)
- Settling Time (low)
- Offset

Use the Cadence Virtuoso Calculator tool to create the expressions for these outputs! In case groups have problems with the calculator and its predefined functions, they can ask the supervisor. Due to the high amount of necessary runs in the background, the simulation may take a while (ca. 15 min to 1h).
For the Monte Carlo simulation, the DC gain, Gain Bandwidth and Phase margin need a different test bench approach. Please consider section 7 to avoid flawed results for gain, gain bandwidth and phase margin.

The results (min., max., mean and sigma values) of the Monte Carlo runs should be listed in a table, as described in the document *Written_Report.pdf*! Based on these results and other aspects (like area or routing complexity), groups may decide to optimize the design.

6. Monte Carlo Analysis of ADC, BGR and PGA

Mismatch effects in the remaining circuit can also significantly deteriorate the overall performance of your building block. The required simulations depend on your individual task.

BGR:

Here the output voltage and the temperature coefficient need to be investigated. Check the min, max, mean and std of these properties using the Monte Carlo analysis. Use

- Statistical Variation: Process and Mismatch! (All)
- Number of Points: 1000

PGA:

Here the gain is of main interest. Check the min, max, mean and std of these properties for all possible binary input codes (000, 001, … , 111) using the Monte Carlo analysis. The number of points is reduced to only 100 for a faster simulation runtime (Since in total each run must be done for all 8 possible input codes). Use

- Statistical Variation: Process and Mismatch! (All)
- Number of Points: 100

ADC:

Here the INL/DNL as well as SNR/SINAD/ENOB are of major interest. Unfortunately, a single run has a runtime of over an hour. So, a Monte Carlo as well as Corner Analysis of the ADC is not feasible within the resources of this lab and hence skipped.

7. New Testbench for AC Simulation (for Monte-Carlo Runs)

At this point it is assumed, that the testbenches according to *OPAMP_Design&Simulation.pdf* have already been successfully setup.

As you probably noticed during optimization of your design, setting the right offset voltage is a crucial pre-requisite for a meaningful simulation. The right offset ensures that the OPAMP is working at a correct DC operating point. Thus, the linearized circuit by the ac simulation represents the circuit behavior. If the

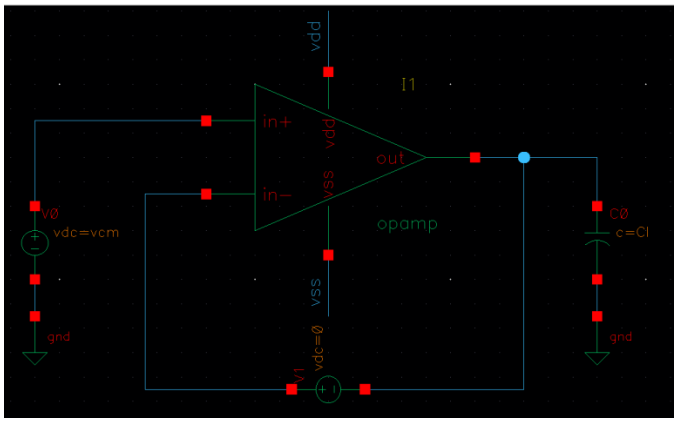
offset is insufficiently compensated, the DC output will be close to one of the supply rails. This means, that the transistors are not working as intended and thus poor ac performance will be obtained. Since a proper DC operating point will be ensured by the overall circuit (BGR, PGA, ADC), these conditions will not appear during the real operation of the device.

Since the Monte Carlo Simulation use random deviations for all devices, the input offset voltage will vary randomly. Consequently, the offset needs to be compensated for each single run. The previously used manual compensation technique is not feasible any more, so a different simulation setup is necessary.

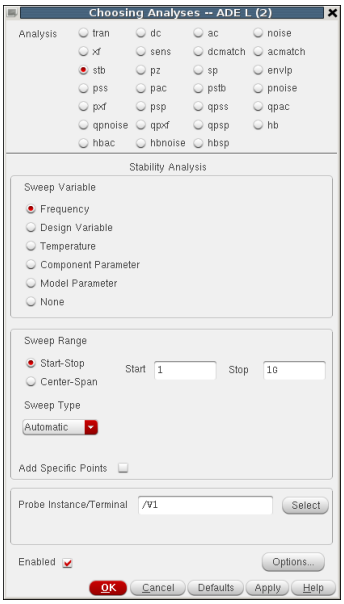
The so called stability (stb) analysis of the Cadence spectre simulator provides a convenient simulation setup for this task. It is based on the closed loop circuit. This ensures that the DC operating points are correct. An additional voltage source must be integrated in the feedback path. The stability simulation will calculate the AC gain based on this added source.

7.1. Cadence Setup

First, set up the testbench circuit as shown below. The common mode voltage is applied to the non-inverting input of the operational amplifier. The OPAMP itself is configured as unity gain follower with the mentioned voltage source (0V) in the feedback path. As usual, the output of the OPAMP is connected to the load capacitance.



Add a new *Test* in the ADE XL window, like already done for corner simulation (*Corner_simulation_umc65.pdf*). In your ADE window, choose the *Analyses → stb* simulation. The *sweep range* can be configured like a normal ac simulation. In the additional *Probe Instance/Terminal* insert the voltage source of the feedback path using the select button. See image below.



After the setup has been completed, start the simulation using the green run button. After finishing, the outputs have to be added. Go to *Results → Direct Plot → Main Form* in the ADE L window. The direct plot window like shown below will appear. There you can select the functions and add them to the ADE L outputs by using the *Add To Outputs* button. Based on this you can setup the relevant parameters for DC gain, Phase Margin and Gain Bandwidth (cadence naming can be slightly different). Verify your outputs manually once, to make sure the setup is correct. As soon as the correct values are shown in the *Value* column of the ADE L outputs, this testbench is ready for Monte Carlo Simulation.