# Reference Testbench

The preparation of a testbench is an essential step in the design flow. We need a testbench in order to simulate the specified properties of our circuit. Based on simulation result we can judge the performance of our design and make improvements if necessary. Hence, any undetected errors will lead to wrong simulation results, heavily affecting the optimization process. Potentially this can lead to a flawed design.

Hence, we provide this reference testbench for the Opamp as additional safety net to eliminate consequential errors. It simulates all essential parameters and waveforms for the AICD Lab. Please use it to validate your simulation results.

We still highly encourage you to use your own testbench. Especially during optimization, it can provide additional design insight. You can modify it and e.g. monitor internal nodes easily. Instructions for the advanced simulation strategies of Corner and Monte Carlo can be found in moodle. (Corner_Simulation.pdf and Monte_Carlo_Simulation.pdf).

**Please note:** Although we call this reference testbench, it is not(!) a sample solution. We intentionally use a different (and unusual+complicated) method for the reference testbench. Therefore, this testbench won't be helpful in case this leaks to students of the following years.

General remark: Even with a correctly setup testbench you might experience small variations. Different settings like simulation accuracy, step size as well as slight difference of the expression definition will lead to minor variances. Differences in the third significant figure can be tolerated. Some parameters tend to be more sensitive to variations than others.

## Getting the Reference Testbench

Please close cadence virtuoso first and make sure it is properly closed. To get the reference testbench open a terminal and type the following command:

```
sh ~/lehrepub/aic/AICD_lab_project/get_reference_testbench.sh
```

## Structure of the Reference Testbench & Preparation

The structure of the *reference_testbench* library is shown in Figure 1. Only the two read marked cells "Opamp_DUT" and "reference_testbench" are relevant for the usage of the library. Please do not modify any other cell.

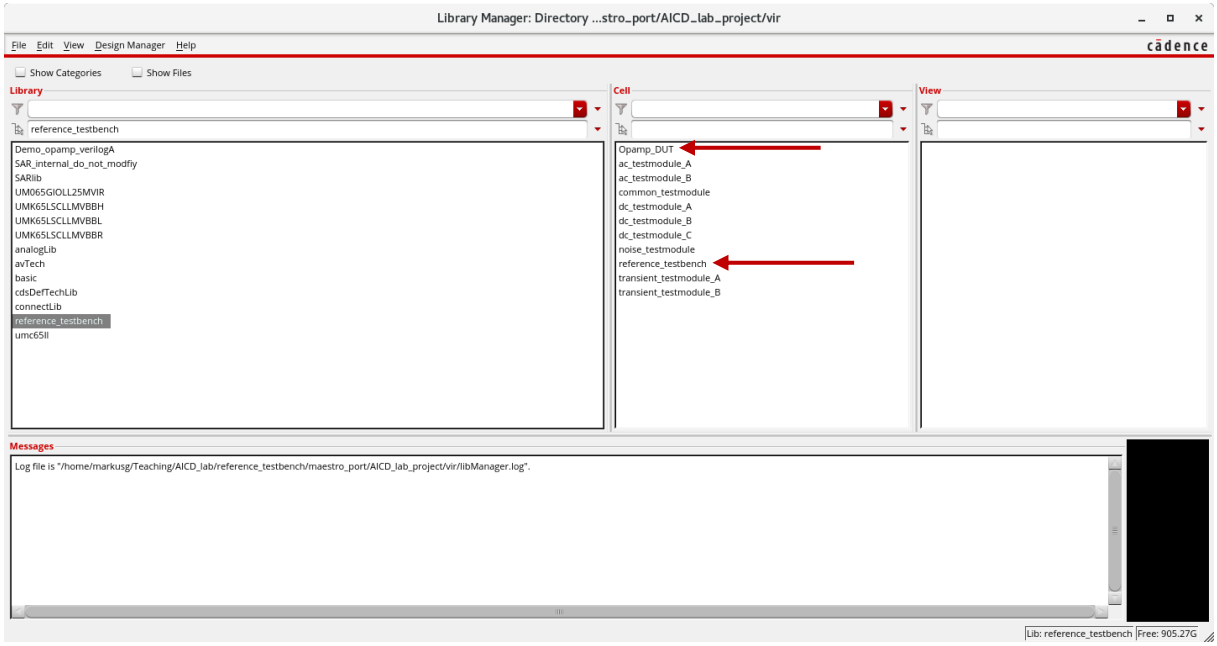


Figure 1 Library view of the *reference_testbench*

The "Opamp_DUT" specifies your OPAMP for simulation. To prepare the testbench for simulation of your OPAMP, please open the schematic of the "Opamp_DUT" cell. As shown in Figure 2, remove the existing Opamp (the verilogA opamp is inserted as place holder) and replace it with your design. Make sure to connect the pins of your Opamp with the respective pins in the schematic. Now, the reference_testbench is fully prepared and ready for simulation.

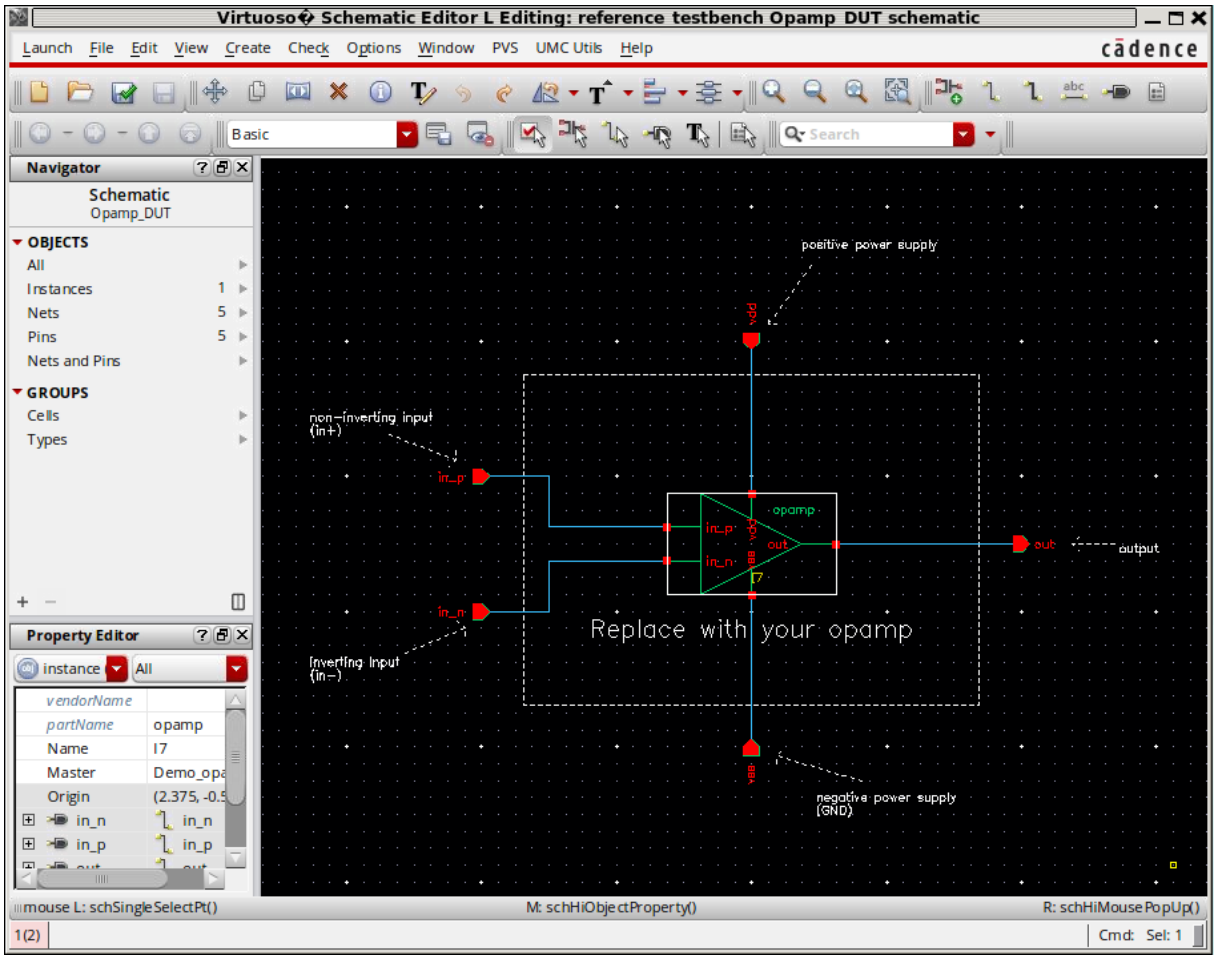


Figure 2 The schematic of the "Opamp_DUT". Please replace the Opamp inside the schematic with your own.

The "*reference_testbench*" includes the testbench itself with all relevant simulation setups. All 5 views can be seen in Figure 3. There are two cellviews for the **ADE Explorer** simulation tool, one **ADE Maestro** state for Corner and Monte Carlo simulation as well as a **config** for Post Layout simulation. Additionally, the **schematic** itself is included. Be careful to not change any of these cellviews, since this might break the testbench or cause flawed simulation results.

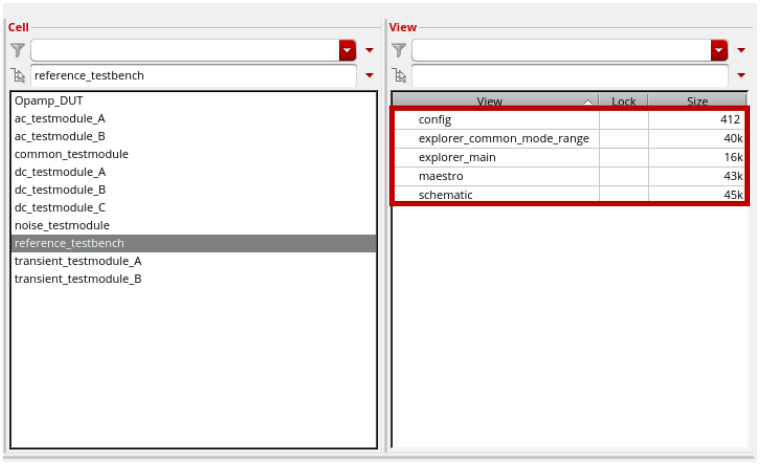


Figure 3 Available cellviews of the reference testbench.

## ADE Explorer: Running Typical Case Simulations

Two ADE Explorer views are provided. You can just open them by double clicking on the cellview.

### *explorer_main:*

This is the main simulation state with the setup for dc, ac, transient and noise simulation. With exception of the common mode ranges (ICMR and OCMR), it includes all relevant performance parameters and plots the essential waveforms. An example is shown in Figure 4.

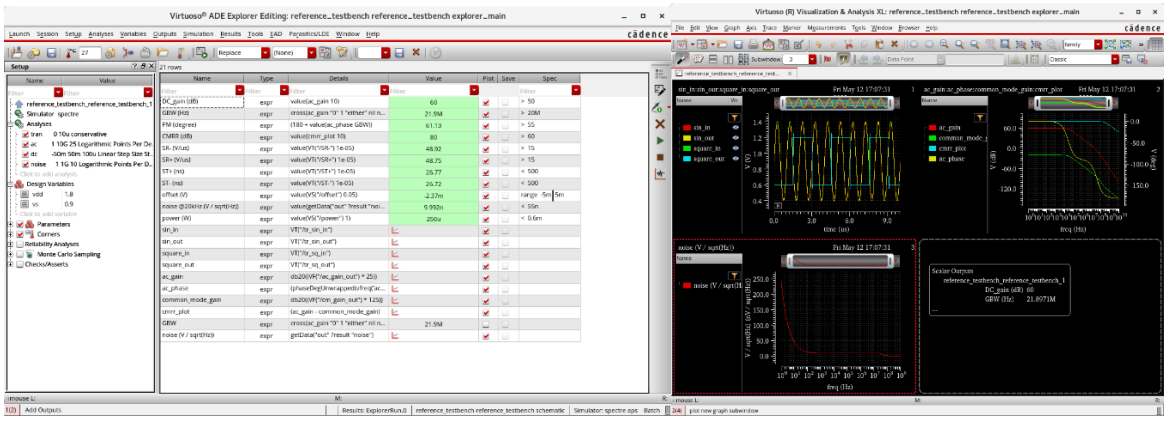

Figure 4 ADE Explorer Main state and plotted waveforms.

### *explorer_common_mode_range:*

This is a dedicated state just for the Input common mode range (ICMR) and output common mode range (OCMR). Since these require different sweeps, it is separated in an additional state. An example is shown in Figure 5.

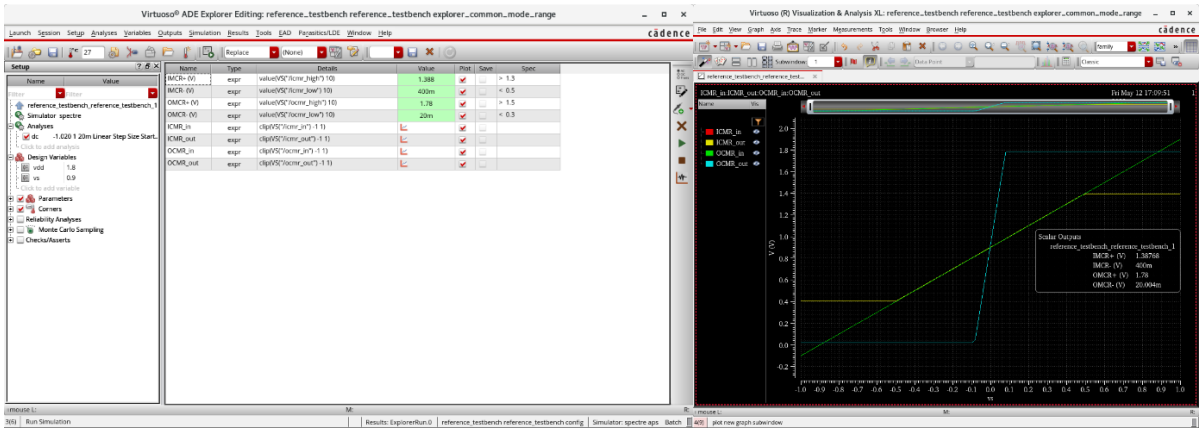

Figure 5 ADE Explorer state for the common mode range simulation and plotted waveforms.

## ADE Maestro: Corner & Monte Carlo Simulation

For running Corner and Monte Carlo Simulation we will need ADE Maestro. Detailed instruction on setting up ADE Maestro and usage can be found in the *Corner_Simulation.pdf* and *Monte_carlo_Simulation.pdf* in Moodle.

**For the following instructions, it is assumed, that you have already read the Corner and Monte Carlo pdfs available in moodle.**

Please open the *maestro* view. The ADE Maestro window should look like Figure 6. At the highlighted section
you can see different tests. Per default, "*main*" is chosen. This includes all relevant parameters with exception of the common mode range. It is identical to the ADE Explorer state "*explorer_main*". In case you are only interested in a specific simulation you can disable the main test and activate one of the other "*transient_only*", "*ac_only*", "*offset_only*", "*common_mode_range_only*" and "*noise_only*", depending on what you wish to do.

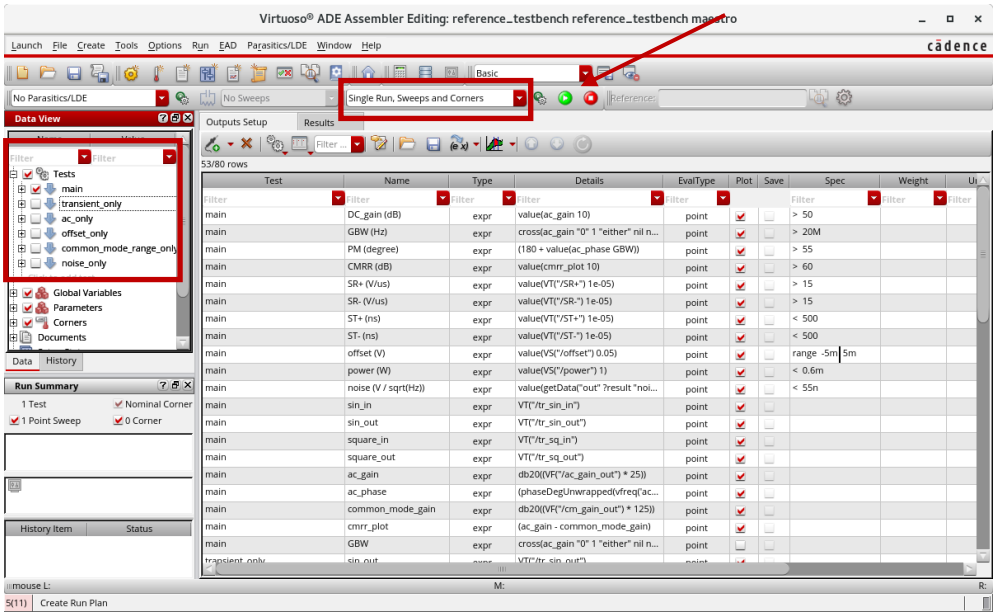


Figure 6 ADE Explorer main window

### Corner Simulation

The Corner Simulation will check the circuit performance for various conditions. It will test it at -25°C and 85°C, at 1.68V and 1.98V supply voltage and for the extreme cases of process variations (slow and fast). The transistors have 4 extreme cases: Fast-n and Fast-p, Fast-n and Slow-p, Slow-n and Fast-p, Slow-n

and Slow-p. Furthermore, devices like resistor, MOMCAPS and MIMCAPS have two extreme cases: fast and slow.

The total amount of runs is the multiplications of the number of extreme cases for parameters. In our case: 2*2*4*2*2*2 = 128 points. When your design does not include a resistor, MOMCAP or MIMCAP you can remove the extreme cases to save Simulation runs/runtime. This is illustrated in Figure 7, just disable the entry for the device type.

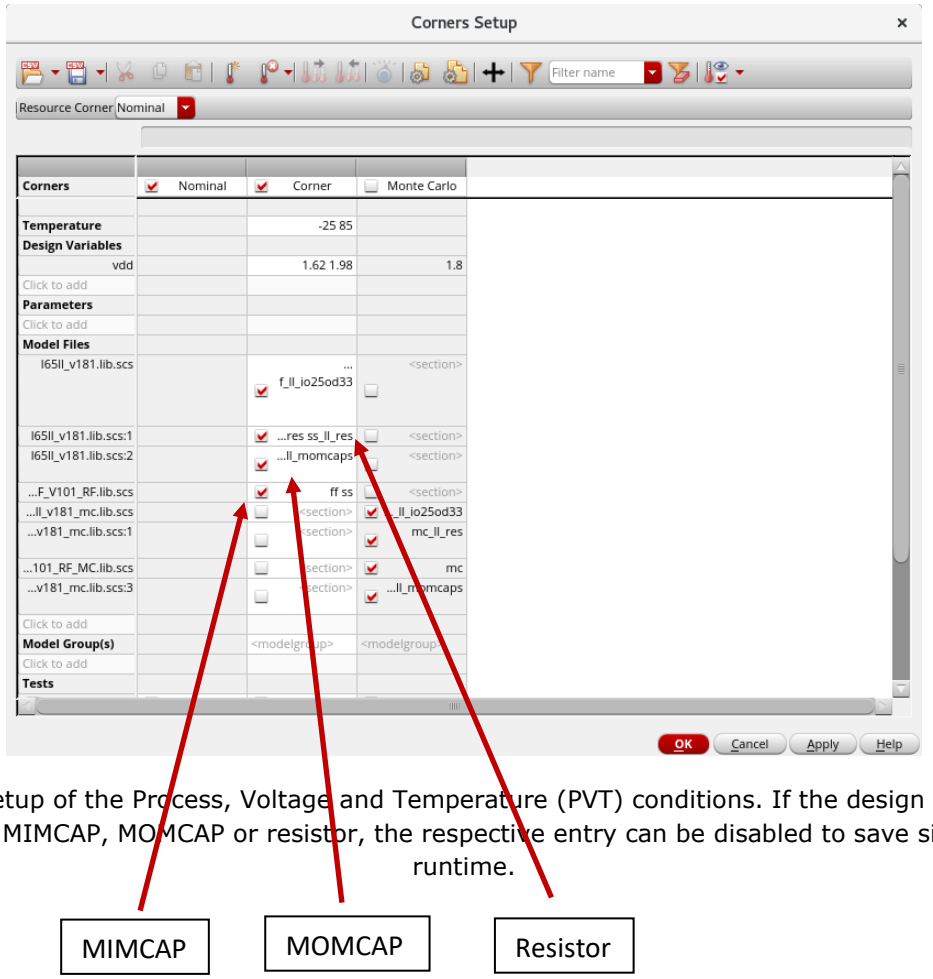


Figure 7 Setup of the Process, Voltage and Temperature (PVT) conditions. If the design does not include a MIMCAP, MOMCAP or resistor, the respective entry can be disabled to save simulation runtime.

To start the corner run, click on the green run button as highlighted by the arrow in Figure 6. Make sure that the text form left of the run button shows "*Single runs, Sweeps and Corners*". Also check that the Corner is activated, and the Monte Carlo deactivated as shown in Figure 7. Upon simulation you will see the performance for all the corner points, similar to Figure 8.

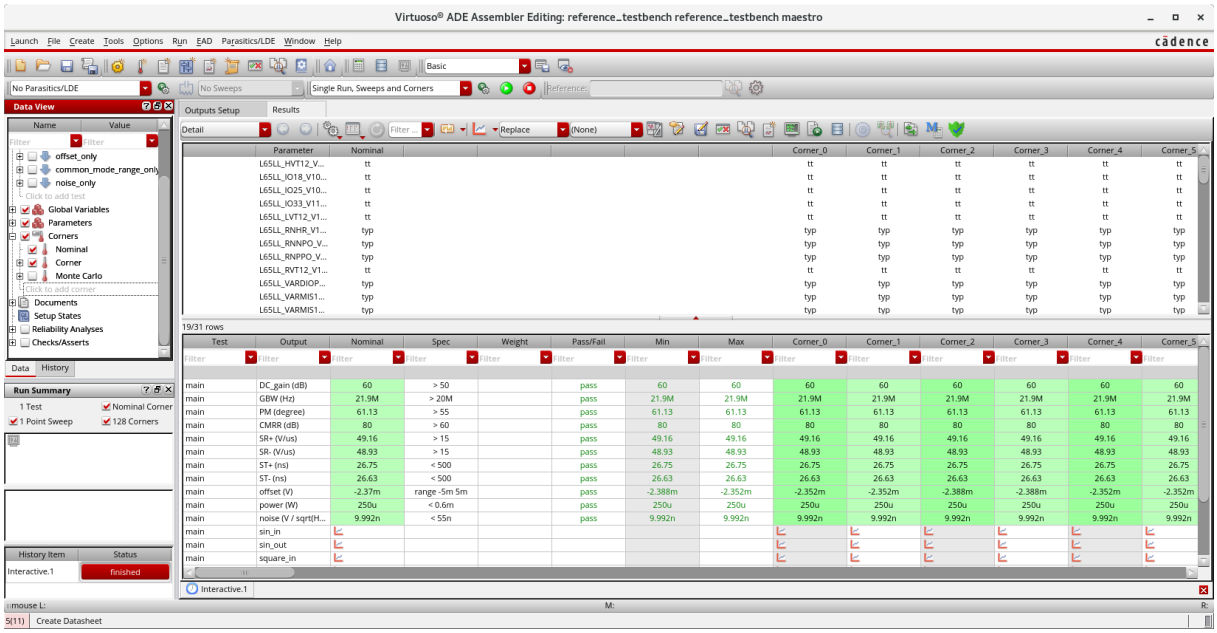


Figure 8 Example outcome of a corner simulation (This shows results of the ideal Demo verilogA Opamp, which is not affected by the temperature and process variations. Your OPAMP will show different values for each corner point!!)

## Monte Carlo

Change the settings to Monte Carlo. As seen in Figure 7, disable the "*nominal*" as well as "*Corner*" and enable "*Monte Carlo*". Switch the mode from "*Single, Runs, Sweeps and Corners*" to "*Monte Carlo Sampling*" (mode type highlighted in Figure 6). By clicking on the gear symbol right of the mode you can set the number of Monte Carlo runs. A window as shown in Figure 9 will appear and the "Number of Points" can be set accordingly. By clicking on run you can start simulation, which will now run the Monte Carlo simulation.

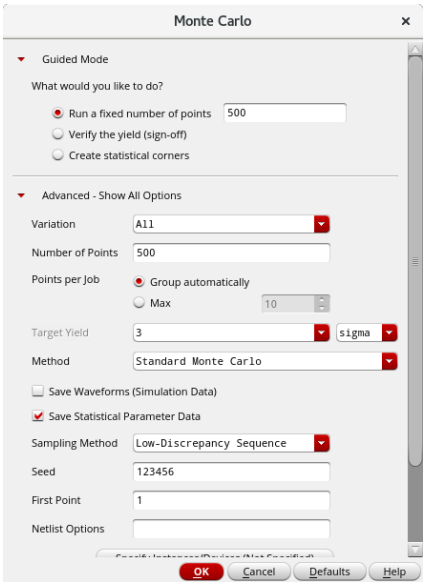


Figure 9 Setting the number of runs for the Monte Carlo Simulation.

## Speeding up ADE Maestro Simulations

Since a lot of simulation at different conditions will be conducted, the simulation runtime will increase significantly. Because the simulation runs are independent from each other, we can run multiples in parallel. To do so, please go to *Options → Job Setup ...* . The window shown in Figure 10 will open after a few seconds. At *Max. Jobs* you can enter 8 instead of 1 to speed up the simulation

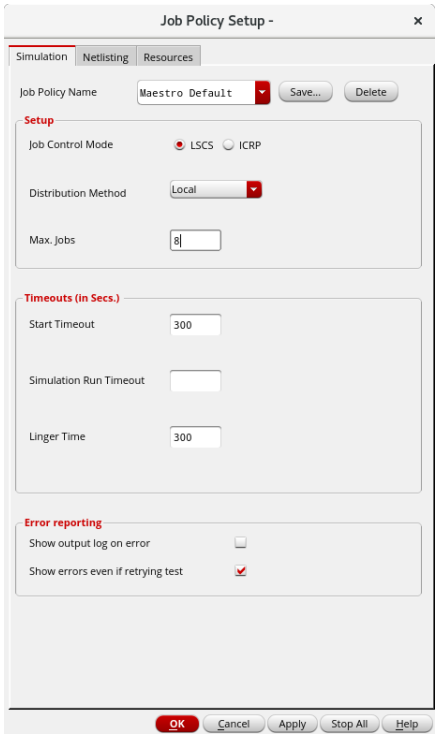


Figure 10 Setting up multiple job to shorten simulation runtime.

## Post Layout Simulation

First, please check the *Post_Layout_Simulation.pdf* in moodle. **You must follow the instructions about the parasitic extraction of the layout. This will generate an av_extracted view, which includes all parasitics from your layout.**

Switching between schematic level and post-layout simulation is done using the *config* cellview (Figure 3). The config will look similar to Figure 11. It lists all elements present in the design hierarchy and shows used views. Find the entry of your Opamp based on its library and name. The "*view found*" column then shows the used view. By right clicking on it you can switch between "*schematic*" for schematic level simulations and "*av_extracted*" for Post-Layout simulation.

As soon as the desired view is chosen in the config, click save and close the config. Then you can proceed with the simulation.

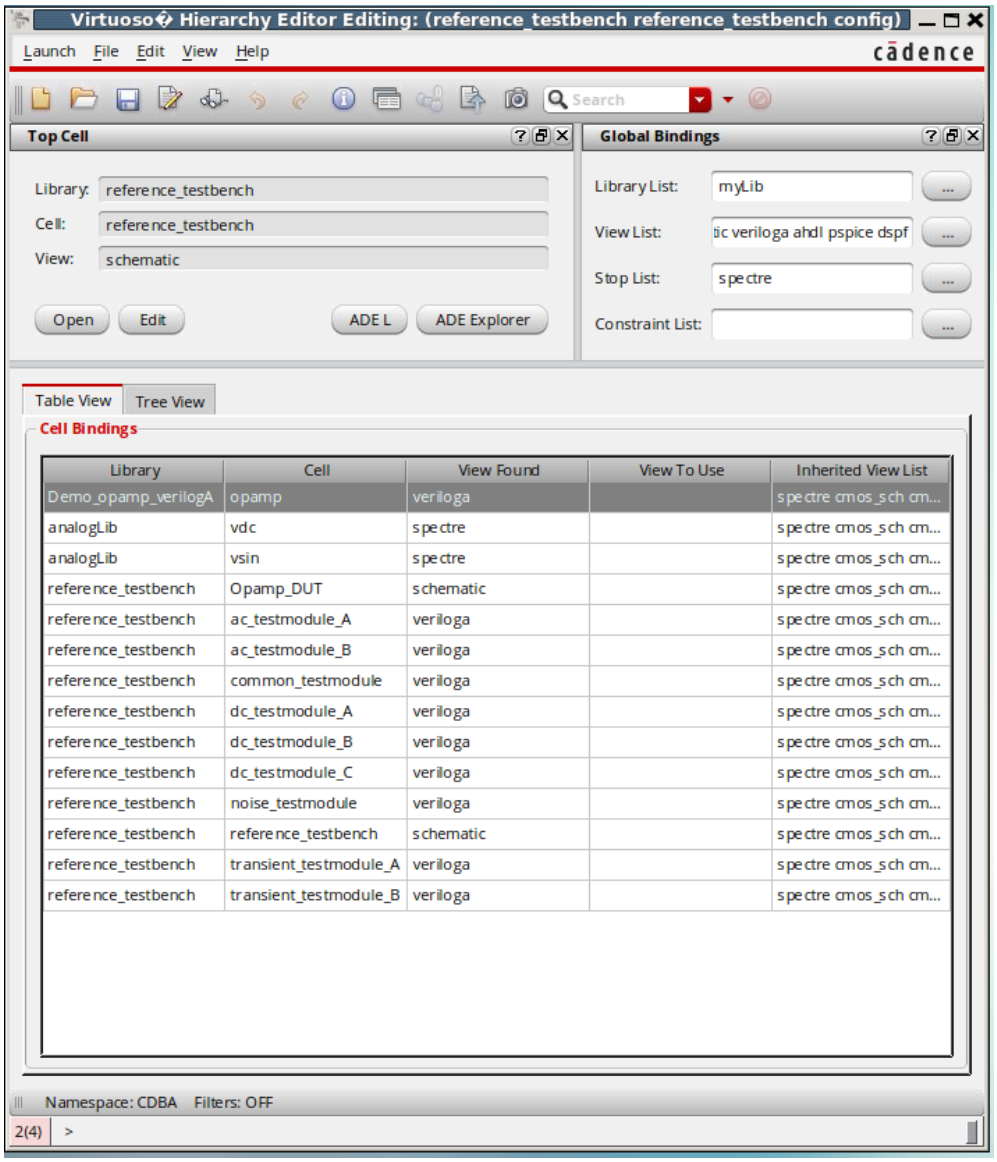


Figure 11 Example of a config.