Advanced Integrated Circuit Design Lab

Project Description BGR

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Overview of the Design Task

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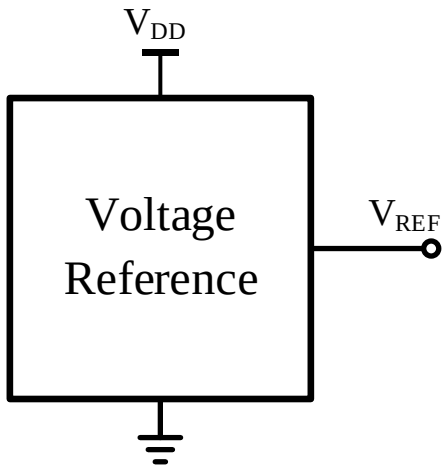
Bandgap Reference based Voltage Reference (BGR)

Voltage references are used to produce constant voltages for other circuits in a system. In case of the audio amplifier IC which we are considering in this lab, the voltage reference is used to produce a common-mode reference voltage (V_{REF}) for the 8-Bit Successive-Approximation-Register-ADC (SAR-ADC) and the programmable gain amplifier (PGA).



BGR - Architecture

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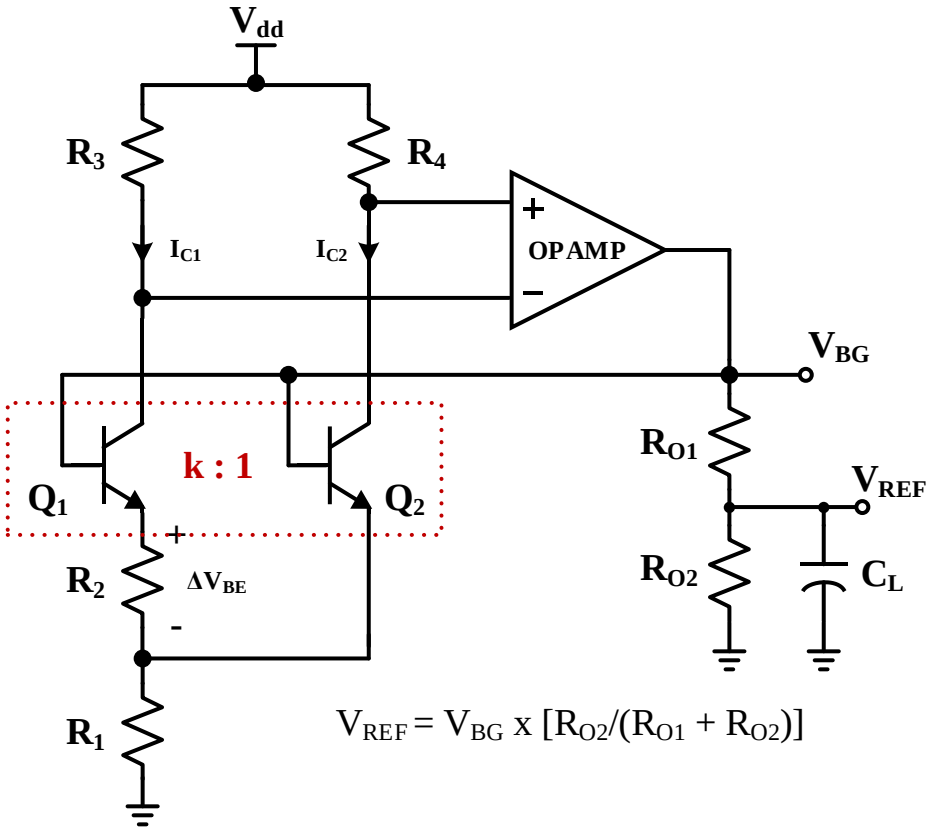
- The BGR circuit uses a Brokaw cell implementation to generate a reference voltage that is less sensitive to supply voltage, temperature and process variations.
- The circuit is based on the bandgap voltage of silicon to generate 1.205 V.
- This bandgap voltage can then be scaled to generate the reference voltage required for PGA and SAR_ADC.

The internal structure is depicted on the next slide.

Brokaw Cell Voltage Reference

- Use a Brokaw cell configuration to generate the bandgap reference voltage and from that in turn generate the 0.9 V reference voltage required for the PGA and SAR-ADC.



Use BJT
NPN_V20X20_LL

Brokaw Cell - Principle

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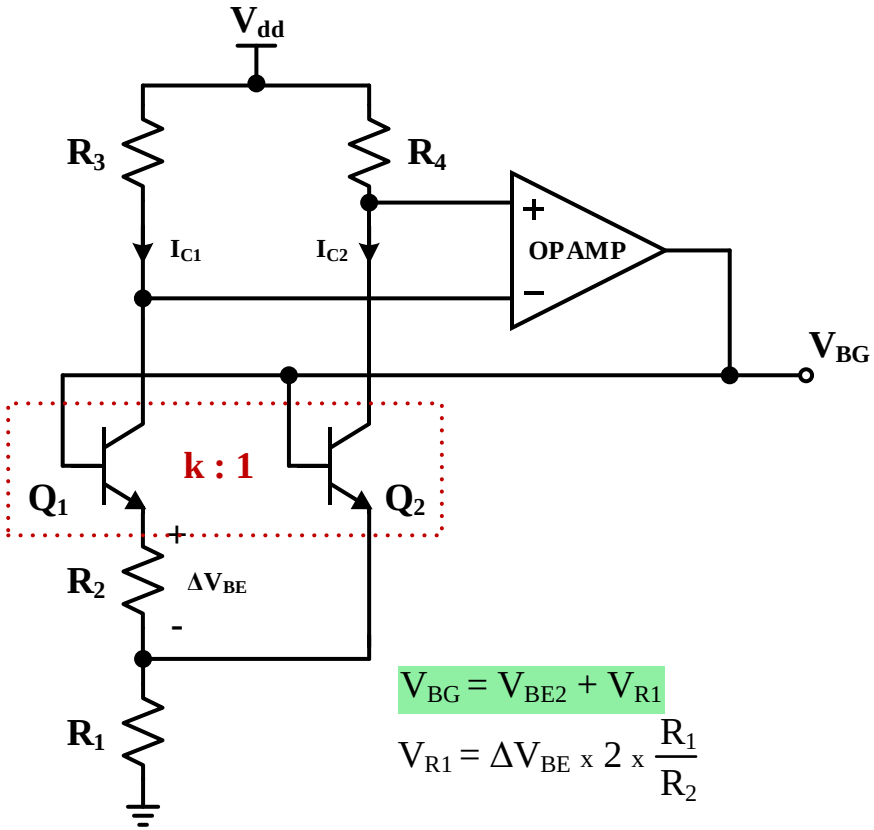
- Temperature compensation
  - V_{BE} of a BJT decreases with temperature → Complementary to absolute temperature (CTAT).
  - $\Delta V_{BE} = V_{BE2} - V_{BE1}$ increases with temperature → Proportional to absolute temperature (PTAT).
  - The PTAT and CTAT characteristics are combined to compensate the temperature dependence of V_{REF}.
- Dimensioning
  - Emitter area's of Q_1 and Q_2 have a ratio of k:1.
  - The value of k was 8 for the originally proposed Brokaw cell [AD580 from Analog Devices].
  - The k needs to be adjusted for the technology being used → use simulations to find the k value for *umc65ll* technology with which you will be working in this lab.

Brokaw Cell – Generate V_{BG}

- V_{BG}
  - V_{BG} = 1.205 V.
    - Silicon bandgap voltage.
  - Generated by compensating CTAT and PTAT behaviours.

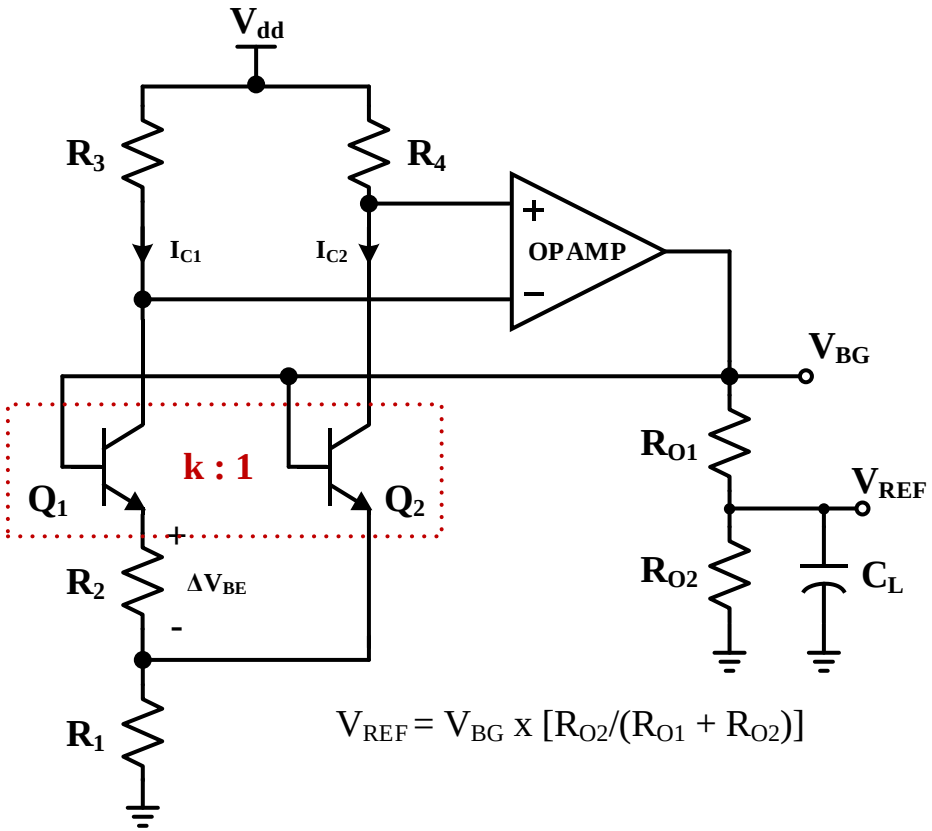


$$V_{BG} = V_{BE2} + V_{R1}$$

$$V_{R1} = \Delta V_{BE} \times 2 \times \frac{R_1}{R_2}$$

Brokaw Cell – Generate V_{REF}

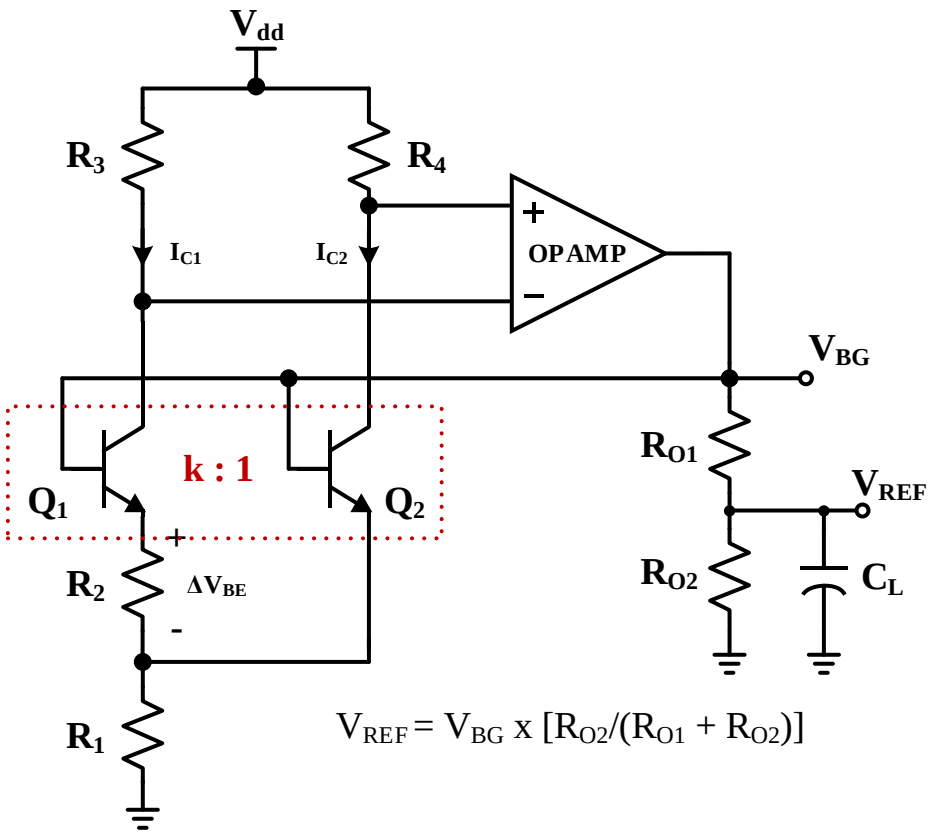
- V_{REF}
  - Add a resistive divider to generate V_{REF} from V_{BG}.
  - A decoupling capacitor C_L is used to stabilize V_{REF}.
  - Choose $C_L \approx 250$ fF



Brokaw Cell – Startup

- Startup-circuit
  - Intended operating point
    $V_{BG} \approx 1.205$ V
  - There can be another stable operating point:
    $V_{BG} \approx 0$ and $I_{C1} = I_{C2} \approx 0$

→ Add a circuit to avoid the undesired operating point



BGR - Specifications

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- The below specifications have to be met for all corners (based on post-layout simulations):

Parameter	Unit	Specification
Reference Voltage (V_{REF})	V	0.9
Tolerance	%	< 3
Temperature Coefficient (TC) *	ppm/°C	< 100
DC Power Consumption	uW	< 1100
Power Supply Rejection Ratio (PSRR)	dB	> 40

* here defined as: $TC = \left|\frac{V_{max}-V_{min}}{T_{max}-T_{min}}\right|$ for the temperature range $T_{min} = 20°C$ to $T_{max} = 40°C$

- The Monte-Carlo simulations (no. of runs = 500) should satisfy the following (based on post-layout simulations):

Parameter	Unit	Specification
Standard Deviation for V_{REF}	%	< 1
Standard Deviation for TC	ppm/°C	< 50

BGR – Essential Information I

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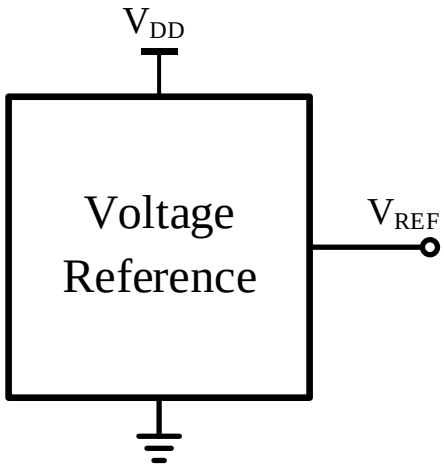
- Supply voltage
  - The single supply voltage is V_{DD} = 1.8 V. Use *vdc* components from the *analogLib* library in simulations. In the hierarchical modules use components *vdd* and *gnd* to specify the global supply nets (see Cadence_Virtuoso_Tutorial.pdf).
- Corner analysis
  - The following corners need to be considered:

Corners		Range
Supply [V]		1.62, 1.98
Process Corners	mos	ff, fs, sf, ss
	res	ff, ss
	cap	ff, ss
	bjt	ff, ss
Temperature [°C]		0, 85

BGR – Essential Information II

- Simulations
  - Use DC analysis for V_{REF}, TC, Tolerance and DC Power Consumption measurements.
  - Use XF analysis for PSRR measurement.
  - V_{DD} = 1.8 V.



- Start-up Verification
  - A start-up circuit should be implemented to ensure that the circuit behaves as expected after power on.
  - Use transient analysis for start-up verification.
  - Use a ramped supply with a rise time of 10 ms for the simulation.
    - Use *Vpulse* component from *analogLib* for this ramped supply.

Implementation Tips

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Use *RNHR_LL* resistors. Avoid excessive resistance, keep it well below < 1MΩ

Temperature coefficient can be optimized for operation at room temperature.

Your startup circuit should have a minimal influence during normal operation ($V_{BG} \approx 1.205$ V), but prevent the undesired operating point effectively.

Instructions for the testbench can be found in moodle.