# AICD Lab - Troubleshooting Document

## General

### 1. First step when facing any error

Most of the errors / warnings which are blocking your progress or troubling you in your workflow are usually listed either

- In the main Virtuoso window
- Or the Terminal window from which you started Cadence.

So, whenever you are in a state of difficulty, the first thing to check would be the above-mentioned windows to see what kinds of errors/warnings are listed.

### 2. Exiting from Virtuoso – Locked Files

It is important to properly close the program as failure to do so would result in files being locked by the session in which it was open previously. This would mean that when you start Cadence the next time, you might not be able to open certain files for Editing.

To overcome this, close Cadence as follows:

- Save all open schematics/ layouts/ ADE Explorer states.
- Go to the main Virtuoso window and then: File → Close Data → All → OK. Now you can see in the main Virtuoso window the list of all files which have been closed and purged from memory. (Refer **Fig. 1**).

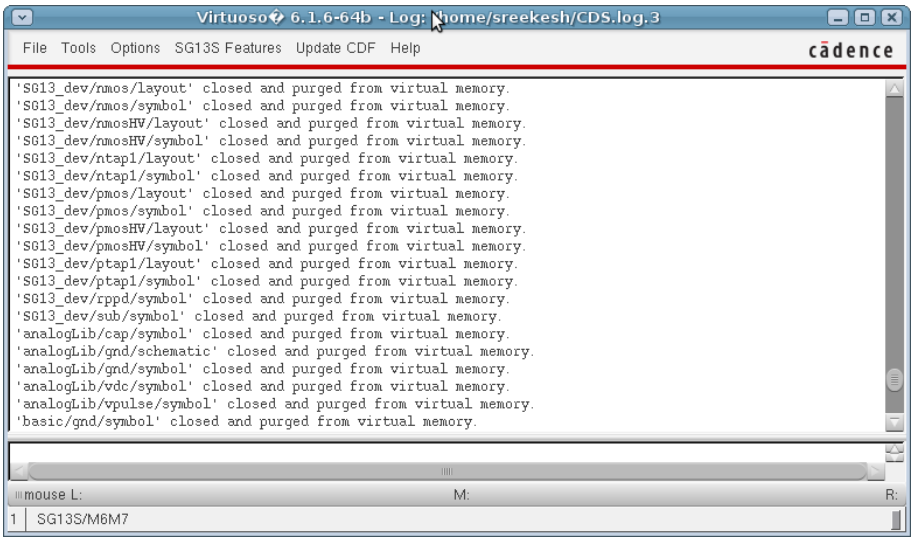


**Fig. 1 – Close and purge**

- Now you are ready to exit the program, File → Exit.

If you have already locked files in your library, you can unlock them by deleting all *.cdslck* files in the corresponding folder *aic##/AICD_lab_project/vir/library/…*

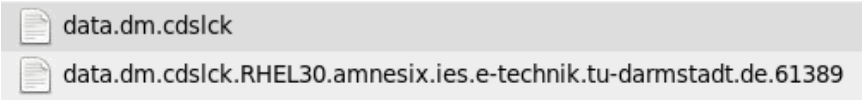


**Fig. 2 – .cdslck files**

## 3. Disk Quota Exceeded Error:

At the start of the lab each group is provided a disk quota of 1.6 GB (or 2 GB). This should be sufficient for the length of the lab if the disk space is managed carefully. However, if you do not manage the disk utilization, you might end up getting disk quota exceeded error (**Fig. 2**).

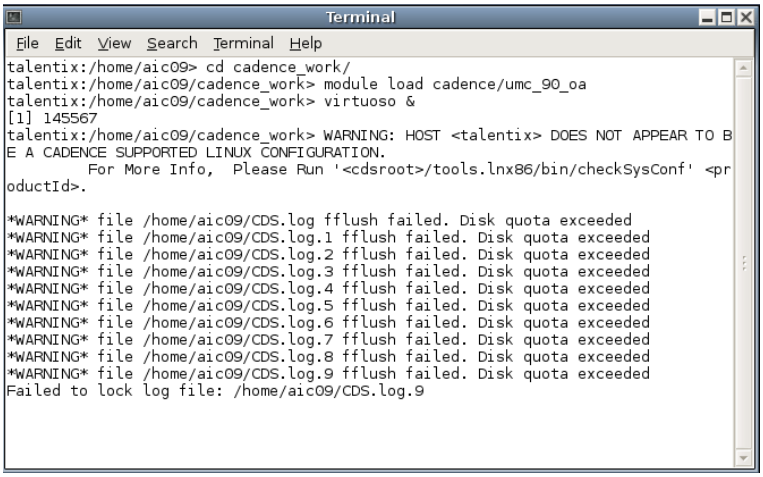


**Fig. 3 – Disk quota exceeded error**

Steps to manage the disk quota are mentioned below:

a) In a terminal window, you could use the 'quota' command to check your available and used up disk space.

b) Clear up old unused simulation data in folder: */home/aic##/simulation* to make space. Identify the simulation data that you do not need anymore and delete those alone.

c) Limit the data that is saved when running a simulation.

- Open the ADE Explorer and go to Outputs → Save All.
- Set up the form as in **Fig. 3**. This setup reduces the space required for each simulation drastically.

d) The Corner as well as the Monte Carlo Simulation for noise need a large amount of disk space. You should not simulate the noise in your Corner and Monte Carlo Simulation, it is also not necessary.

e) Another possibility to save disk space and to reduce simulation time is to reduce simulation ranges. For example, you can reduce the stop time in the transient analysis, so that only the absolute necessary time for the Slew Rate and the Settling Time Simulation is covered (e.g. one period of the signal). Also, the Frequency range in the AC/Noise Simulation can be reduced to cover only the interesting parts (e.g. noise range: 1kHz to 1MHz).

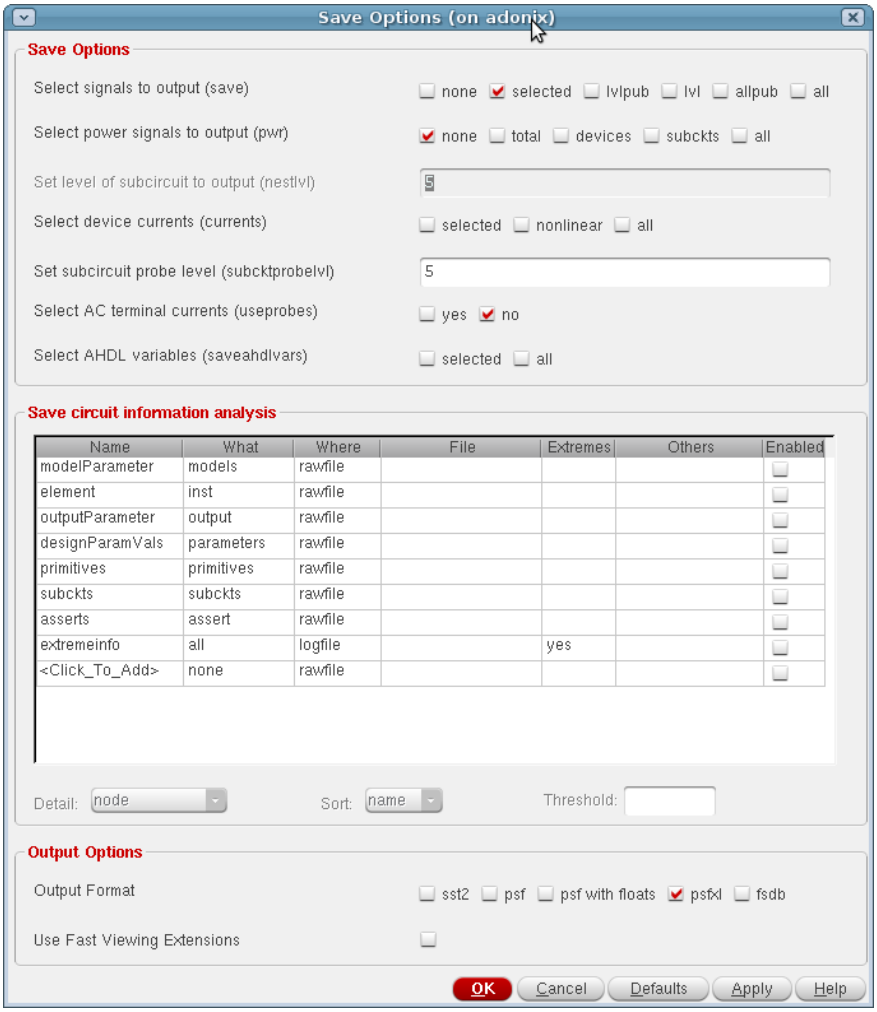


**Fig. 4 – Save Options**

## 4. Library name changing

If you wish to change a library name it is important to use the Cadence Library manager therefor. Do not change a name manually in the folder, this will lead to problems with your library files. To change the library name:

- Open the Library Manager
- right click on the library to rename
- click on rename and enter the new name

# Schematic

1. No Value from Calculator Formula

   If you get no results from your formula, there is often a problem with an expression in the formula. Check the following points:

   - check if the brackets in the formula are set correctly
   - check if you have used the nodes in the schematic for currents and the connections (lines) for voltages
   - check if you have used the correct expression for the voltages (v) and currents (i)
     - *vt* and *it* for Transient Analysis (Slew Rate, Settling Time)
     - *vf* and *if* for AC Analysis (DC Gain, GBW, …)
     - *vdc* and *idc* for DC Analysis (Power Dissipation)
     - *vs* and *is* for DC Sweep (Offset)

2. The Settling Time is exceedingly high

   A common reason for a high Settling Time is that you forgot to subtract the value you get from the *settlingTime()* function from the input signal rise timepoint. The *settlingTime()* function returns only the timepoint where the signal is settled, not the final value. In the example in **Fig. 5**, the *settlingTime()* function returns 1.01305us as result for the positive settling time. To get the settling Time, you can subtract the timepoint where the rising input signal begin to rise (1us) for example. The final settling time is then 13.05 ns.

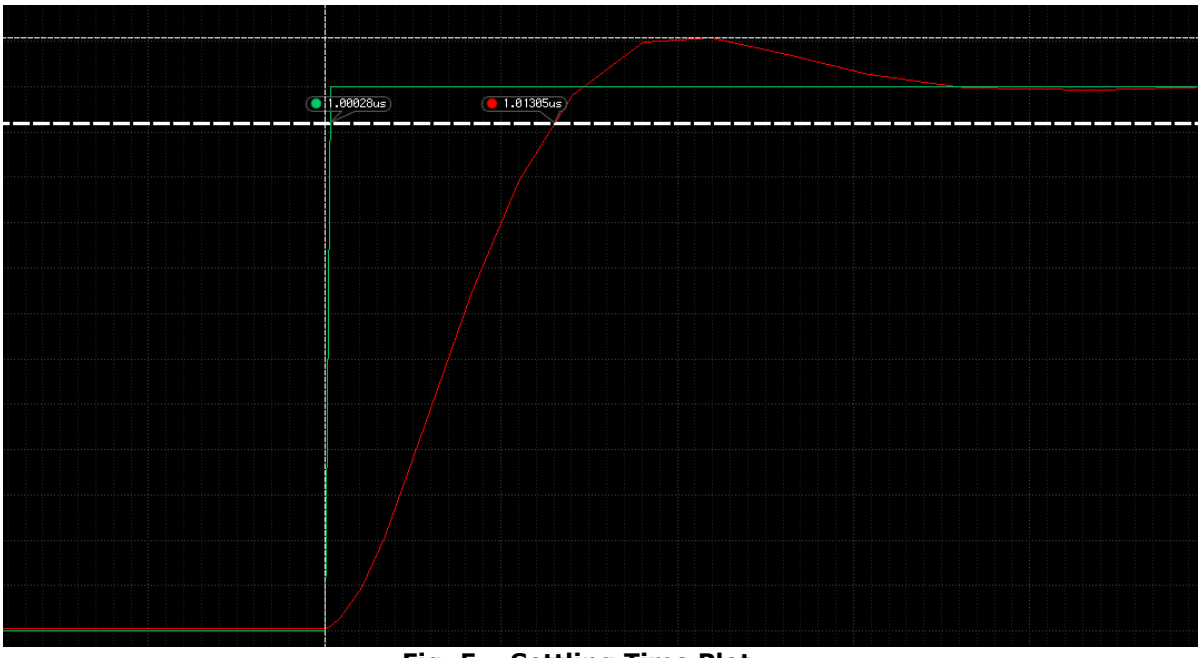


**Fig. 5 – Settling Time Plot**

3. The Noise is exceptionally low

A realistic noise of your OPAMP should be between 20nV/sqrt(Hz) and 100nV/sqrt(Hz) at 20kHz. If your noise measurement results are explicit lower, you should check the following points:

- The Start Frequency range should not be 0Hz in the noise test setup.
- Check if you have selected the correct Output nodes and input voltage Source in the noise test setup.
- Ensure you have chosen the correct unit in the direct plot window (Fig. 6) after simulation.


**Fig. 6 – Noise Direct Plot**

4. Offset is high, or does not change when changing circuit parameters

Your measured offset value is depending on the step size of the DC sweep, so the higher the step size the more unprecise it is. To ensure your offset measurement is precise you should choose a small sweep range (e.g. -20mV to 20mV), this leads to a small step size if the sweep type is set to automatic. You can also set a step size by yourself to ensure that you get a precise result (**Fig. 7**).

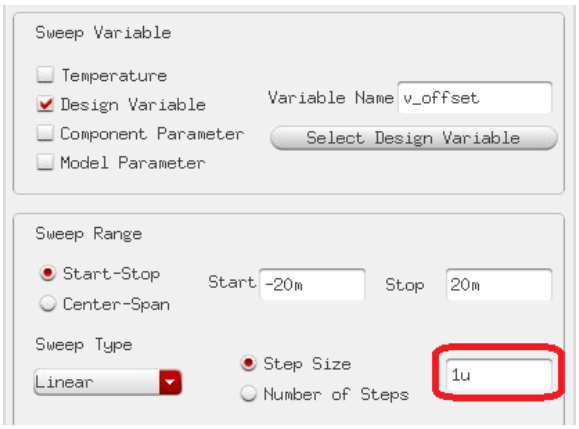


**Fig. 7 – DC Analysis Setup**

## 5. Simulation Error in the Corner or Monte Carlo Simulation

The most common problems in the Simulations occur if a model library is missing or embedded incorrectly. This problem holds for the Corner as well as for the Monte Carlo simulation. An example error message for the Corner simulation is shown in **Fig. 8**. In this example the library for the MIMCAP is missing. An example for a Monte Carlo simulation error where a library is missing, is shown in **Fig. 9**.

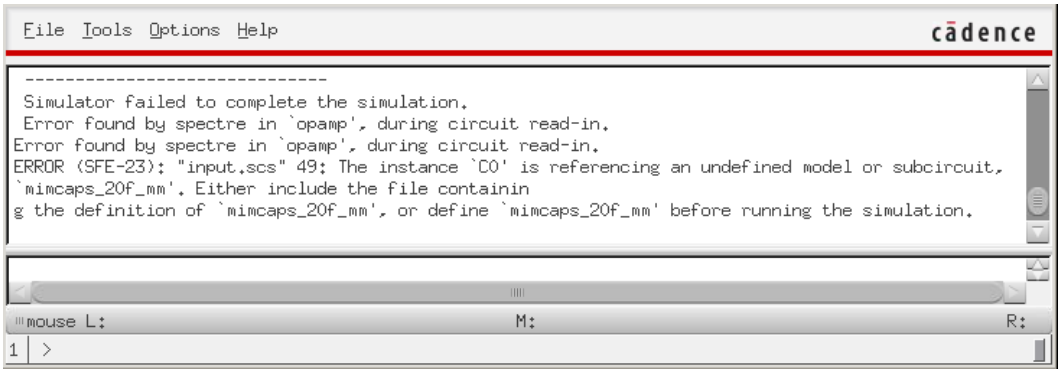


**Fig. 8 – Error Message Corner Simulation**

If you get an error message like in **Fig. 8** or **Fig. 9**, check your Corner respectively Monte Carlo setup. Ensure the model libraries are correct. Therefor check if you are using the correct model libraries for each group of components that are used in the corresponding schematic. Only the components from the *analogLib* do not need a model file for the simulations. Also check the path of the model libraries if it is correct.

You can find a description of the model libraries in the *Corner_Simulation.pdf* and the *Monte_Carlo_Simulation.pdf* documents.

If you get "evaluation error" on corner simulation window, check your model files again and find out if any additional unwanted citation mark has occurred like in Fig. 10. If it does, delete it and click ok again.

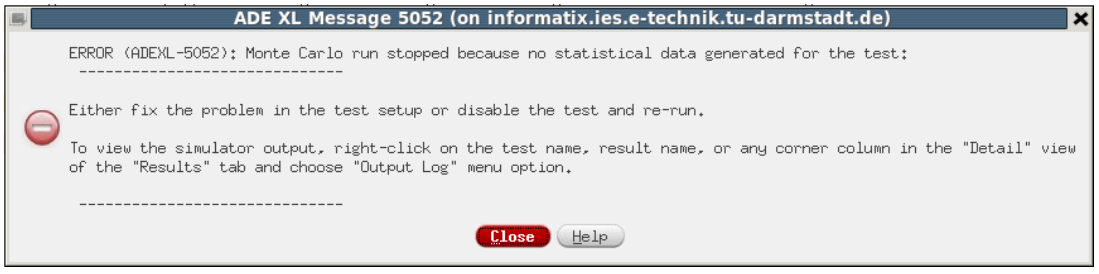


**Fig. 9 – Error Message Monte Carlo Simulation**

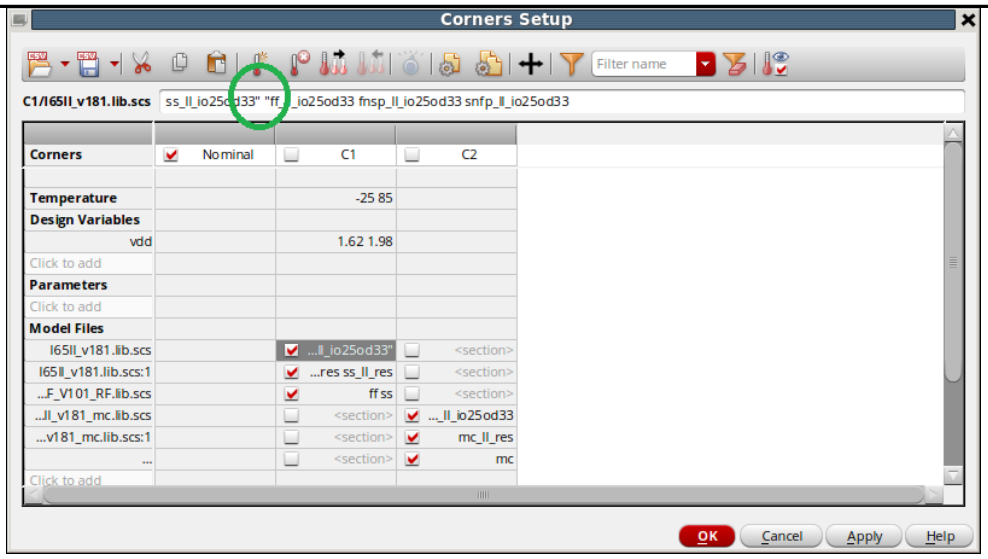


**Fig. 10 – Unwanted citation mark(inside of green circle)**

## 6. Bad Corner or Monte Carlo Simulation Results for OPAMP

If you are getting bad Corner respectively Monte Carlo Simulation results for Gain, GBW and Phase Margin, you may forget to setup a stability analysis for the parameters. If you are using the AC analysis for the parameters you will have at least high deviations, because the change of the OPAMP offset is not considered. A description how to setup the stability analysis is described in the *Monte_Carlo_Simulation.pdf* in section 7 "New Testbench for AC Simulation".

## 7. Resistor Selection

For most cases you should use the RNHR_LL resistor, except for extremely low resistances. The Bulk of the Resistor is connected to VDD.

## 8. Bad Simulation Results for the BGR

A common mistake that leads to bad simulation results for the BGR, is a missing start up circuit. Without a startup circuit, the BGR can not work and the simulation results can be bad.

## 9. PGA Testbench Setup

For the Gain and Bandwidth PGA Testbench you can use an AC simulation like in the OPAMP Testbench. Do not use the Stability analysis for your PGA Testbench, this will not work.

## 10. The Simulation of the ADC does not work

If you have Problems with the transient analysis of your ADC and you get an error message like in Fig. 11, you forgot to use a config file for your testbench. How to setup the config file for the ADC is described in the *ADC_Matlab_testbench.pdf*.

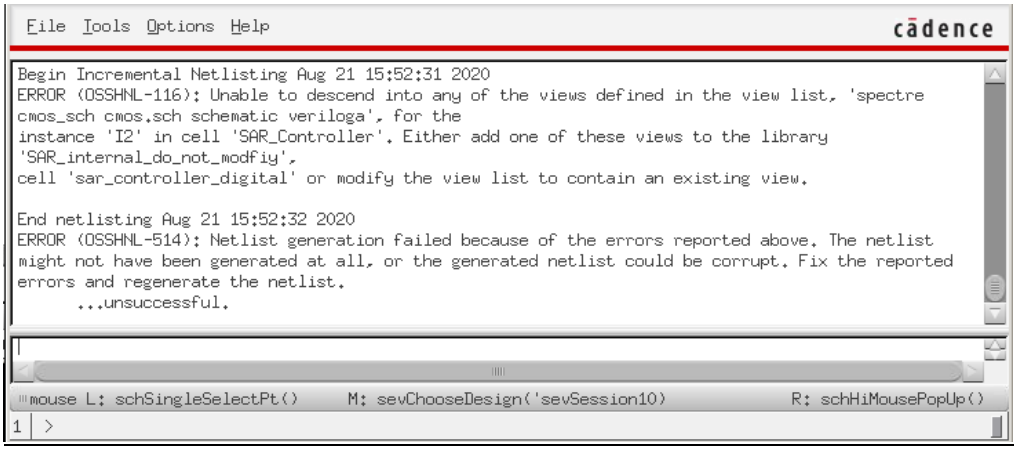


**Fig. 11 – Error Message ADC Transient Simulation**

# Layout

## 1. Connections of BJT, MIMCAP and MOMCAP

The connections of the BJT are shown in **Fig. 12**. The BJT can simply connected by connecting the corresponding Metal layers.

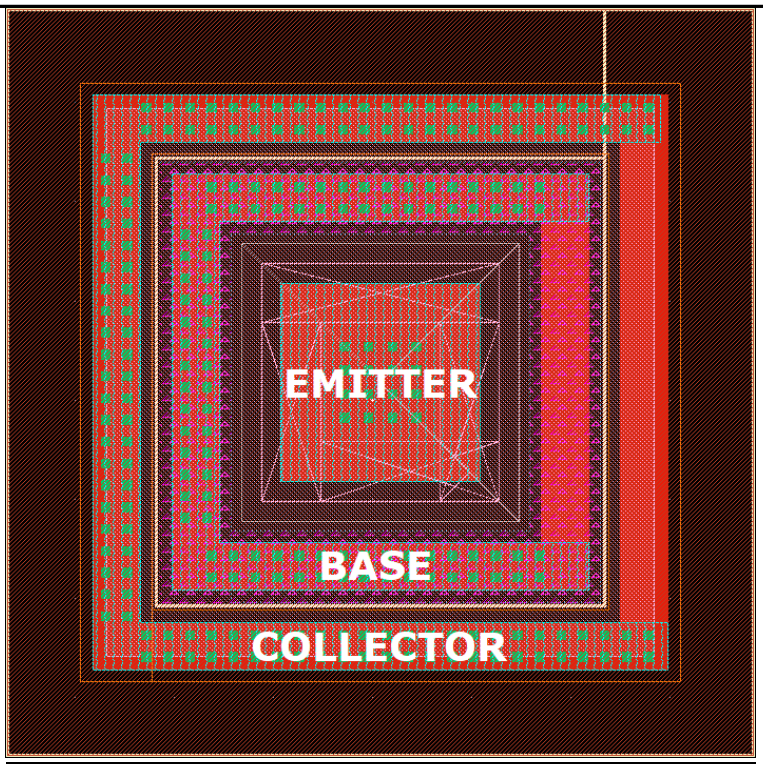


**Fig. 12 – BJT Connections**

For the connection of the MIMCAP, the ME7 layer is used. The connection is shown in **Fig. 13**. It can be helpful to set all layers except the Metal layers invisible for connecting the MIMCAP.

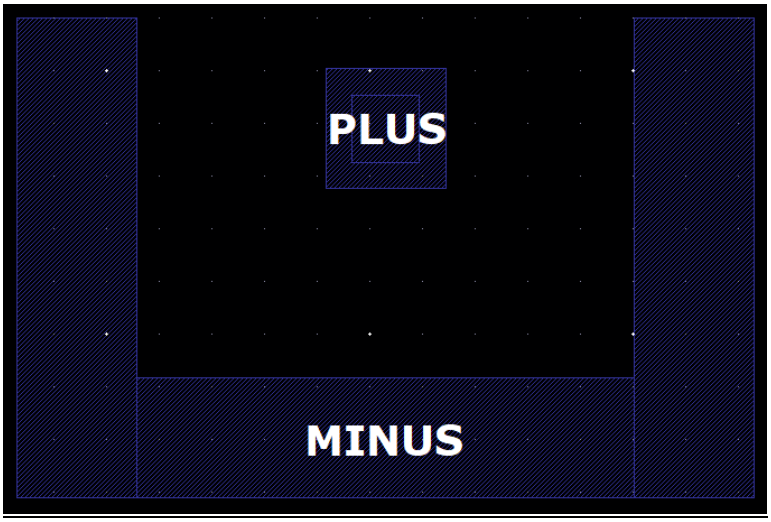


**Fig. 13 – MIMCAP Connection**

In **Fig. 14** the connections of the MOMCAP is shown. The MOMCAP uses ME1 up to ME6, depending on your configuration. The connection of the poles can be done with any of the used metal layer.

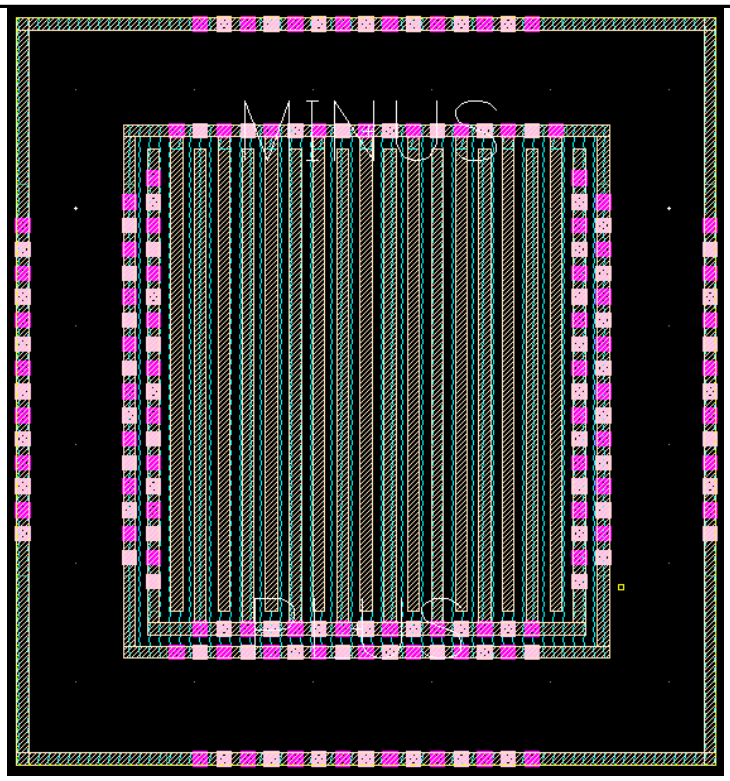

**Fig. 14 – MOMCAP Connection**

## 2. Wrong layer for pin names

A common error in the layout is the use of a wrong layer for the pin names. Typical error messages are the following:

- **DRC Error**: NWEL is connected to nodes other than VDD or VCC (Example for wrong pin layer for VDD)
- **LVS Error**: Pin error

If you have similar error messages in your layout, check the used layer of your pin names. Therefor select a pin name and open its properties (press 'q'). The window that is shown in Fig. 15 should appear. There you should check the used layer. The correct layer should be "MEX | drw", where X is replaced by the used metal layer (ME1, ME2, ME3, ME4, … )

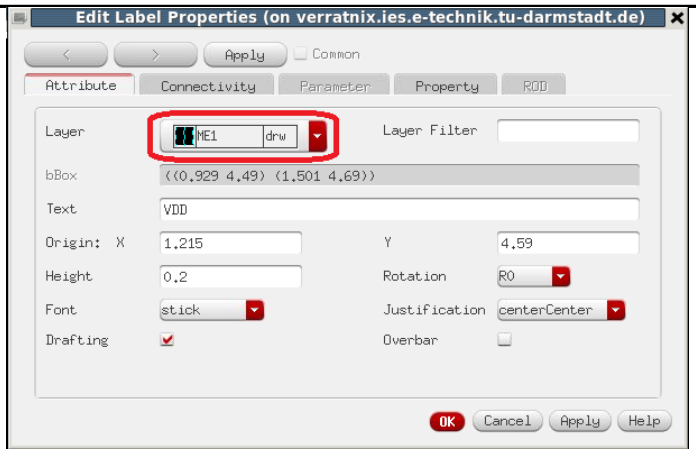


**Fig. 15 – Edit Label Properties**

3. The AV Extraction does not work (The Quantus QRC run "lvs" failed)

The most common reason why the AV Extraction fails is that the Ref Node in the settings is not set correctly. To setup the Ref Node, go to *Assura -> Run Quantus QRC -> Extraction* (**Fig. 16**). There you should enter the exact name of your lowest potential that you have used in the corresponding schematic (e.g. GND, VSS).
If you have already an av_extracted file and you want to refresh it, delete the old one first to avoid problems.

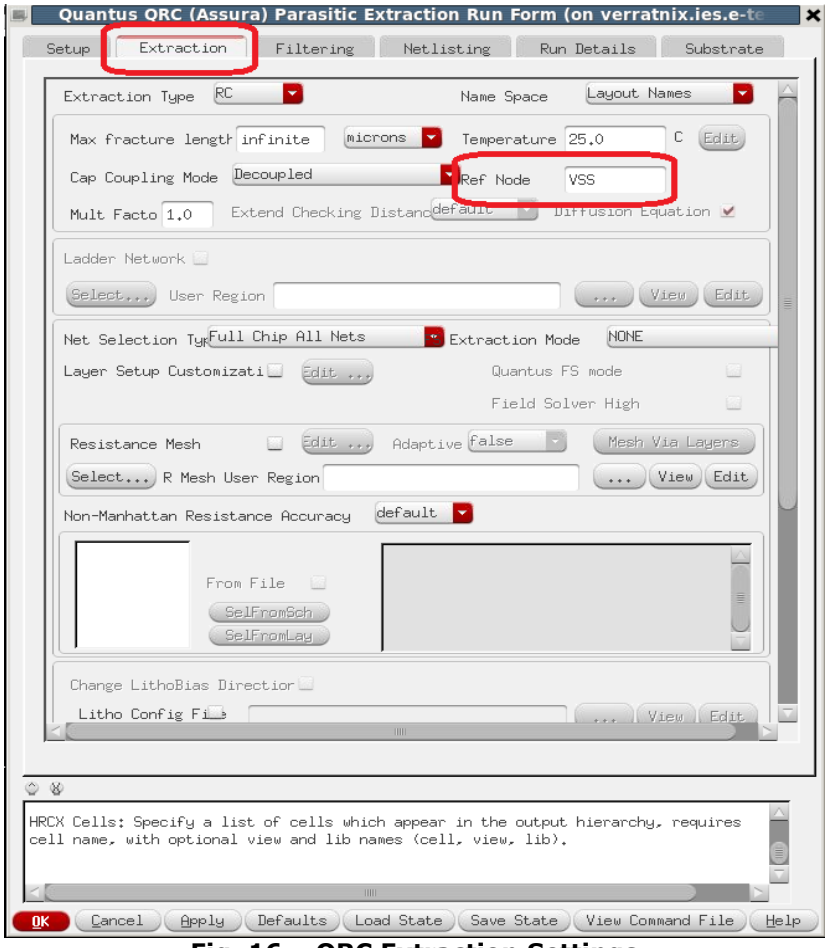


**Fig. 16 – QRC Extraction Settings**

4. SYNTAX ERROR in the LVS

Sometimes it can happen that you can get a SYNTAX Error in the LVS. This probably happens through some temporary files. If you get this error message, try to close Cadence completely and try the LVS again. Also, it might be helpful if you change the server. It might need more than one restart of Cadence to overcome this type of error.