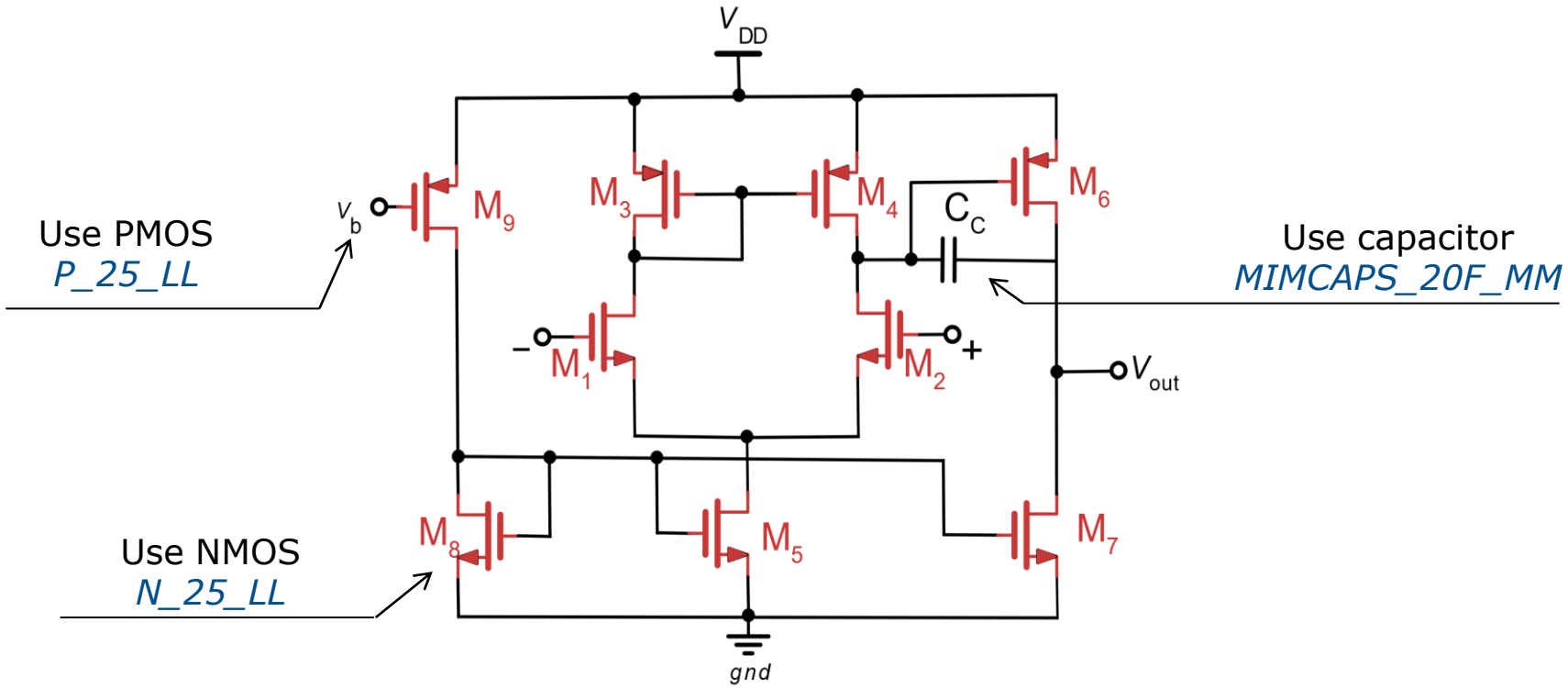
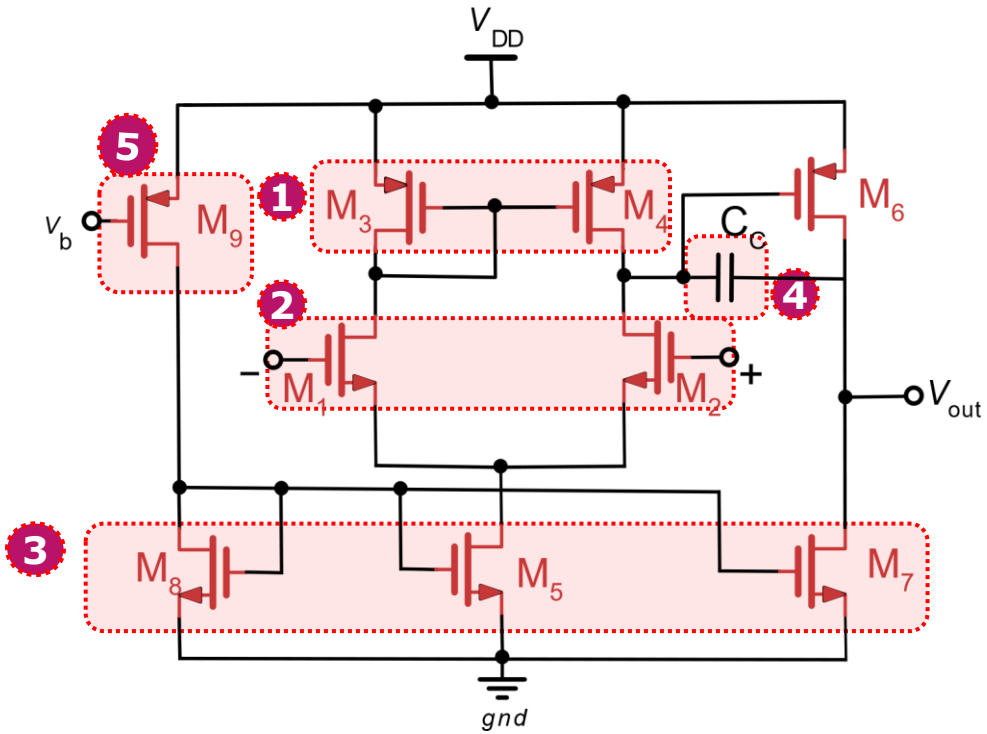
Two-Stage Miller OPAMP

- A two-stage Miller OPAMP is used here.
  - Note: You also have to design a biasing circuit for V_b!
- If you have prior design experience and would like to try other amplifier architectures, you could do so.



Two-Stage Miller OPAMP



[1]Diode Connected Active Load

[2]Differential Input Pair

[3]Tail Current Sources

[4]Compensation Capacitor

[5]Bias Voltage

OPAMP Specifications

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Parameter	Abbr.	Unit	Specification
DC Gain	Av	[dB]	> 50
Gain Bandwidth	GBW	[MHz]	≥ 20
Phase Margin	PM	[°]	≥ 55
Common-Mode Rejection Ratio	CMRR	[dB]	> 60
Slew Rate (+ve, -ve)	SR+ , SR-	[V/µs]	≥ 15 , 15
Settling Time @ 5 % error (high, low)	ST_{high}, ST_{low}	[ns]	≤ 500 , 500
Input Common-Mode Range	ICMR	[V]	0.5 … 1.3
Output Voltage Swing	-	[V]	0.3 … 1.5
Input Offset Voltage	-	[mV]	≤ 5
Input Referred Noise @ 20 kHz	$V_{ni,rms}$	[nV/$\sqrt{Hz}$]	≤ 55
Power Dissipation	P_{DC}	[mW]	≤ 0.6
Load Capacitance	C_L	[pF]	≥ 2
Supply Voltage	V_{DD}	[V]	1.8

**The given specifications are absolute minimum for typical corner post-layout simulations.*

Your design will be evaluated based on:

- How optimized it is.
- How power & area efficient it is.
- How well the specifications for Corner and Monte-Carlo analysis are met.

OPAMP Design

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Design procedure for the OPAMP:

1. Initial design using hand calculations.
   - Please understand the operating principles of the OPAMP and the transistors before attempting to design the OPAMP. Otherwise, you will not be able to make good design decisions.
   - A provided Matlab Script will help you with the initial calculations. It is based on simplified equations and uses look-up tables for the transistor sizing.

2. Adapted/optimized design using Cadence Virtuoso.
   - Setup your testbench to simulate all relevant parameters.
   - Optimize your design based on simulation with Cadence Virtuoso.
   - After achieving good performance in the nominal case, check and fine-tune your design using Corner and Monte-Carlos Analysis.

OPAMP Design

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3. Layout creation using Cadence Virtuoso.
   - Your layout must not have DRC violations or LVS errors.

4. Post-Layout Simulation
   - Extract the layout to include the parasitic effects. Simulate your extracted design and make sure, that your design still meets the specifications.

➢ *OPAMP_Design&Simulation.pdf* for some hints on the design of the OPAMP and on how to do its simulations!