Digital Logic Systems

Sequential Logic

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ALKÜ

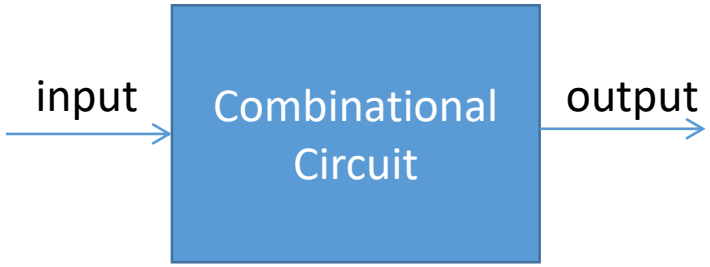
Last Week

- Completed Combinational Circuits
  - Decoder
  - Encoder
  - Multiplexer

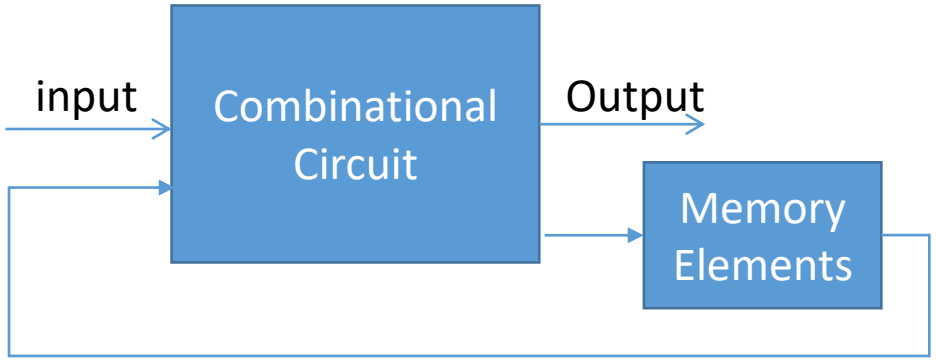
- Able to design/analyze combinational circuits with any combination of logic gates, decoders, multiplexers.
- Can design decoders / multiplexers by combining decoders / multiplexers in various sizes.

Digital Logic Systems

- Digital Logic Design: Combinational Circuits

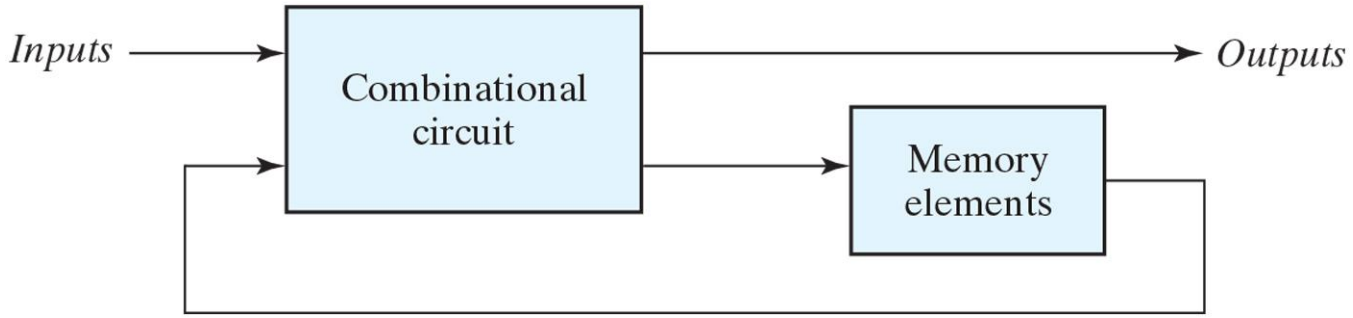


- Digital Logic Systems: Sequential Circuits



Synchronous Sequential Logic

Block Diagram of Sequential Circuit



- Memory Elements
  - Store binary data.
  - This data is referred as the current state of the flip-flop.
- Sequential Circuit
  - Determines the output using input and the current state.
  - Input and the current state determine the next state.

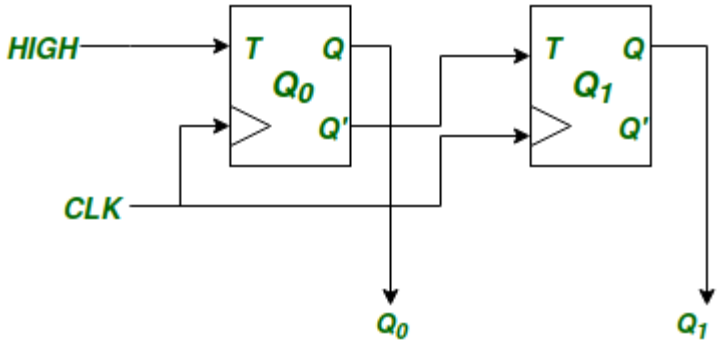
Sequential Circuit

- is defined by?
  - Time
    - input
    - output
    - state

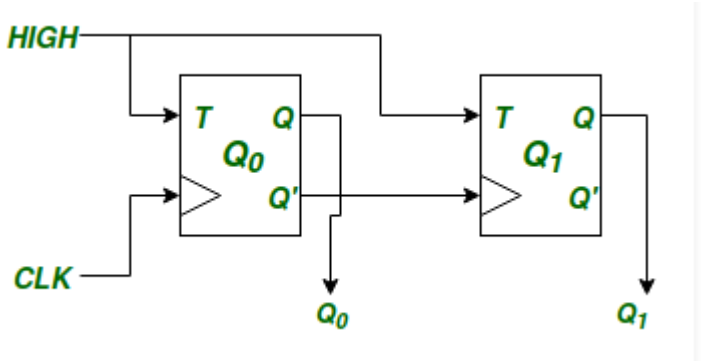
- Types:
  - **Synchronous sequential Circuit**: A *synchronous* sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instant s of time.
  - **Asynchronous sequential Circuit:** The behavior of an async*hronous* sequential circuit depends upon the input signals at any instant of time *and* the order in which the inputs change.

Types of Sequential Circuits

- Synchronous Sequential Circuit



- Asynchronous Sequential Circuit



Synchronous Sequential Circuit

- Employs signals that affect the storage elements at only discrete instant of time.
- Synchronization is achieved by a timing device called a *clock* generator which provides a clock signal having the form of a periodic train of *clock pulses.*
- The clock pulses are distributed throughout the system in such a way that storage elements are affected only with the arrival of each pulse.
- The clock pulses determine *when* computational activity will occur
- Other signals (external inputs and otherwise) determine *what* changes will

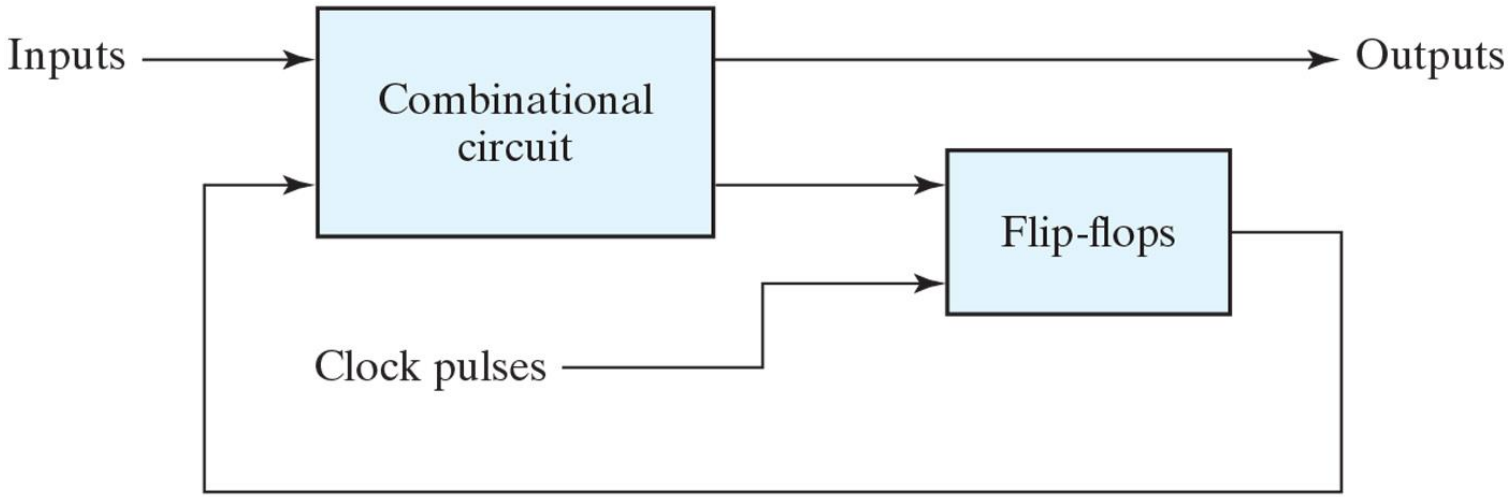
take place affecting the storage elements and the outputs

Memory Elements

- Flip-flop: A flip-flop is a binary storage device capable of storing one bit of information.
- Flip-flop has two outputs.
  - Bit which determines the state of the flip-flop.
  - Complement of the bit representing the state of the flip-flop.

- Depending on the number of bits represented by the sequential circuit, the number of flip-flops is determined.

Synchronous Sequential Circuit



(a) Block diagram

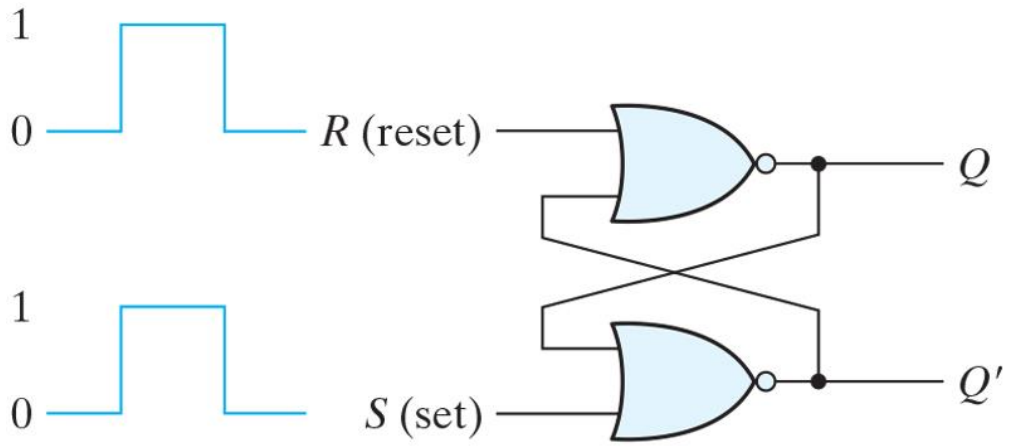
(b) Timing diagram of clock pulses

Flip-Flops

- A flip-flop can hold its state until an input signal is asserted to change its state.
- Types of Flip-flops vary:
  - By the number of input signals.
  - How the inputs effect the binary state of the flip-flop.

A Simple Flip-flop Circuit

x	y	x NOR y
0	0	1
0	1	0
1	0	0
1	1	0



(a) Logic diagram

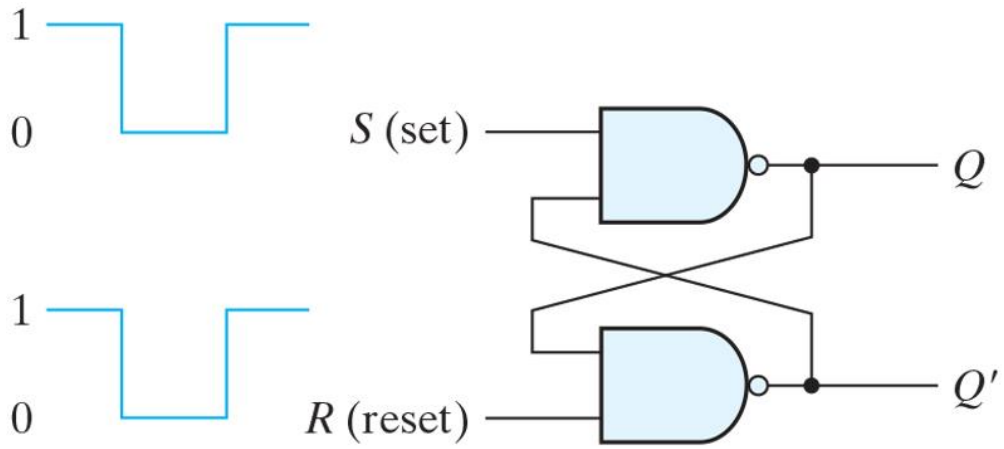
S	R	Q	Q′	
1	0	1	0	
0	0			(after $S = 1, R = 0$)
0	1			
0	0			(after $S = 0, R = 1$)
1	1			(forbidden)

(b) Function table

Q state of the flip-flop, Q' complement of Q.
Q=1, Q'=0 set
Q=0, Q'=1 reset

Flip-Flop with NAND Gates

x	y	x NAND y
0	0	1
0	1	1
1	0	1
1	1	0



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1			(after $S = 1, R = 0$)
0	1			
1	1			(after $S = 0, R = 1$)
0	0			(forbidden)

(b) Function table

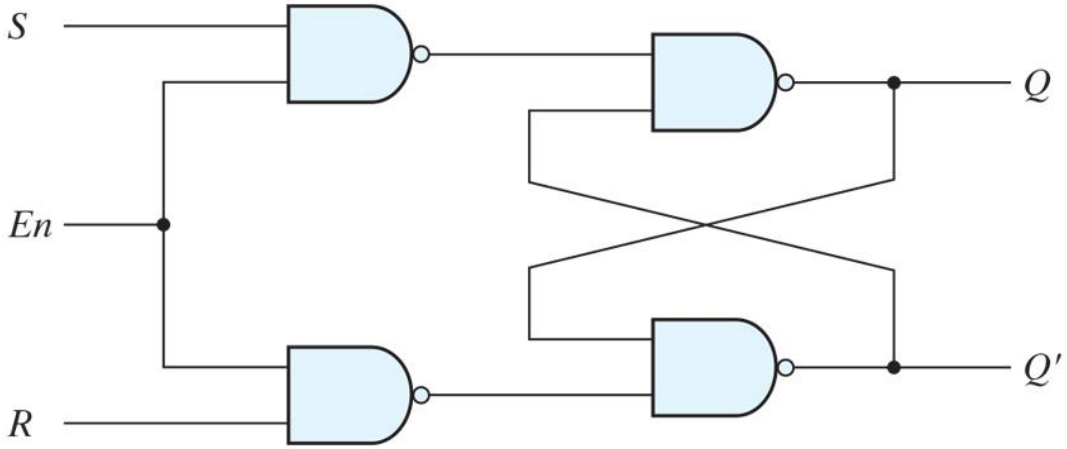
RS Flip-Flop

	00	01	11	10
0			X	1
1	1		X	1

Q(t+1)=S + R'Q
SR = 0
Characteristic Equation

Q	S	R	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Characteristic Table



(a) Logic diagram

(b) Function table

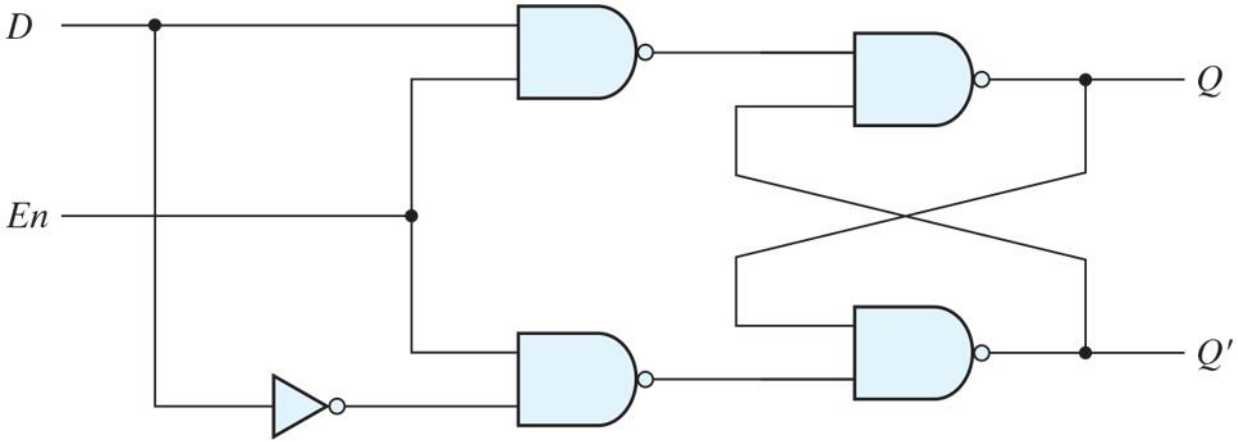
D Flip-Flop

Q	D	Q(t+1)
0	0	?
0	1	
1	0	
1	1	

Characteristic Table

	0	1
0		1
1		1

Q(t+1)=D
Characteristic Equation

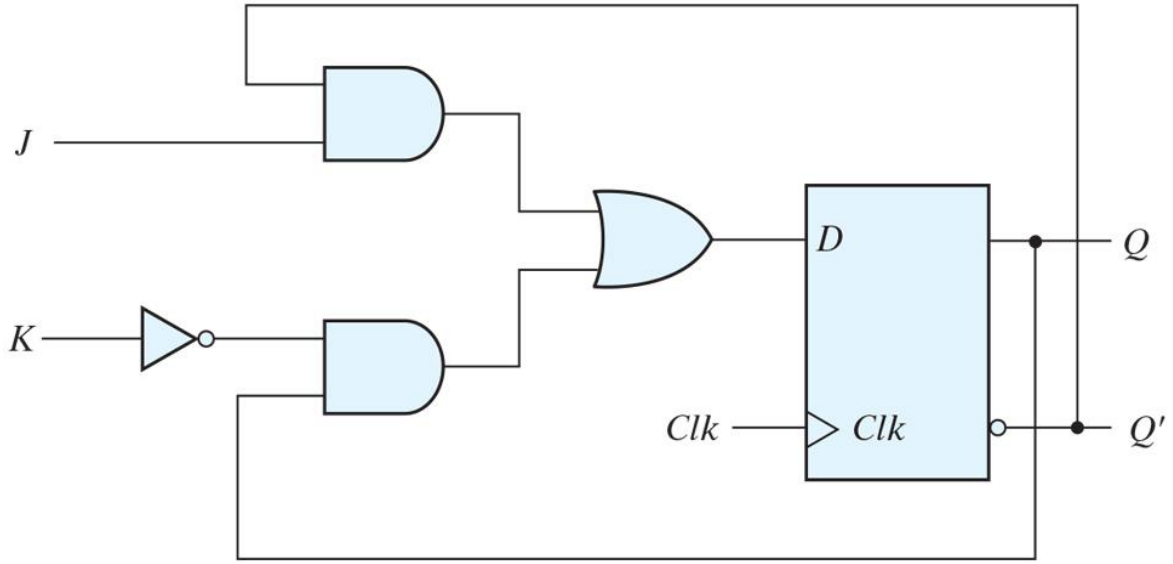


(a) Logic diagram

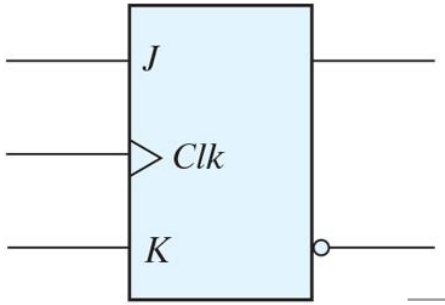
?

(b) Function table

J-K Flip-Flop



(a) Circuit diagram



(b) Graphic symbol

	00	01	11	10
0			1	1
1	1			1

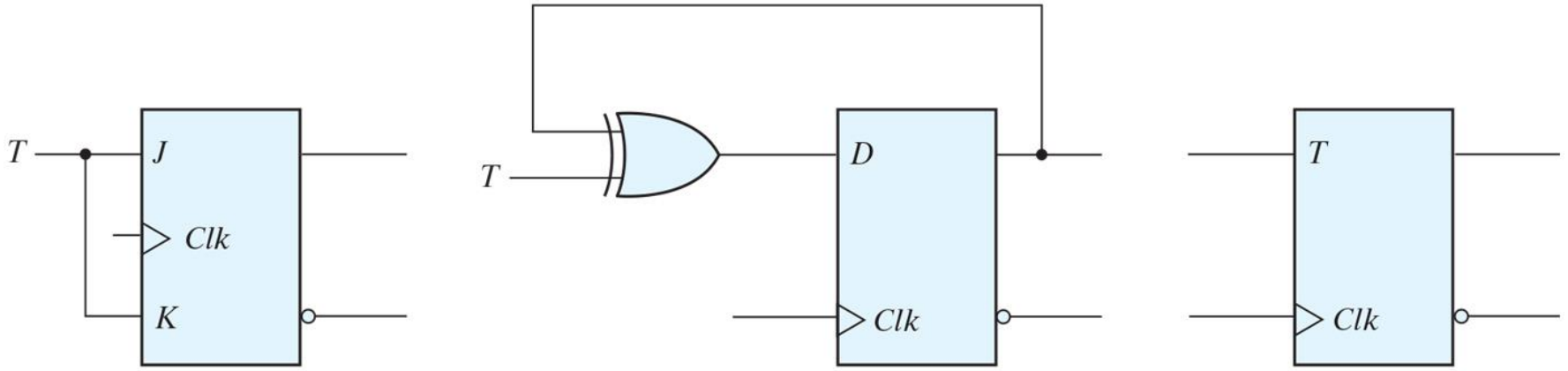
$Q(t+1)=JQ'+K'Q$

Characteristic Equation

Q	J	K	Q(t+1)
0	0	0	?
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Characteristic Table

T Flip-Flop



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

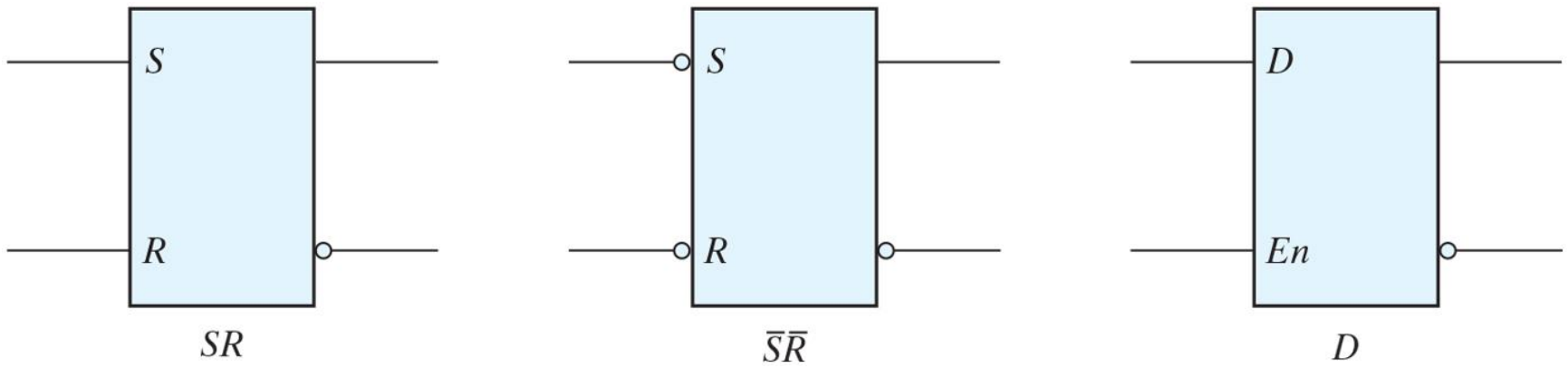
Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Table

	0	1
0		1
1	1	

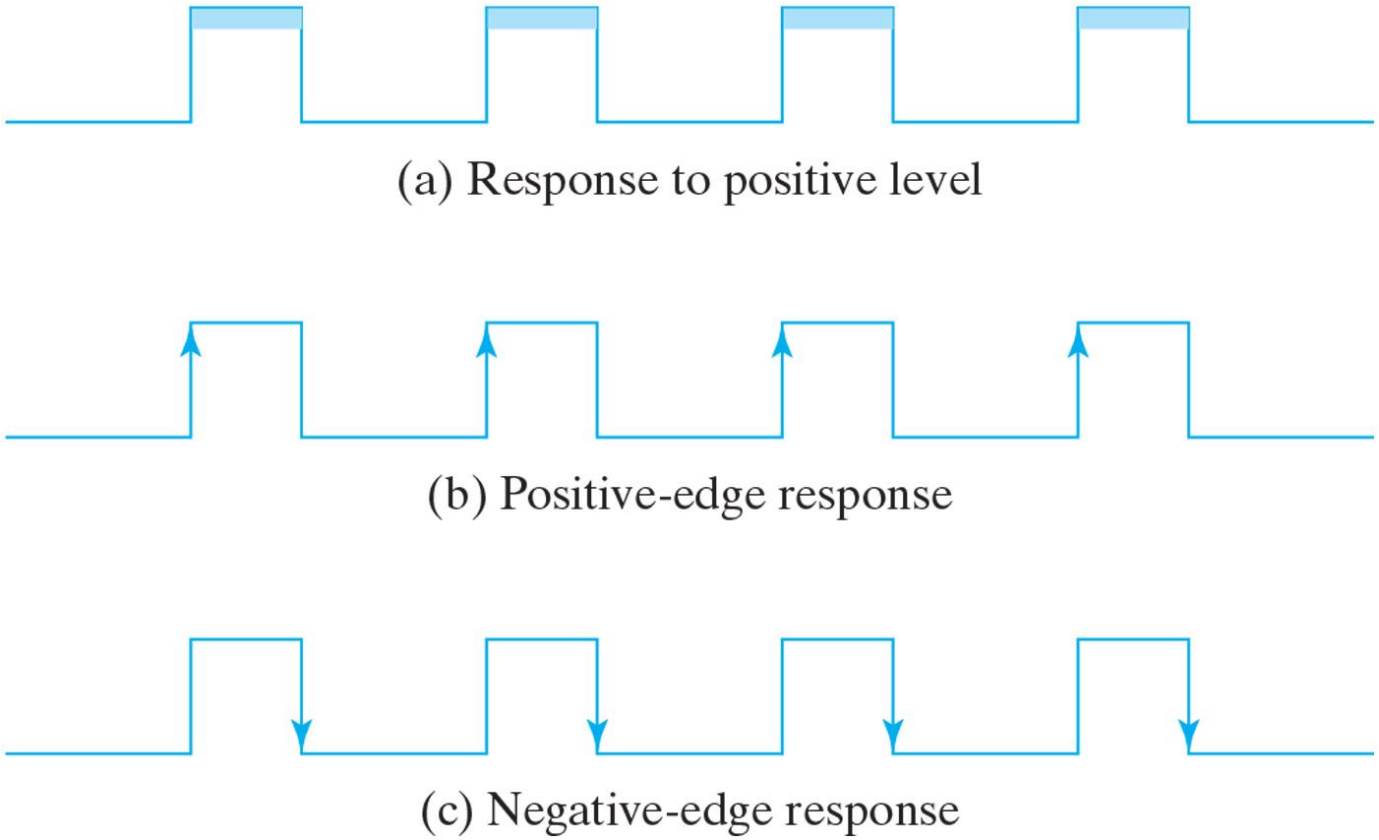
Q(t+1)=TQ'+T'Q
Characteristic Equation

Graphical Symbols of Flip-Flops



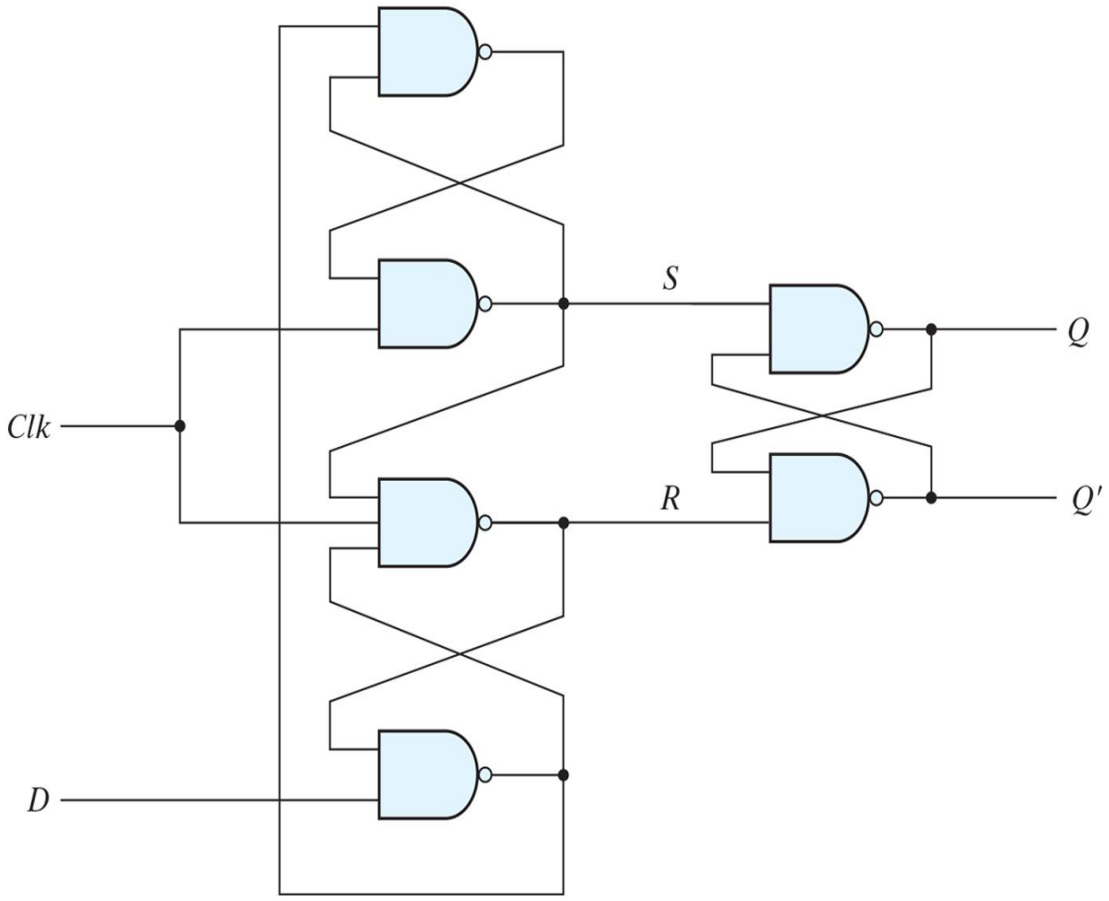
Flip-Flop and Clock Signal

- If flip-flops respond to a level of clock, indetermined conditions may arise.
  - If the flip-flop outputs change while the output of the combinational circuit which are fed as input to flip flops then indetermined condition arises.
  - Solution: Flip-flops respond to clock transitions..

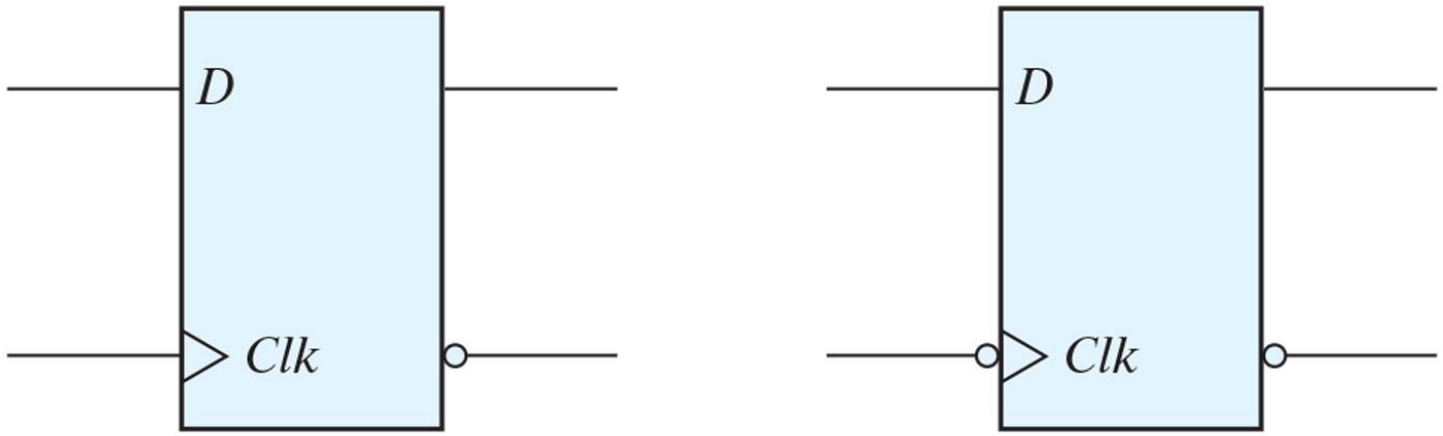


Positive Edge Triggered D Flip-Flop

- For the third flip-flop
  - S=0, R=1 → Q=1
  - S=1, R=0 →Q=0
- 4 conditions:
  - CP=0, D=0 →
    - R=1, S=1 → Forbidden
  - CP=0, D=1 →
    - R=1, S=1 → Forbidden
  - CP=1, D=0 →
    - R=0, S=1 → Q=0
  - CP=1, D=1 →
    - R=1, S=0 → Q=1
- Summary: When the input CLK signal changes make a positive transition, value of D is transferred to Q.
- When CP is always 1 changes in D are not transferred to Q.



Graphical Representation of Edge Triggered D Flip-Flops



(a) Positive-edge (b) Negative-edge

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

- Questions?

References

- Morris Mano, Digital Design