Digital Logic Systems – Synchronous Sequential Logic - III

Assist. Prof. Özge ÖZTİMUR KARADAĞ

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Previously..

- Analysis of Synchronous Sequential Circuit
  - Circuit → State Table / Diagram
    - State Reduction
    - State Asignment
    - Flip-flop excitation tables
- Design of Synchronous Sequential Circuit
  - Design of a circuit whose behaviour is described by text..
  - Design of a circuit whose state diagram is given..
  - An example with JK Flip-flops.

Example

- Given the state table, design the corresponding sequential circuit using D flip-flops:
- Flip-flop inputs as sum of products:
  - $DA(A, B, x) = \sum(2,4,5,6)$

	00	01	11	10
0				1
1	1	1		1

$= AB' + Bx'$

  - $DB(A, B, x) = \sum(1,3,5,6)$

	00	01	11	10
0		1	1	
1		1		1

$= A'x + B'x + ABx'$

  - $y = \sum(1,5)$

	00	01	11	10
0		1		
1		1		

$= B'x$

Current State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

Design with Unused States

- There will be 2^m possible states with m flip-flops.
- But there can be unused states.
- Unused states are considered as don’t care conditions.

Example

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S	R	Q(t+1)	R
0	0	Q(t)	No chnage
0	1	0	Reset
1	0	1	Set
1	1	?	0

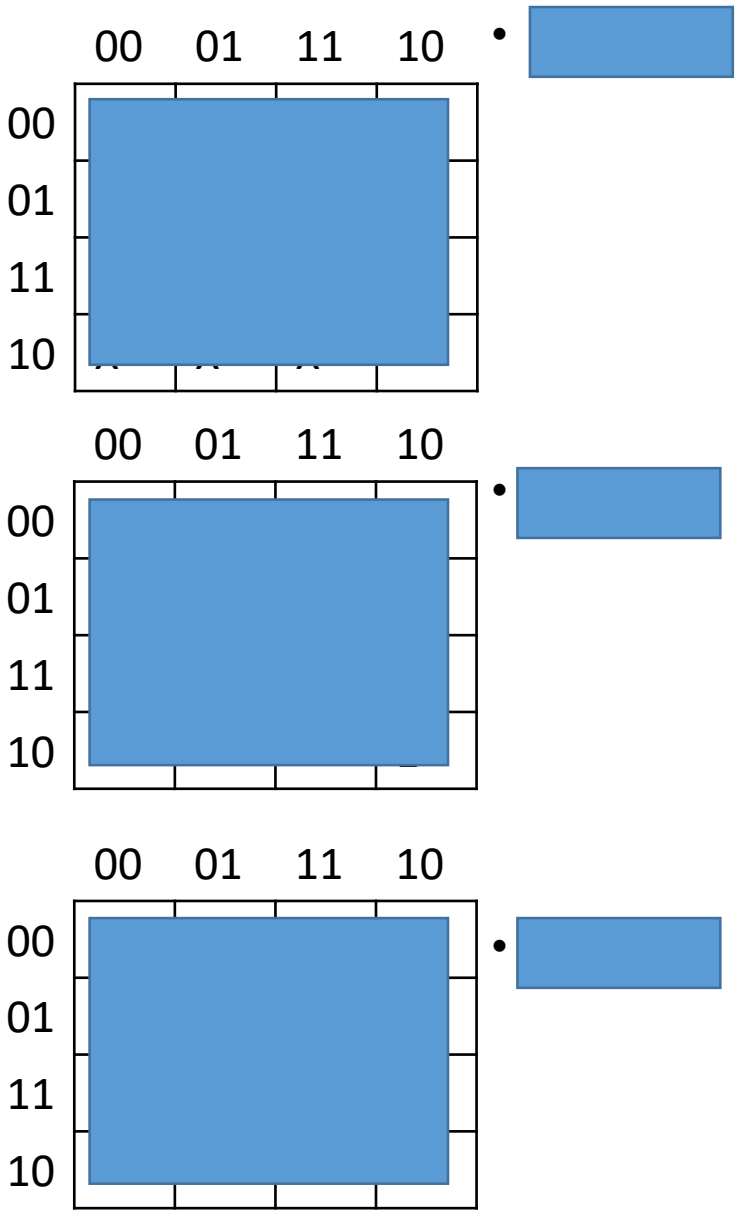
Current State			Input	Next State			Flip-flop Inputs						Output
A	B	C	x	A	B	C	SA	RA	SB	RB	SC	RC	y
0	0	1	0	0	0	1							0
0	0	1	1	0	1	0							0
0	1	0	0	0	1	1							0
0	1	0	1	1	0	0							0
0	1	1	0	0	0	1							0
0	1	1	1	1	0	0							0
1	0	0	0	1	0	1							0
1	0	0	1	1	0	0							1
1	0	1	0	0	0	1							0
1	0	1	1	1	0	0							1

Example…

- Unused States:
  - 000,110,111

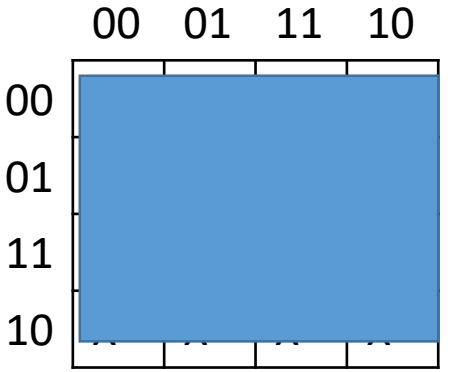
Şimdiki durum			Giriş	Sonraki durum			Flip-flop girişleri						çıkış
A	B	C	x	A	B	C	SA	RA	SB	RB	SC	RC	y
0	0	1	0	0	0	1	0	X	0	X	X	0	0
0	0	1	1	0	1	0	0	X	1	0	0	1	0
0	1	0	0	0	1	1	0	X	X	0	1	0	0
0	1	0	1	1	0	0	1	0	0	1	0	X	0
0	1	1	0	0	0	1	0	X	0	1	X	0	0
0	1	1	1	1	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	1	X	0	0	X	1	0	0
1	0	0	1	1	0	0	X	0	0	X	0	X	1
1	0	1	0	0	0	1	0	1	0	X	X	0	0
1	0	1	1	1	0	0	X	0	0	X	0	1	1

- Combinational Circuit:
  - SA,RA,SB,RB,SC,RC,y

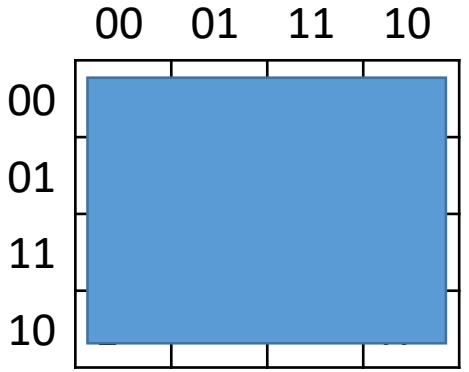


Example…

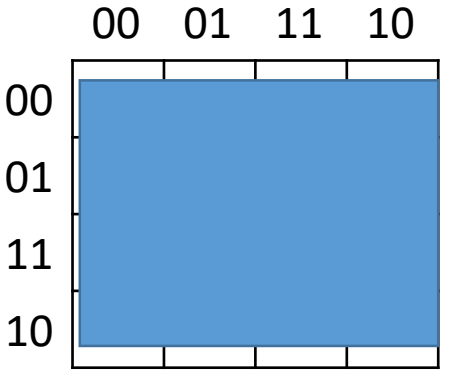
Current State			Input	Next State			Flip-flop inputs						output
A	B	C	x	A	B	C	SA	RA	SB	RB	SC	RC	y
0	0	1	0	0	0	1	0	X	0	X	X	0	0
0	0	1	1	0	1	0	0	X	1	0	0	1	0
0	1	0	0	0	1	1	0	X	X	0	1	0	0
0	1	0	1	1	0	0	1	0	0	1	0	X	0
0	1	1	0	0	0	1	0	X	0	1	X	0	0
0	1	1	1	1	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	1	X	0	0	X	1	0	0
1	0	0	1	1	0	0	X	0	0	X	0	X	1
1	0	1	0	0	0	1	0	1	0	X	X	0	0
1	0	1	1	1	0	0	X	0	0	X	0	1	1



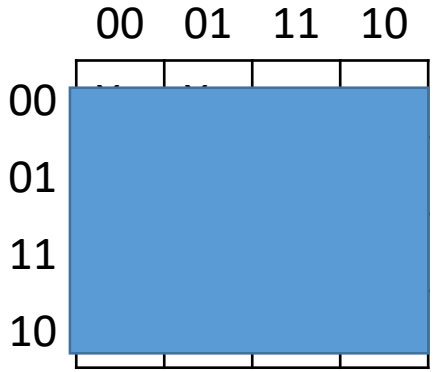
- RB=



SC=



- RC=



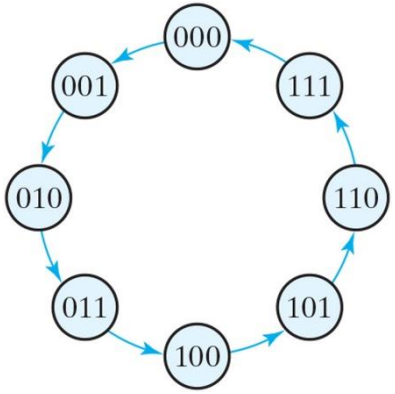
y=

Initial State of Sequential Circuits

- It is not possible to know in advance in which state the circuit will be when the energy in given.
- In general, a reset or set is applied to all flip-flops in the beginning.
- In order to be sure that the circuit is not stuck in some unused state, it is safe to put the circuit in an initial state.

Design of Counters

- A counter is a sequential circuit which goes through previously defined states as input signal is applied.
- State diagram of a 3 bit binary counter:
  - Note that the arrows are not signed with input/output values.

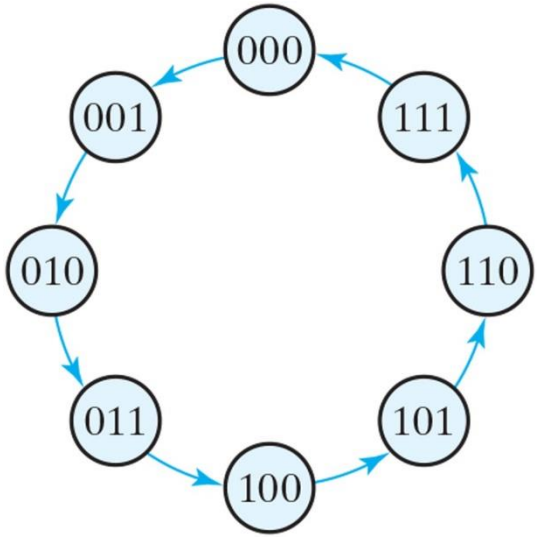


Design of Counter

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

T	Q(t+1)	
0	Q(t)	No change
1	Q'(t)	Complement

- 3 bit binary counter



- Excitation Table?

Current State			Next State			Flip-flop Inputs		
A2	A1	A0	A2	A1	A0	TA2	TA1	TA0
0	0	0	0	0	1			
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	1	0	1			
1	0	1	1	1	0			
1	1	0	1	1	1			
1	1	1	0	0	0			

Desing of Counter

- Flip-flop input functions?

Current State			Next State			Flip-flop Inputs		
A2	A1	A0	A2	A1	A0	TA2	TA1	TA0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

TA2 ?

TA1 ?

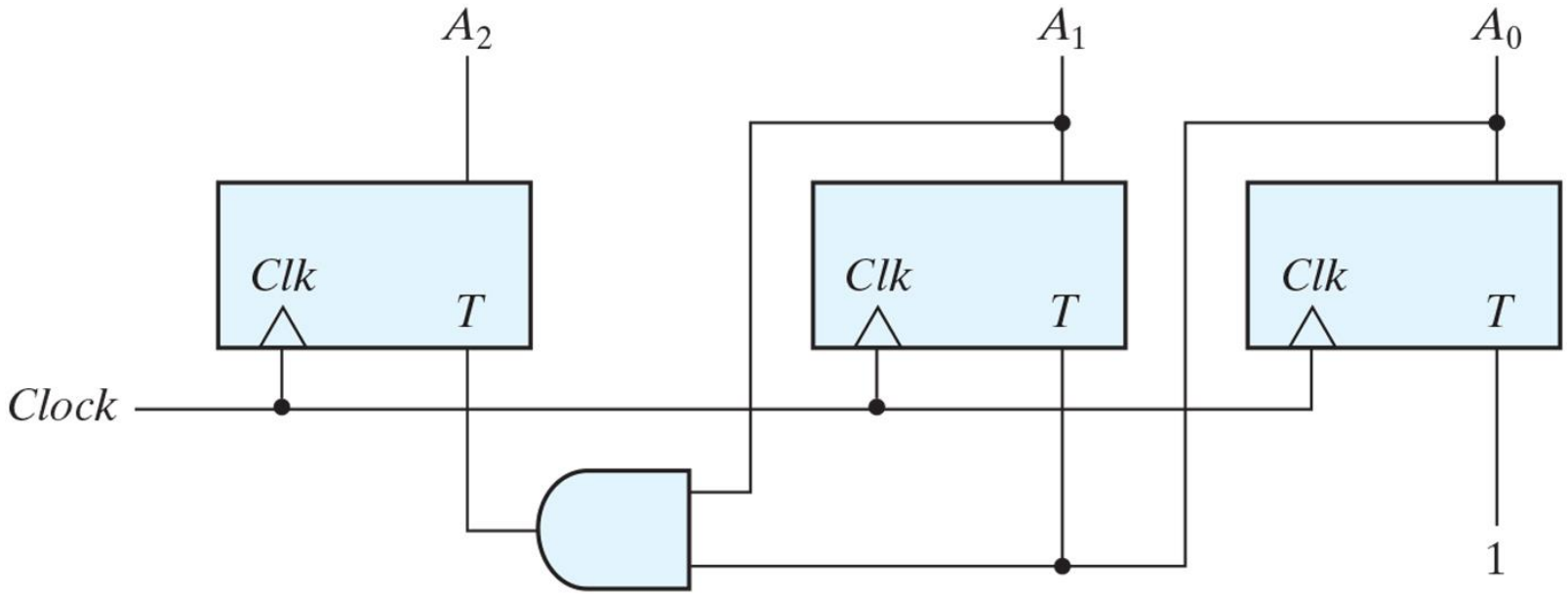
TA0 ?

Design of Counter

TA2=A1A0

TA1=A0

TA20=1



Other Counters

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J	K	Q(t+1)	R
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t+1)	0

- A counter with n flip-flops may have less then 2^nnumber of states.
- Ex:

Current State			Next State			Flip-flop inputs					
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1						
0	0	1	0	1	0						
0	1	0	1	0	0						
1	0	0	1	0	1						
1	0	1	1	1	0						
1	1	0	0	0	0						

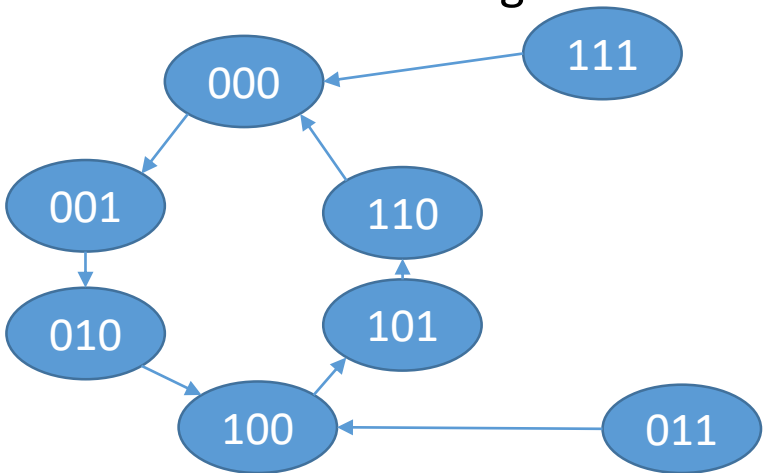
Ex: Other Counters

- Flip-flop inputs:
  - JA=B KA=B
  - JB=C KB=1
  - JC=B' KC=1

Current state			Sonraki durum			Flip-flop girişleri					
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

- What happens when the circuit is in state 011?
  - JA=KA=1
  - JB=KB=1
  - JC=0, KC=1
  - Next State: 100

State Diagram of the Counter:



Problem

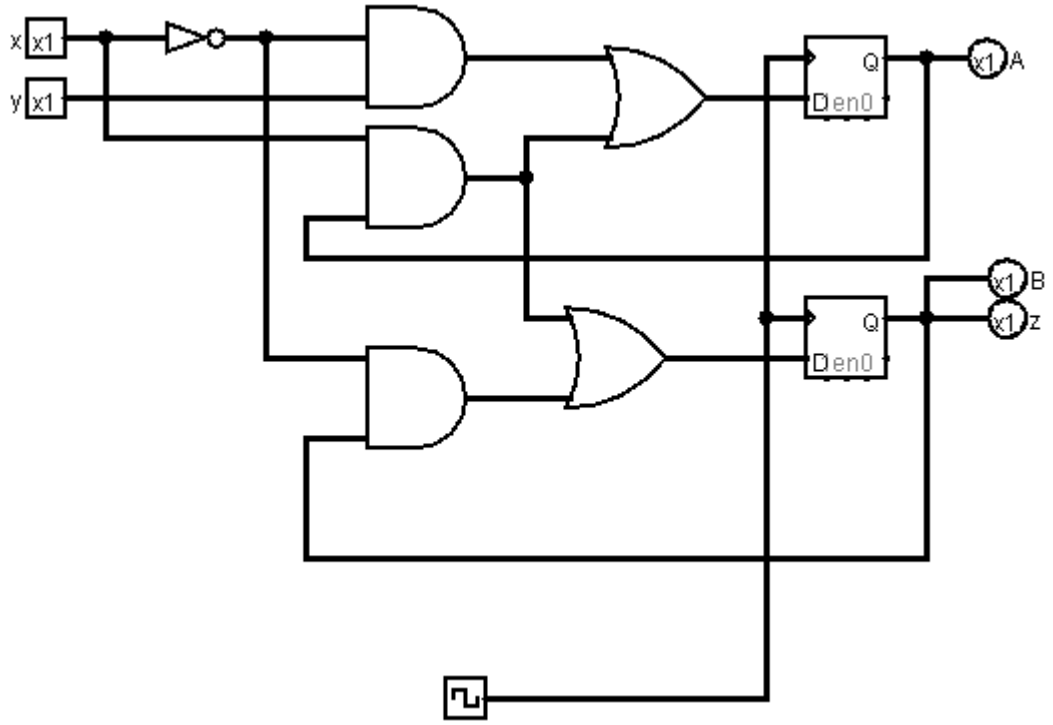
- A sequential circuit with two D flip-flops A and B, two inputs x and y and an output z is defined with the following next state and output functions:
  - $A(t+1)=x'y+xA$
  - $B(t+1)=x'B+xA$
  - $z=B$

  - Draw the logic diagram for this circuit.
  - Write the state table.
  - Draw the state diagram.

Problem…

- A(t+1)=x’y+xA
- B(t+1)=x’B+xA
- z=B

- The logic diagram of the circuit:



Problem…

- State Table

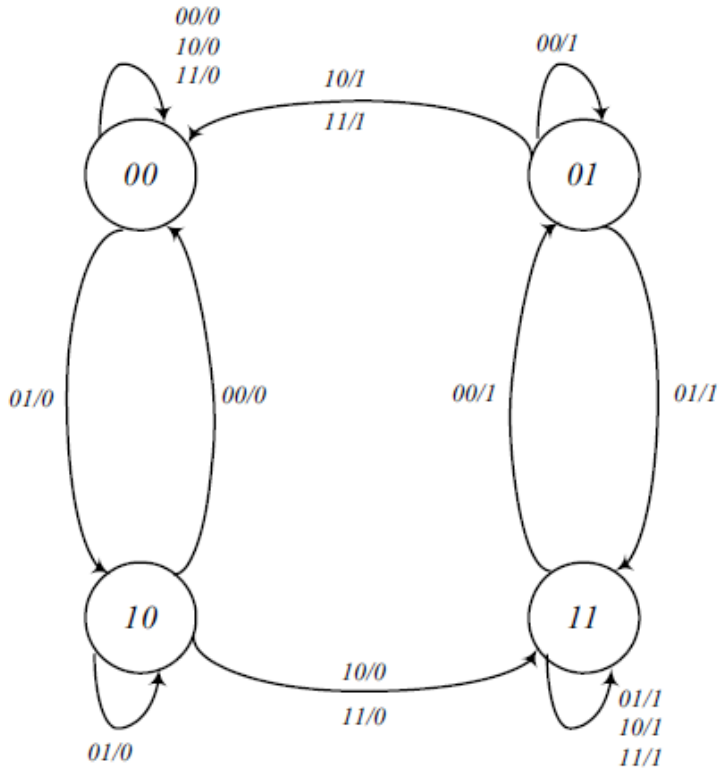
A(t+1)=x’y+xA
B(t+1)=x’B+xA
z=B

Present State		Inputs		Next State		Output
A	B	x	y	A	B	z
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Problem…

- State Diagram:

Present state		Inputs		Next state		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1



References

- Morris Mano, Digital Design.