Digital Logic Systems– Synchronous Sequential Logic- II

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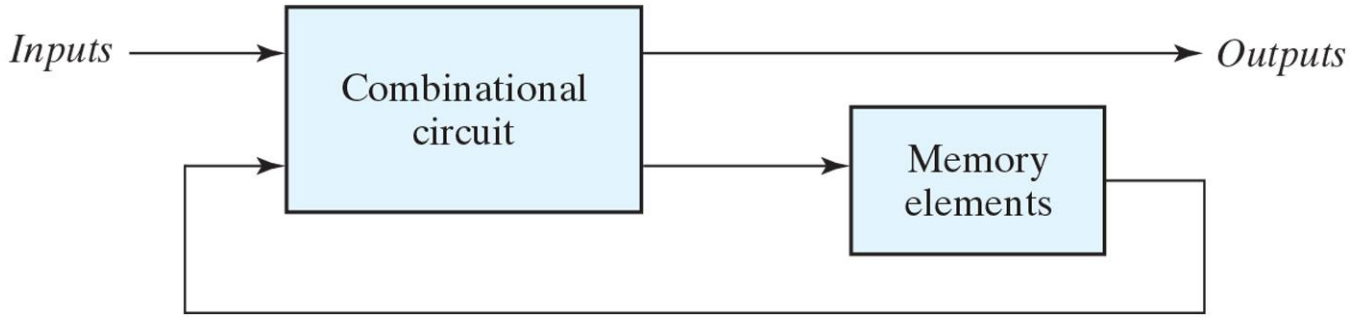
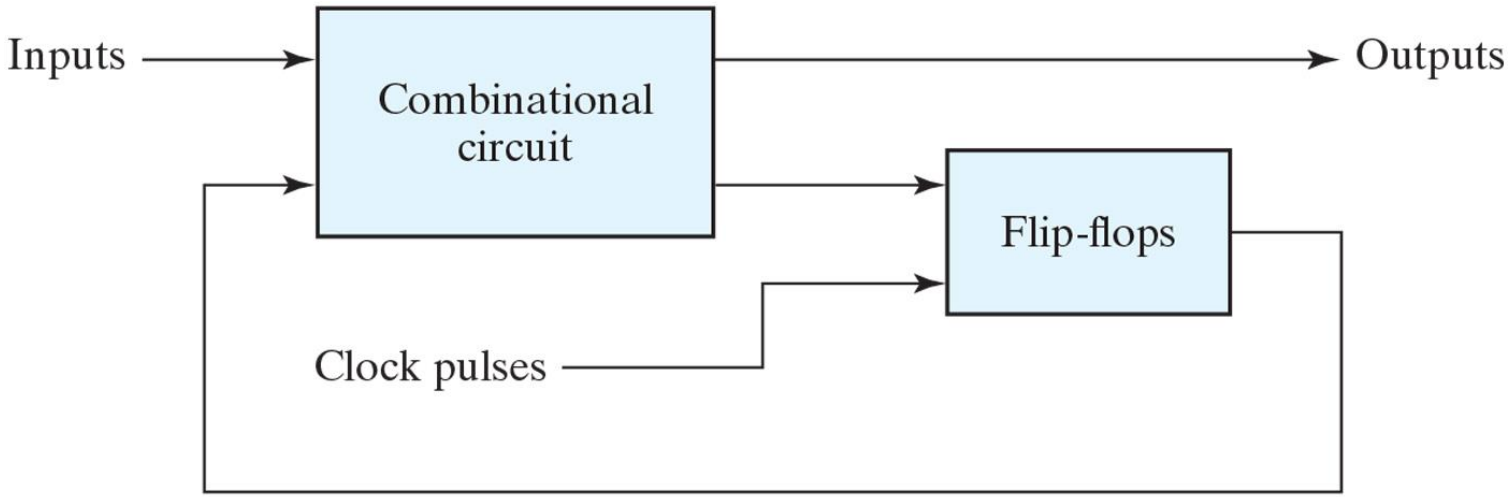
Block Diagram of Sequential Circuit



- Memory Elements
  - Store binary data.
  - This data is referred as the current state of the flip-flop.
- Sequential Circuit
  - Determines the output using input and the current state.
  - Input and the current state determine the next state.

Synchronous Sequential Circuit



(a) Block diagram

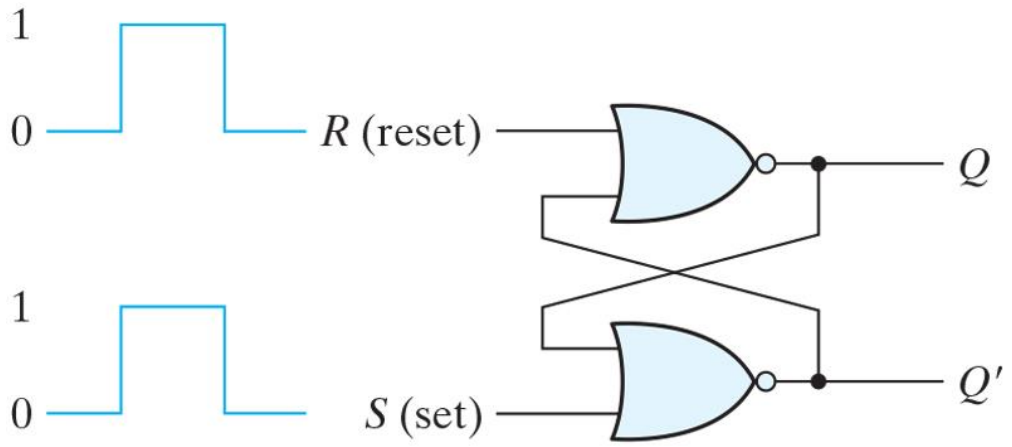
(b) Timing diagram of clock pulses

Flip-Flops

- A flip-flop can hold its state until an input signal is asserted to change its state.
- Types of Flip-flops vary:
  - By the number of input signals.
  - How the inputs effect the binary state of the flip-flop.

A Simple Flip-flop Circuit

x	y	x NOR y
0	0	1
0	1	0
1	0	0
1	1	0



(a) Logic diagram

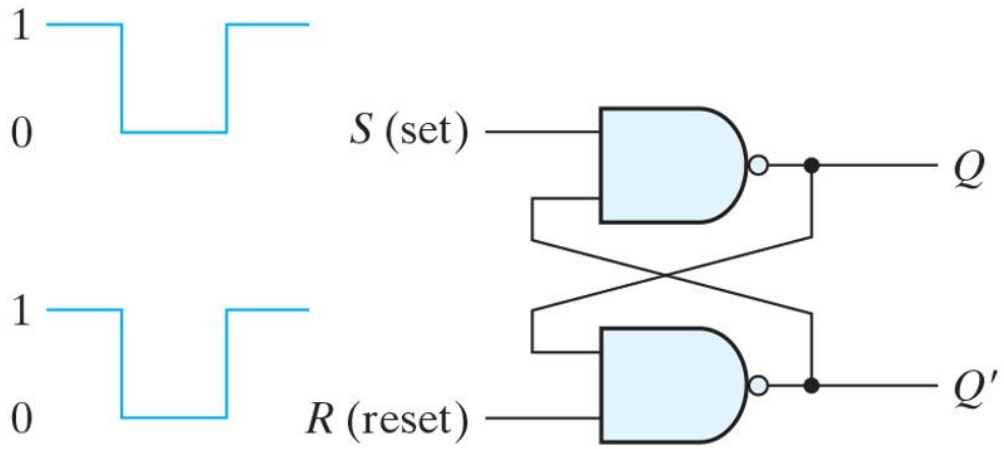
S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

Q state of the flip-flop, Q' complement of Q.
Q=1, Q'=0 set
Q=0, Q'=1 reset

Flip-Flop with NAND Gates

x	y	x NAND y
0	0	1
0	1	1
1	0	1
1	1	0



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

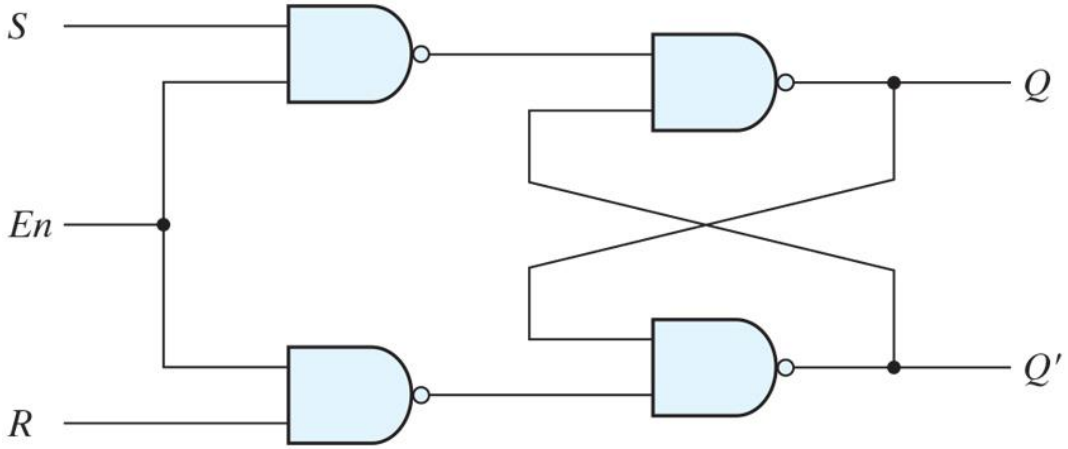
RS Flip-Flop

	00	01	11	10
0			X	1
1	1		X	1

Q(t+1)=S + R'Q
SR = 0
Characteristic Equation

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indetermined
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indetermined

Characteristic Table



(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

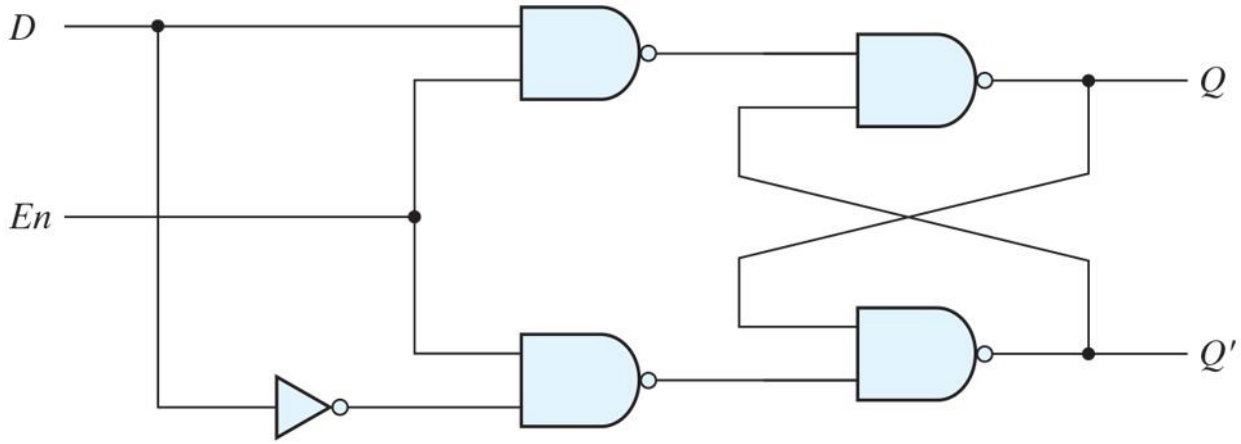
D Flip-Flop

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Table

	0	1
0		1
1		1

Q(t+1)=D
Characteristic Equation

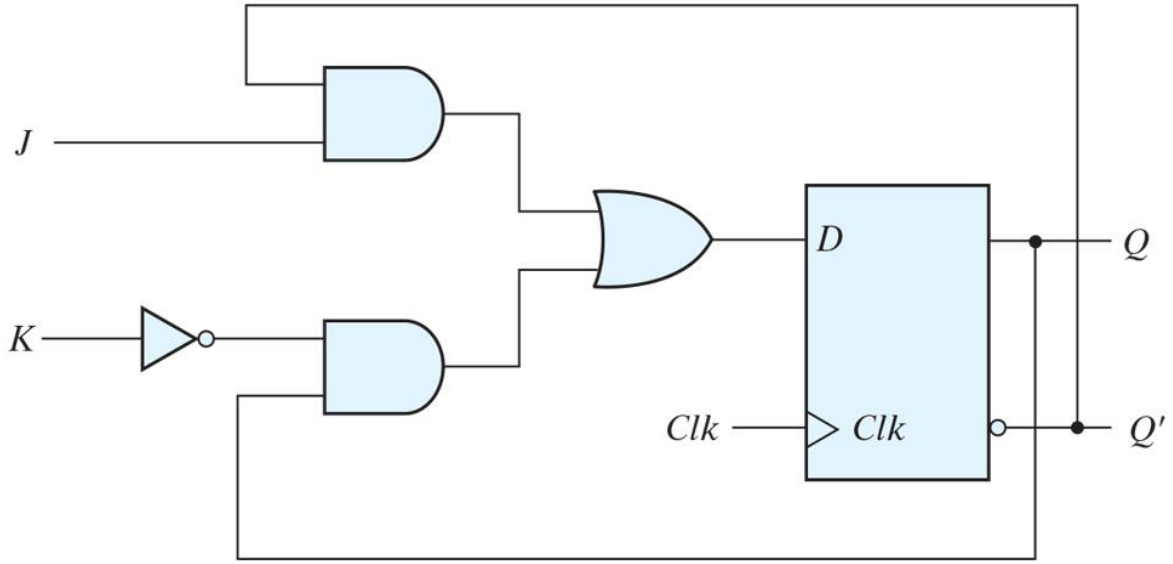


(a) Logic diagram

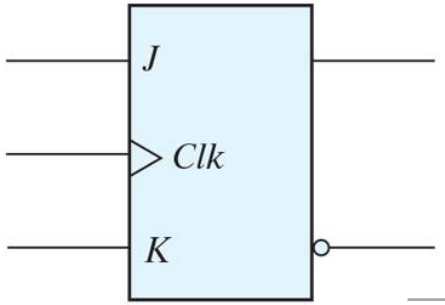
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

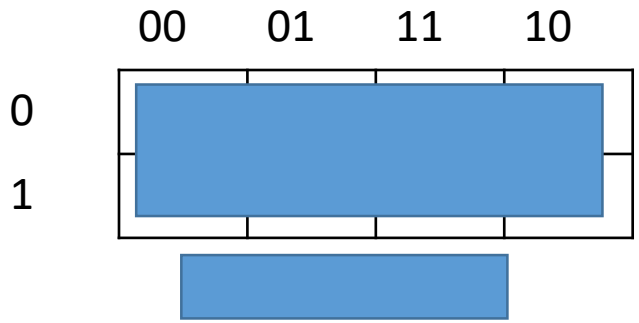
J-K Flip-Flop



(a) Circuit diagram



(b) Graphic symbol

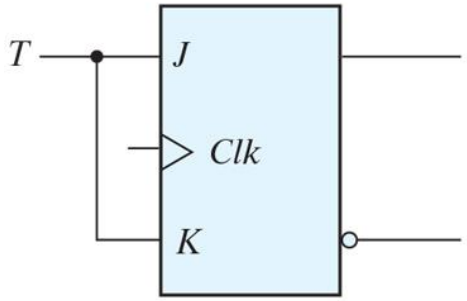


Characteristic Equation

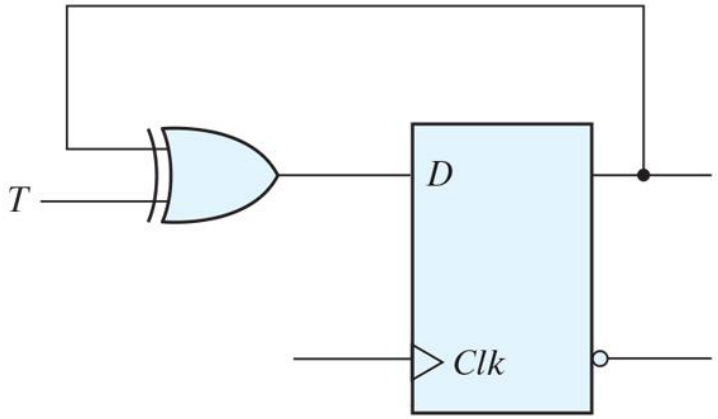
Q	J	K	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Characteristic Table

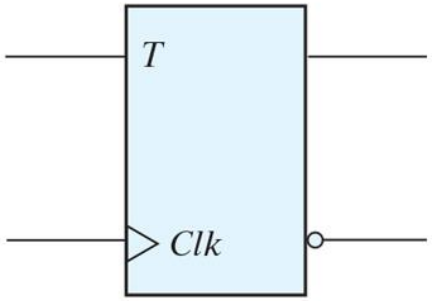
T Flip-Flop



(a) From *JK* flip-flop



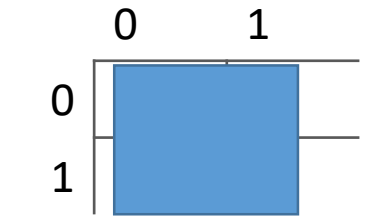
(b) From *D* flip-flop



(c) Graphic symbol

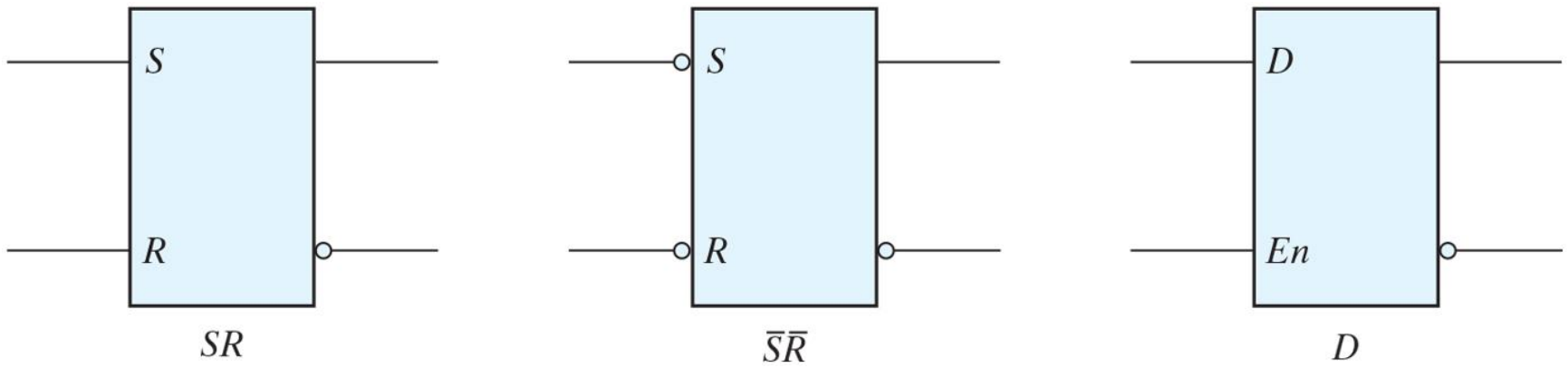
Q	T	Q(t+1)
0	0	
0	1	
1	0	
1	1	

Characteristic Table

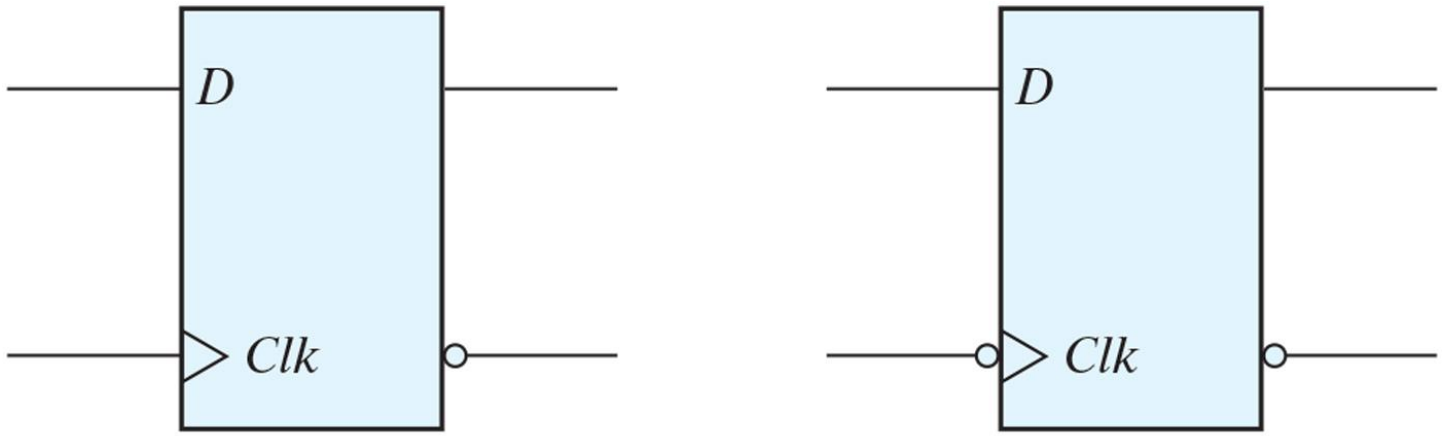


Characteristic Equation

Graphical Symbols of Flip-Flops



Graphical Representation of Edge Triggered D Flip-Flops



(a) Positive-edge (b) Negative-edge

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

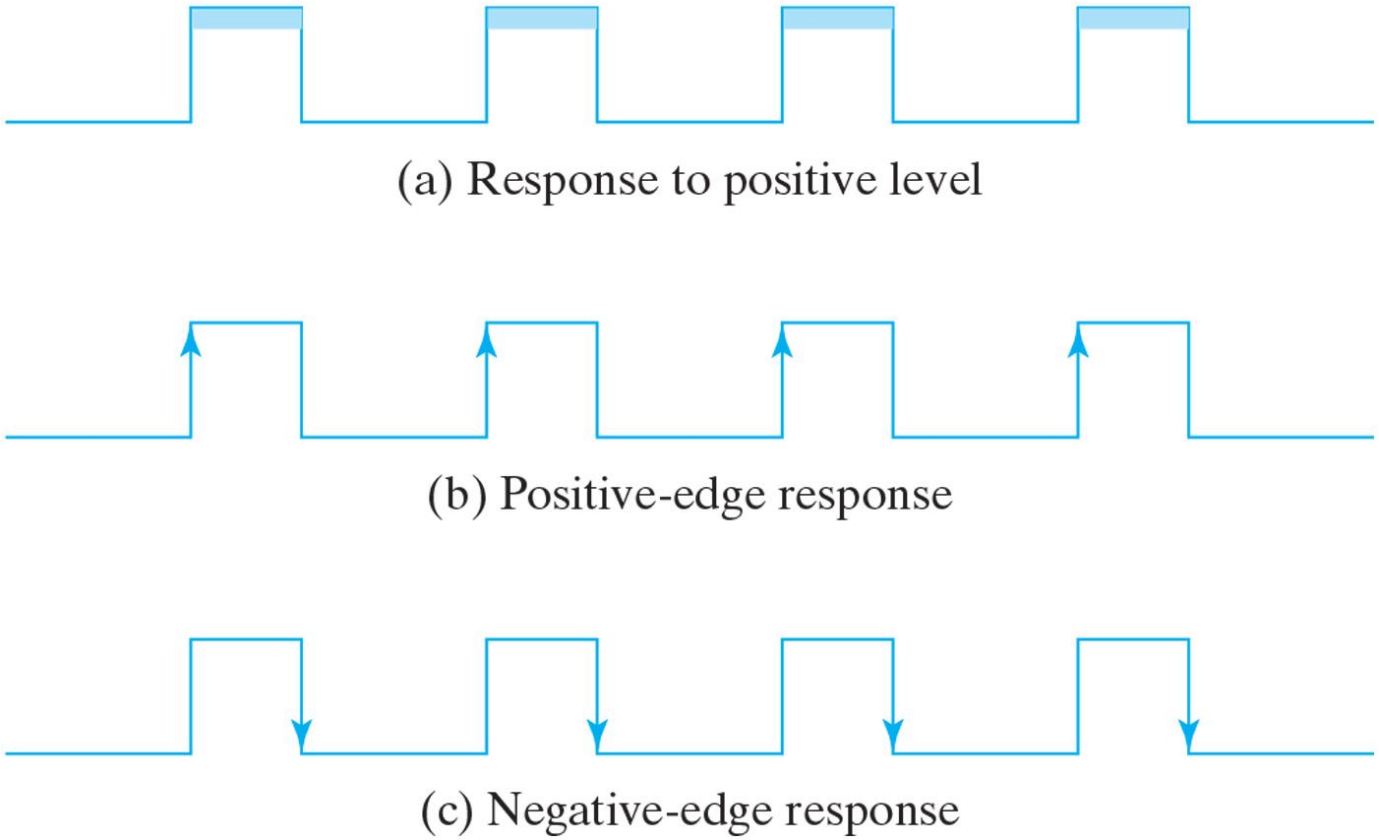
D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Flip-Flop and Clock Signal

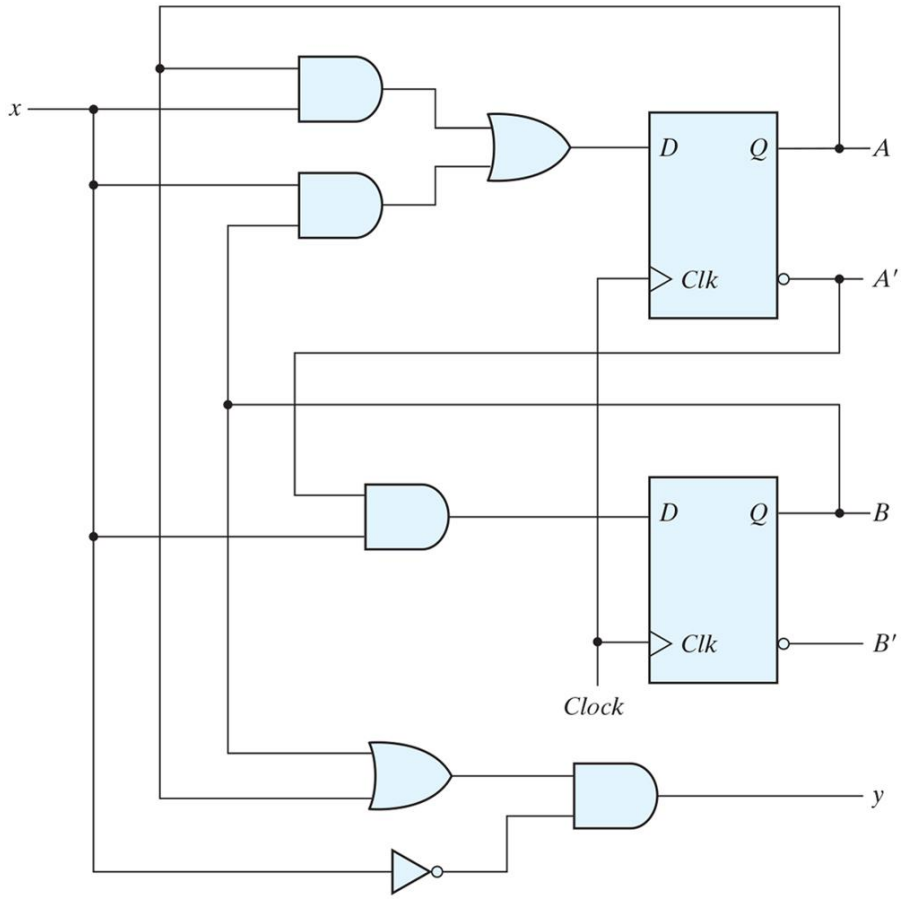
- If flip-flops respond to a level of clock, indetermined conditions may arise.
  - If the flip-flop outputs change while the output of the combinational circuit which are fed as input to flip flops then indetermined condition arises.
  - Solution: Flip-flops respond to clock transitions..



Analysis of Clocked Sequential Circuits

- Analysis describes what a given circuit will do under certain operating conditions.
- Obtain a table or a diagram for the time sequence of inputs, outputs and internal states.
- An algebraic representation for specifying the next-state condition in terms of the present state and inputs.
- **State Equations:** specifies the next state as a function of the present state and inputs.

Example of a Sequential Circuit



- State Equations?

$$A(t+1) = \mathrm{Ax} + \mathrm{Bx}$$

$$B(t+1) = A'x$$

$$y = (A + B)\mathrm{x'}$$

- State Table?

State Table- 1

$$A(t+1) = \mathrm{Ax} + \mathrm{Bx}$$
$$B(t+1) = A'x$$
$$y = (A+B)\mathrm{x}'$$

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

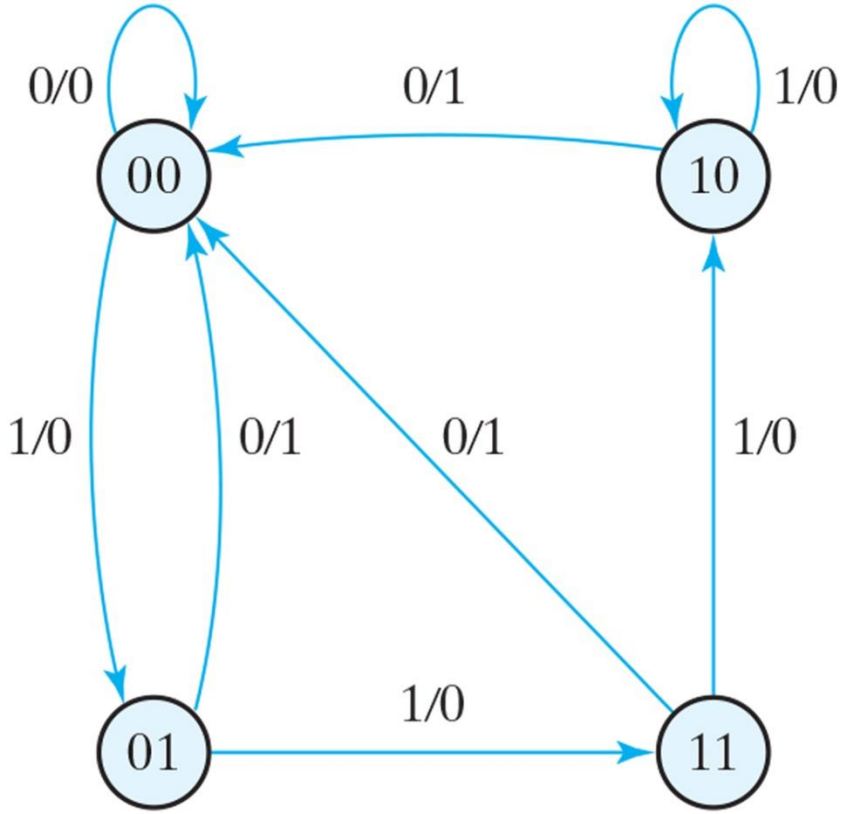
State Table- 2

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

State Diagram

- How many states ?
- How to represent transitions between states?

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

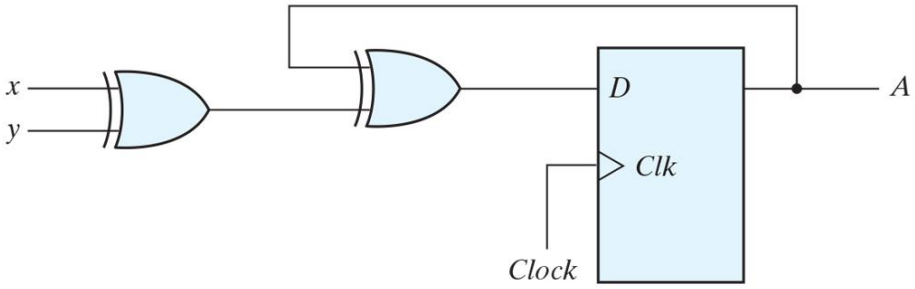


Flip-Flop Input Equations

- *What is the input equation for a D flip-flop which comes from an output of an OR gate with inputs x and y?*
  - $D_Q = x + y$

Analysis with D Flip-Flop

A(t+1) = A xor (x xor y)



(a) Circuit diagram

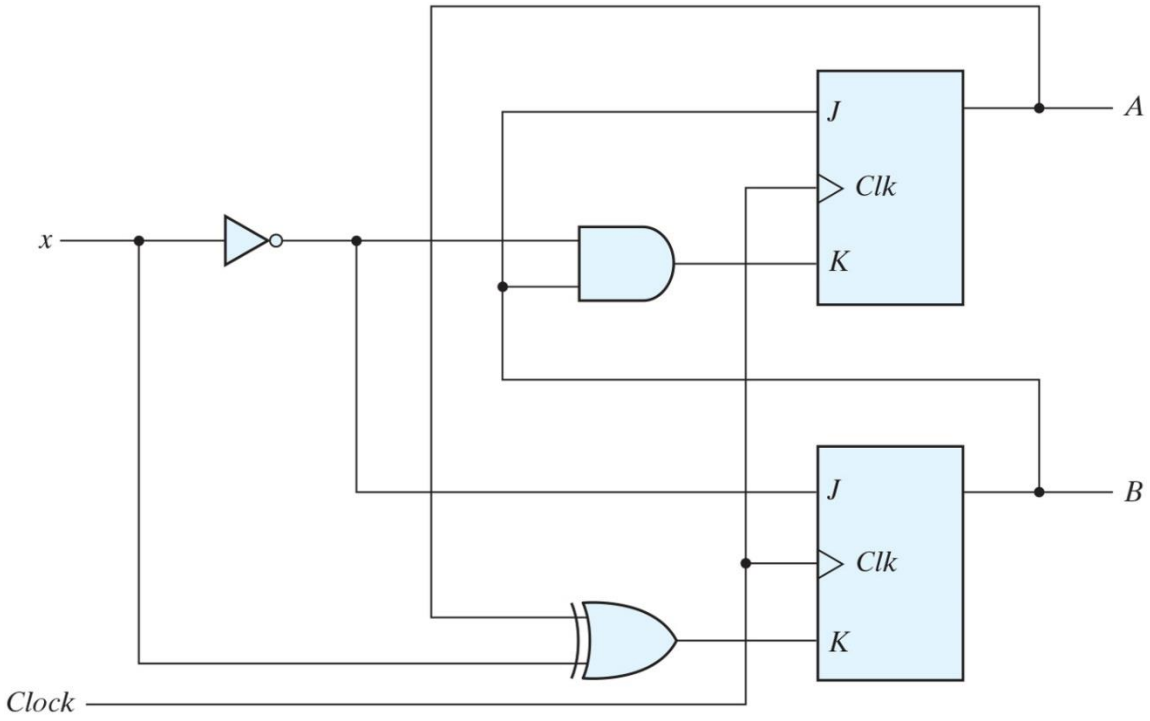
(b) State table

Present State	Inputs		Next State
A	x	y	A
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(c) State diagram

Analysis with JK Flip-Flop

JK Flip-Flop			
J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement



$J_A = B$ $J_B = x'$

$K_A = x'B$ $K_B = A \text{ xor } x$

- State Table

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

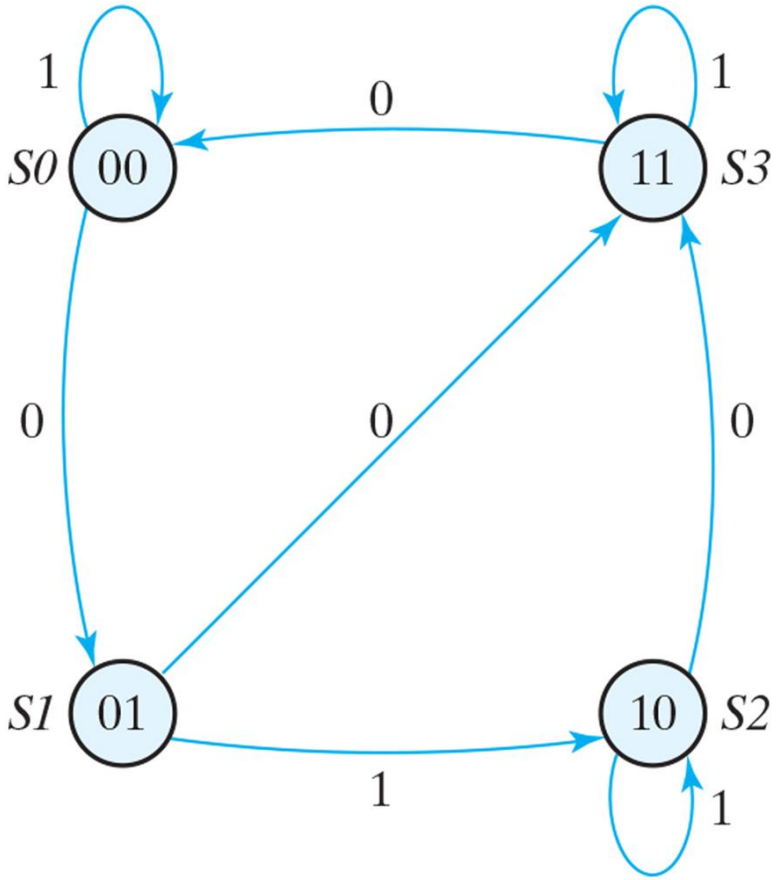
Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Present State		Input	Next State		Flip-Flop Inputs			
A	*B*	*x*	*A*	*B*	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Analysis with JK Flip-Flop..

- State Diagram
  - From state diagram to state table

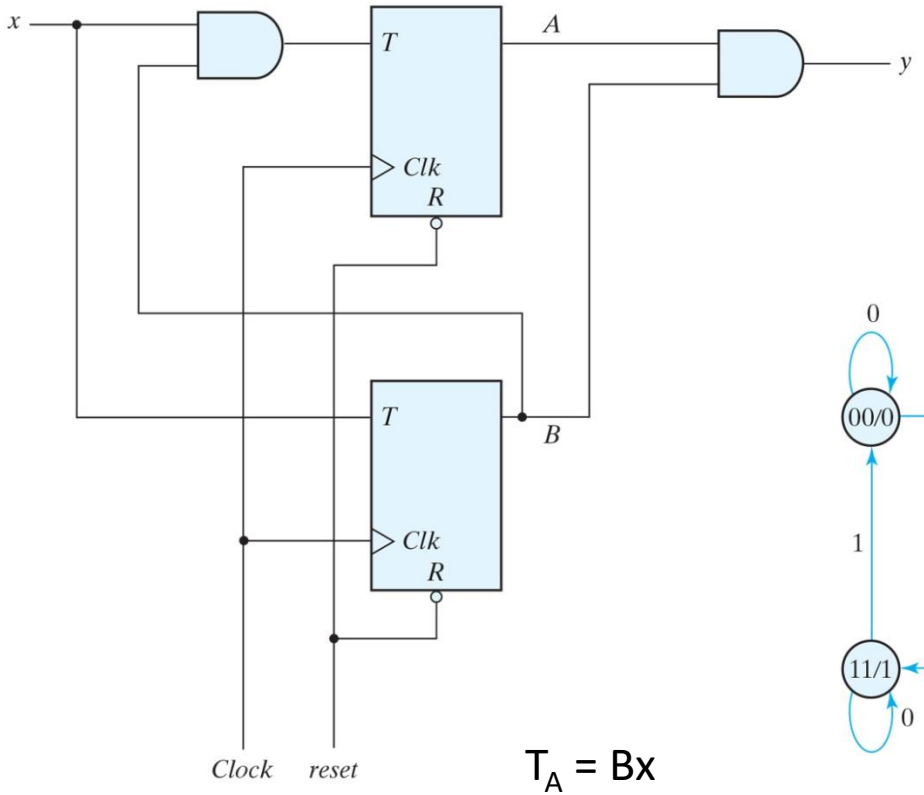
Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0



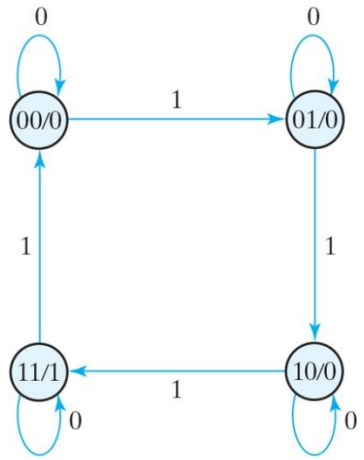
Analysis with T Flip-Flop

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement



(a) Circuit diagram



(b) State diagram

$T_A = Bx$

$T_B = x$

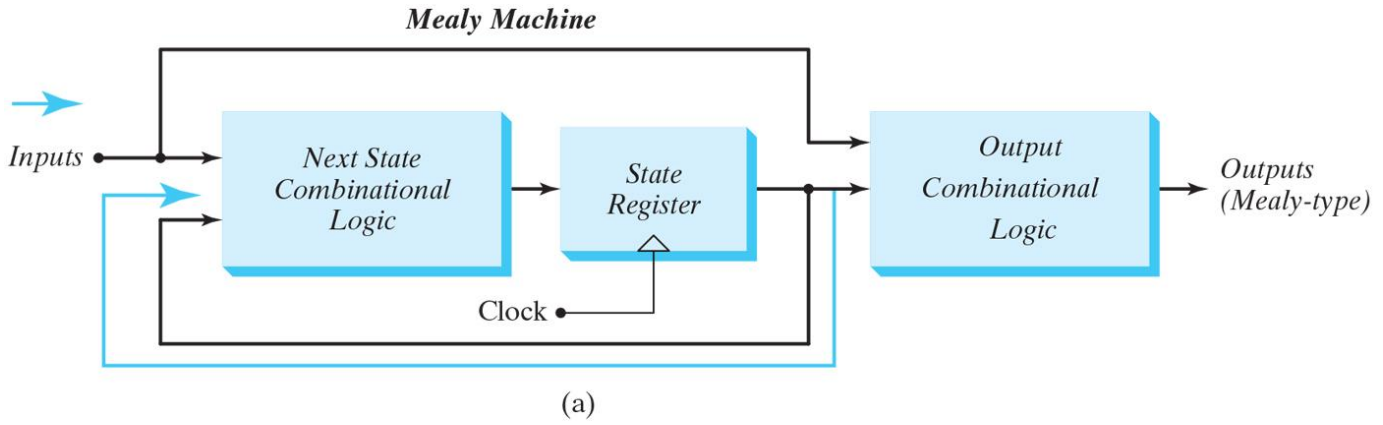
$y=AB$

- State Table

Present State A	Present State B	Input x	Next State A	Next State B	Output y	TA	TB
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

Mealy and Moore Models



- Questions ?
- Comments ?

References

- Morris Mano, Digital Design