Digital Logic Systems – Synchronous Sequential Logic - II

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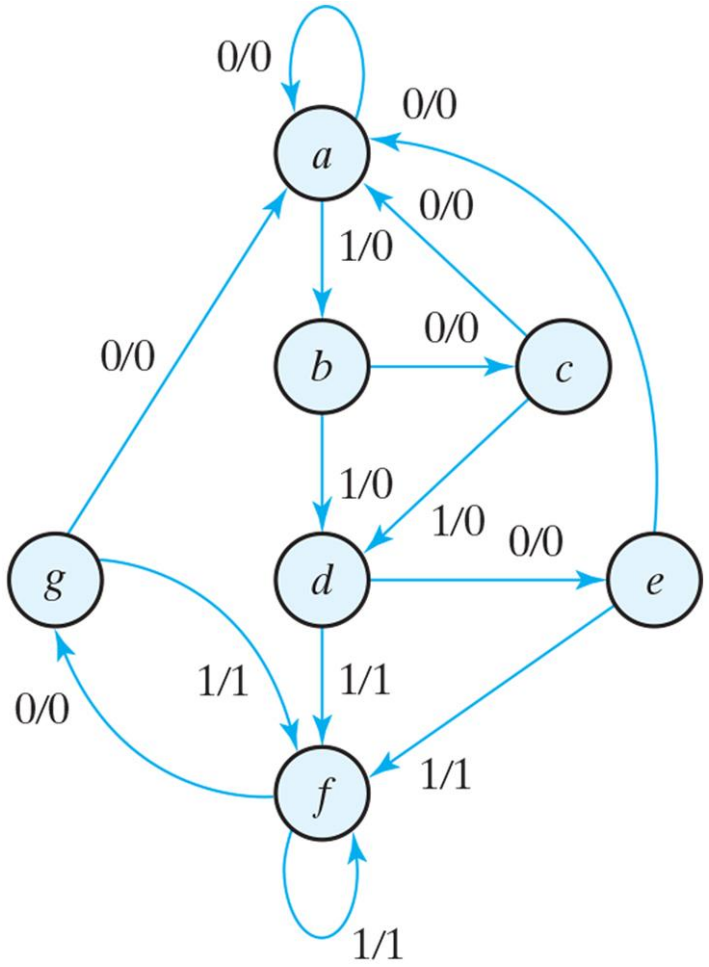
State Reduction and Assignment

- Analysis of Sequential Circuit:
  - Circuit → State Table/Diagram

  - What are the properties of the sequential circuit that enable us to reduce the number of Gates and flip-flops during design?

Example

- State diagram:
  - Only the input-output sequence is important. Internal states are shown as letters.
  - Example iput: 01010110100
    - starting from state a, process the input sequence

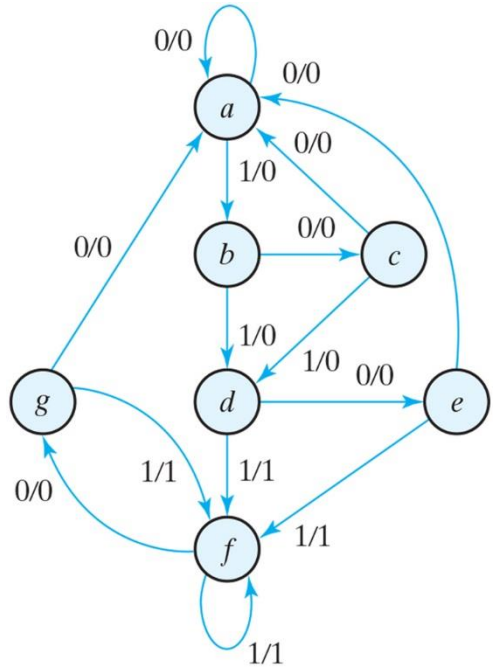


state	a	b	c	d	e	f	f	g	f	g	a	
Input	0	1	0	1	0	1	1	0	1	0	0	
Output												

State Reduction

- The process of reducing the number of states without effecting the input-output relations.
- For the previous example; obtain the **state table**

	Sonraki Durum		Çıkış	
Şimdiki Durum	x=0	x=1	x=0	x=1
a				
b				
c				
d				
e				
f				
g				



Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

State Reduction

- If two states give the same output for each input element and take the circuit to an equivalent state then those states are equavalent states.
- If two states are equivalent, taking one of them out does not change the input-output relation.
- In the previous example:
  - Which states are equivalent?
    - g and e
    - d and f
  - What is the reduced table?

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

State Reduction - Example

- For g and e:

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

- For d and f:

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

State Assignment

- State assignment is important for minimization of the combinational circuit.
- State assignment is the problem of assigning binary values to states such that the cost of combinational circuit which determines flip-flop inputs is reduced.

Previous Example

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

- As long as the input-output relation is preserved the binary values of states do not matter.
  - Any assigment can be used as long as different binary values are assigned to different states.
  - But which one to choose?

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

State Table with Assignment 1

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
000	000	001	0	0
001	010	011	0	0
010	000	011	0	0
011	100	011	0	1
100	000	011	0	1

State Assignment

- A different assignment will result in a different state table with different states but same input-output.
- Binary values of states in the state table are used to determine the combination part of the sequential circuit. The complexity of the combination circuit depends on the binary assignment used.
- Important criteria for choosing the binary assignment:
  - The assignment results in a simple combinational circuit for flip-flop inputs.
  - There is no method for state assignment that guarantees a minimum cost combinational circuit.

Flip-Flop Excitation Tables

- Input and current state known → next state is determined by:
  - Characteristic table

  - In design we usually know the current state and the next state, and we deal with the flip-flop inputs:
    - Table which shows the inputs for state transitions:
      - EXCITATION TABLE

RS Flip-Flop Excitation Table

- RS Flip-Flop Characteristic Table

S	R	Q(t+1)	R
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	?	0

- RS Flip-Flop Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK Flip-Flop Excitation Table

- JK Flip-Flop Characteristic Table

J	K	Q(t+1)	R
0	0	Q(t)	No change.
0	1	0	Reset
1	0	1	Set
1	1	Q’(t+1)	Complement

- JK Flip-Flop Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Flip-Flop Excitation Table

- D Flip-Flop Characteristic Table

D	Q(t+1)	
0	0	Reset
1	1	Set

- D Flip-Flop Excitation Table

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-Flop Excitation Table

- T Flip-Flop Characteristic Table

T	Q(t+1)	
0	Q(t)	No change.
1	Q’(t)	Complement.

- T Flip-Flop Excitation Table

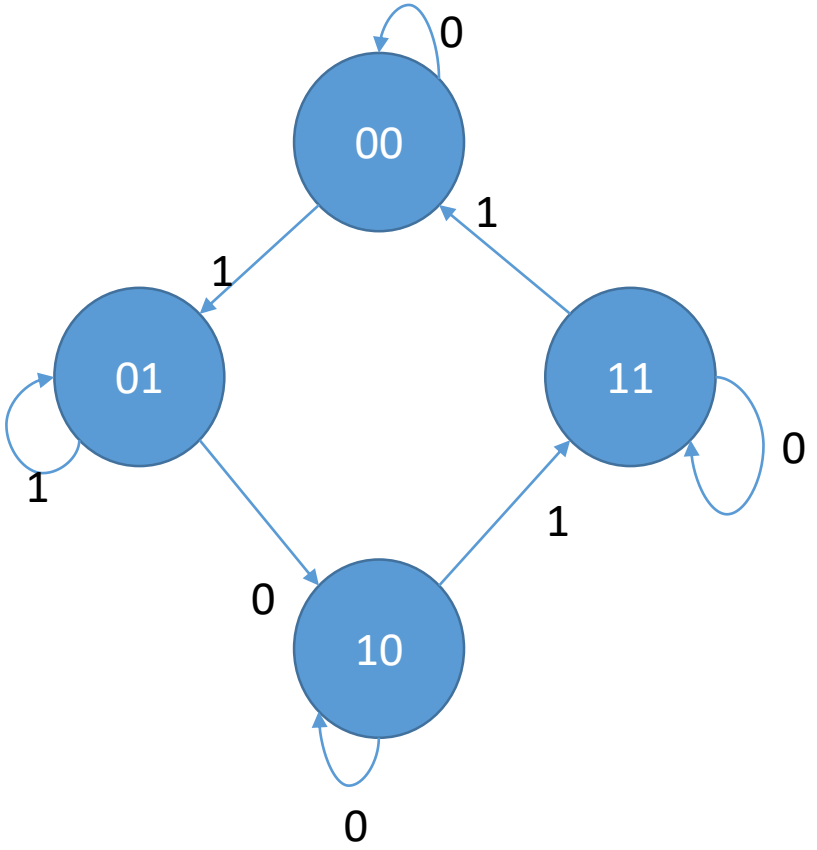
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Design Procedure

1. From the word description and specifications of the desired operation derive a state diagram for the circuit.
2. Reduce the number of states if necessary.
3. Assign binary values to the states.
4. Obtain the binary coded state table.
5. Choose the type of flip-flops to be used.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

Example

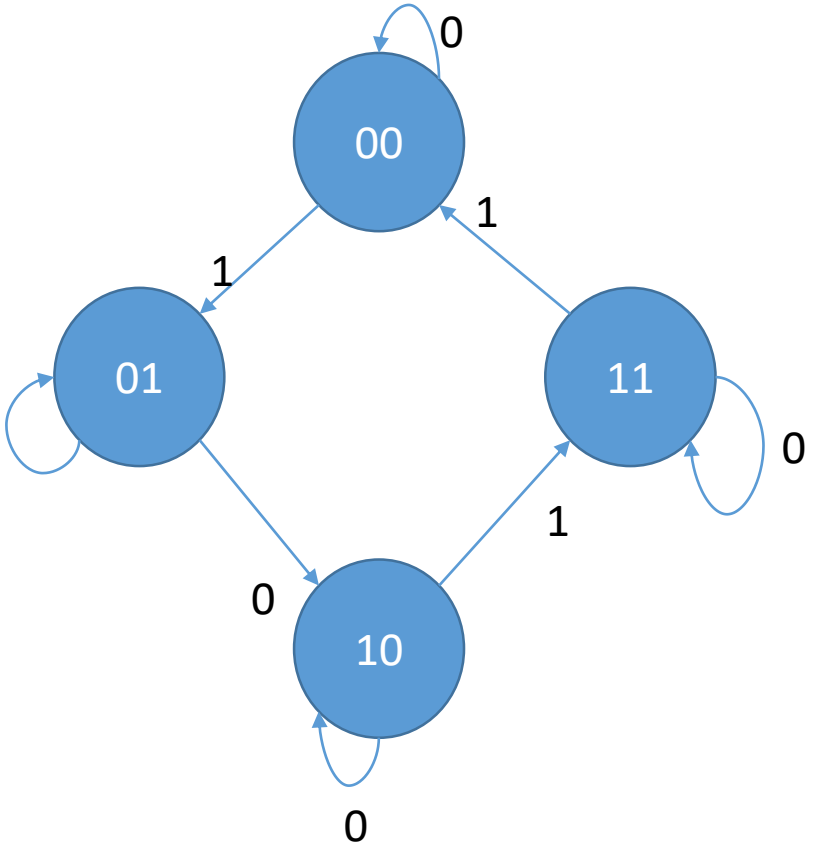
- Design the clocked sequential circuit whose state diagram is given using JK flip-flops.
  - inputs?
  - outputs?
  - Number of states?
  - Number of flip-flops?



Example..

- State table:

Current state		Next State			
		x=0		x=1	
A	B	A	B	A	B
0	0				
0	1				
1	0				
1	1				



Example…

- State Table

Current State		Next State			
		x=0		x=1	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

Example..

- What is an excitation table?
- How can it be obtained?

- Excitation table lists the inputs for each state transition.
- State diagram and JK flip-flop excitation table is used to obtain the excitation table for a circuit.

J	K	Q(t+1)	R
0	0	Q(t)	No change.
0	1	0	Reset
1	0	1	Set
1	1	Q'(t+1)	Complement

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Current State		Next State			
		x=0		x=1	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

Combinational Circuit Inputs					Combinational Circuit Outputs			
Current State		Input	Next State		Flip-flop Inputs			
A	B	x	A	B	JA	KA	JB	KB
0	0	0	0	0				
0	0	1	0	1				
0	1	0	1	0				
0	1	1	0	1				
1	0	0	1	0				
1	0	1	1	1				
1	1	0	1	1				
1	1	1	0	0				

Example…

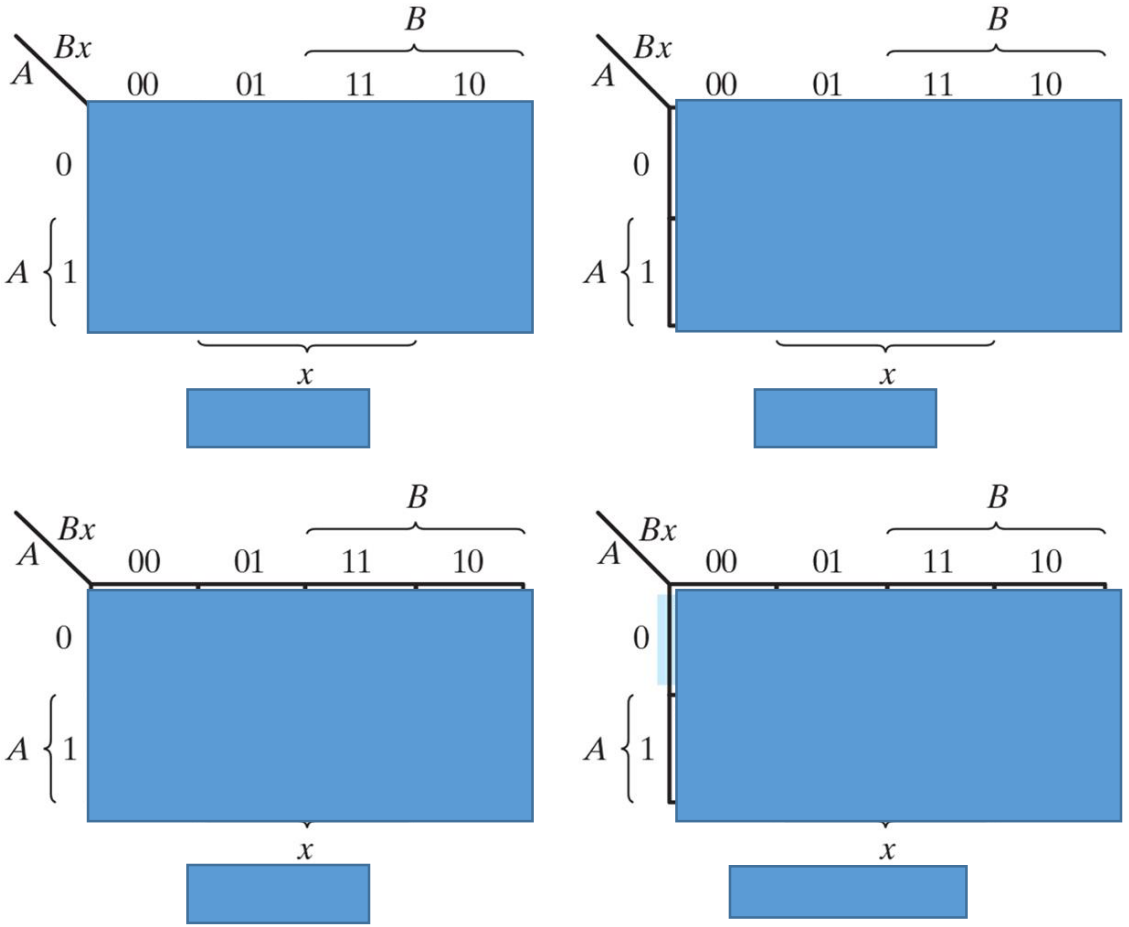
- Excitation Table

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Example…

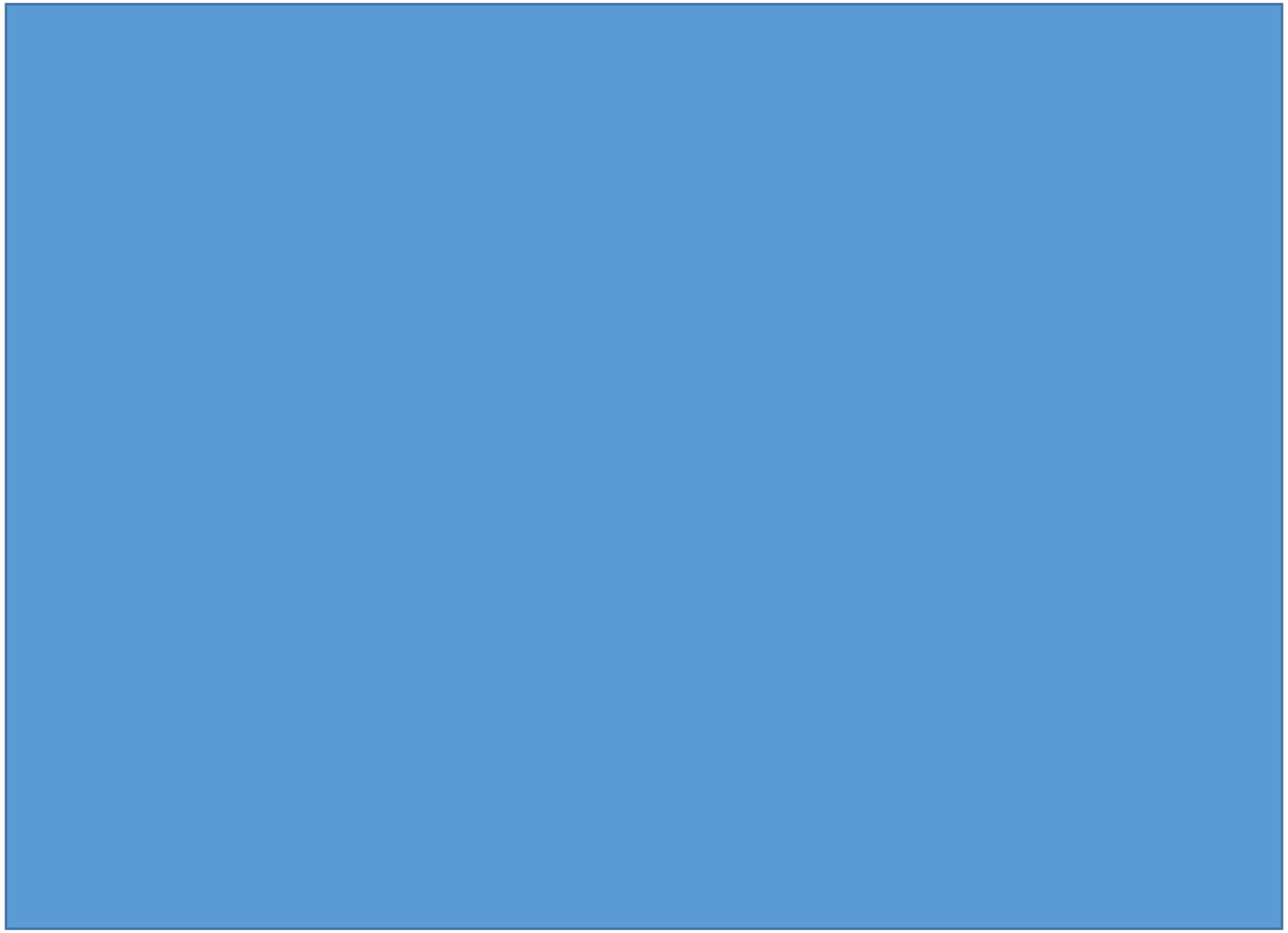
- Karnaugh Maps for Flip-flop inputs

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1



Example…

- Logic Diagram:



- J_A=Bx’
- K_A=Bx

- JB=x
- KB=(A xor x)’

Reference

- Morris Mano, Digital Design, 2nd edition.