# Digital Logic Systems – Registers, Counters and Memory Units- II

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# Previously..

- Synchronous sequential circuits for special purposes:
  - Registers
  - Counters
  - Memory Units

- Registers
  - Register with parallel load
  - Shift registers
  - Universal Shift Register

# Counters

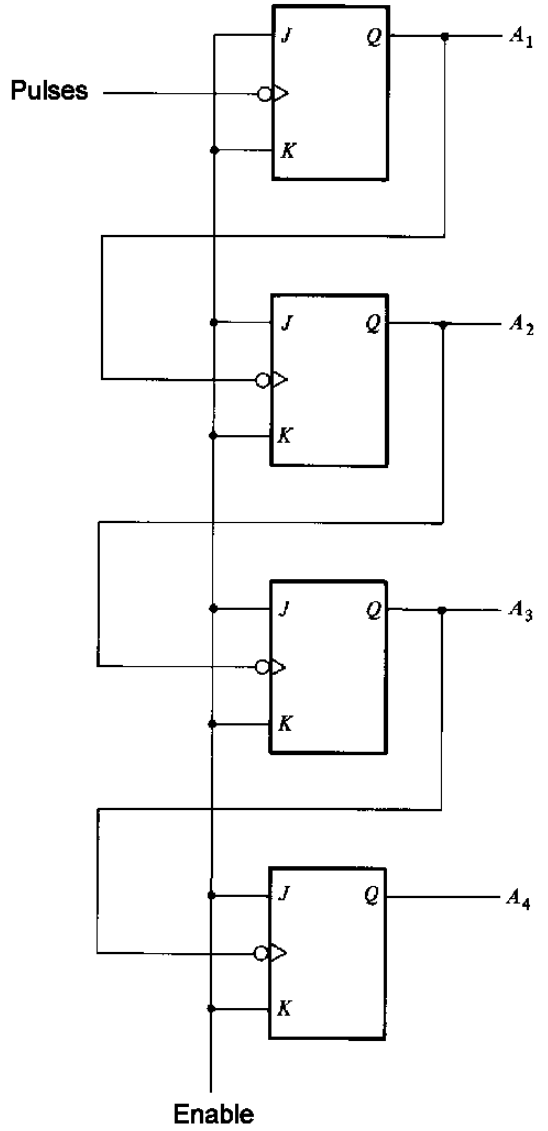
- Two types of MSI Counters
  - Ripple Counters: a flip-flop output transition serves as a source for triggering other flip-flops.
    - the C input of some or all flip-flops are triggered not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.
  - Synchronous Counters: the C input s of all flip -flops receive the common clock.

# Binary Ripple Counter

- A binary ripple counter consists of a series connection of complementing flip-flops with the output of each flip-flop connected to the C input of the next higher order flip-flop.
- The flip-flop holding the least significant bit receives the incoming count pulses
- A complementing flip-flop can be obtained from:
  - JK flip-flops by tieding J and K inputs together.
  - T flip-flops
  - D flip-flop with the complement output connected to the *D* input.

# Binary Ripple Counter

- 4 bit binary ripple counter:
  - JK inputs are 1. What does that mean?
    - Flip-flops will complement each time they are triggered.
  - Circle in the clock input implies that the flip-flop is negative edge triggered.



# Binary Ripple Counter

- Counting sequence:

| Sayma Sırası | | | | | |
|---|---|---|---|---|---|
| $A_4$ | $A_3$ | $A_2$ | $A_1$ | | |
| 0 | 0 | 0 | 0 | Complement of $A_1$ | |
| 0 | 0 | 0 | 1 | Complement of $A_1$ | $A_1$ 1→0, $A_2$ is complemented |
| 0 | 0 | 1 | 0 | Complement of $A_1$ | |
| 0 | 0 | 1 | 1 | Complement of $A_1$ | $A_1$ 1→0, $A_2$ is complemented |
| | | | | | $A_2$ 1→0, $A_3$ is complemented |
| 0 | 1 | 0 | 0 | Complement of $A_1$ | |
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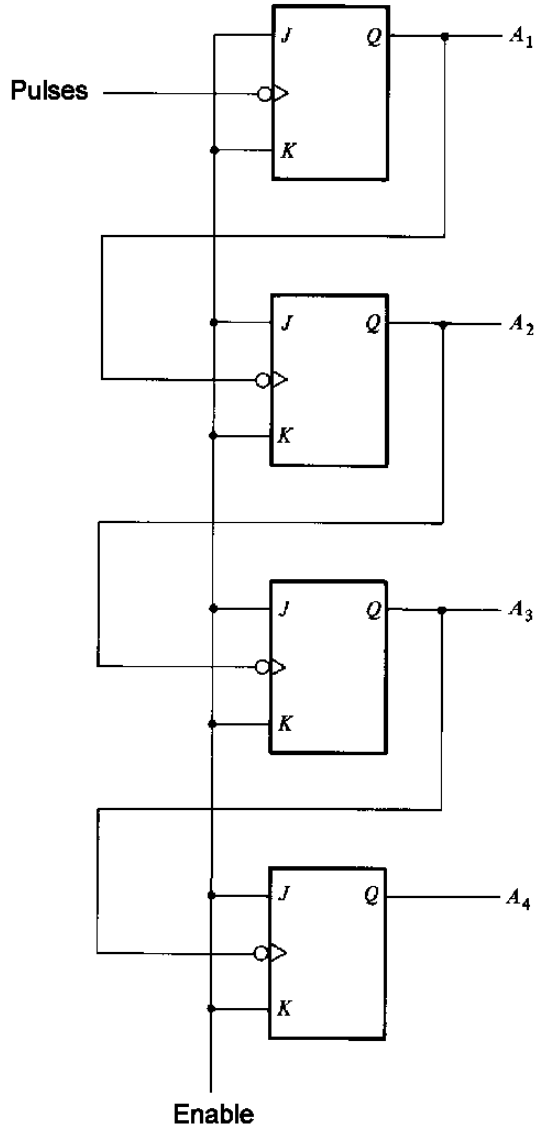
| | | | | | $A_2$ 1→0, $A_3$ is complemented |
| | | | | | $A_3$ 1→0, $A_4$ is complemented |
| 1 | 0 | 0 | 0 | … | |



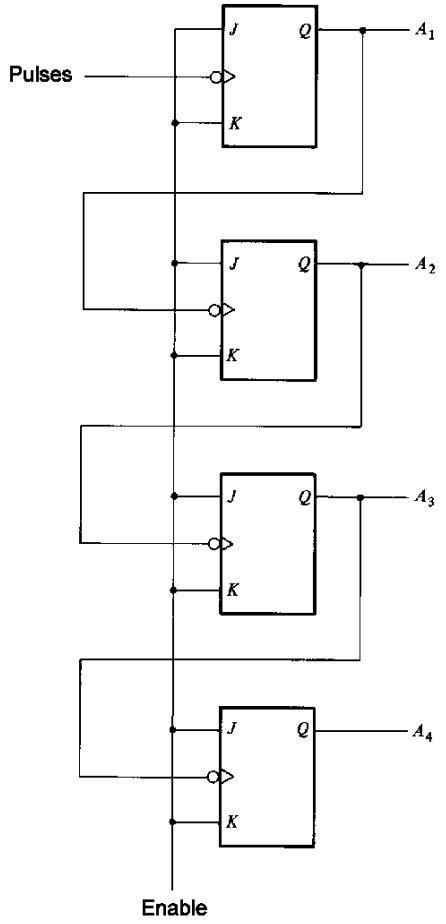
# Binary Ripple Counter

- The flip-flops change one at a time in succession, and the signal propagates through the counter in a ripple fashion from one stage to the next.
- Ripple counters are asynchronous counters.

# Ripple Counter

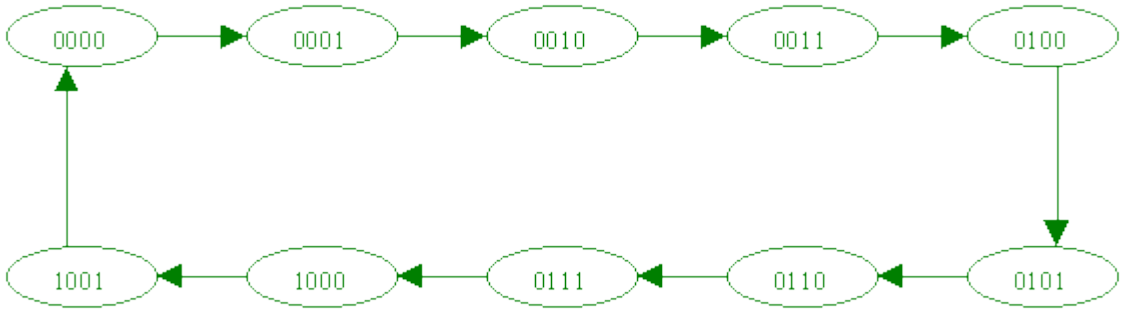
- Binary Countdown Counter: A binary counter with a reverse count.
  - the binary count is decremented by I with every input count pulse.
  - The count of a four-bit countdown counter starts from binary 15 and continues to binary counts 14,13,12,…,0. and back to 15.
  - If the outputs are obtained from Q’ instead of Q then a binary countdown counter is obtained.
    - The least significant bit is complemented at each pulse.
    - Other bits are coplemented when a previous bit goes from 0 to 1.
      - Either all flip-flops are positive edge triggered.
      - Or the C inputs of flip-flops are obtained from Q’ of the previous flip-flop.

1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000



# BCD Ripple Counter

- Decimal Counter 0-1-2-…-9-0
- How many flip-flops are required to represent a decimal?
  - 4
- State diagram?

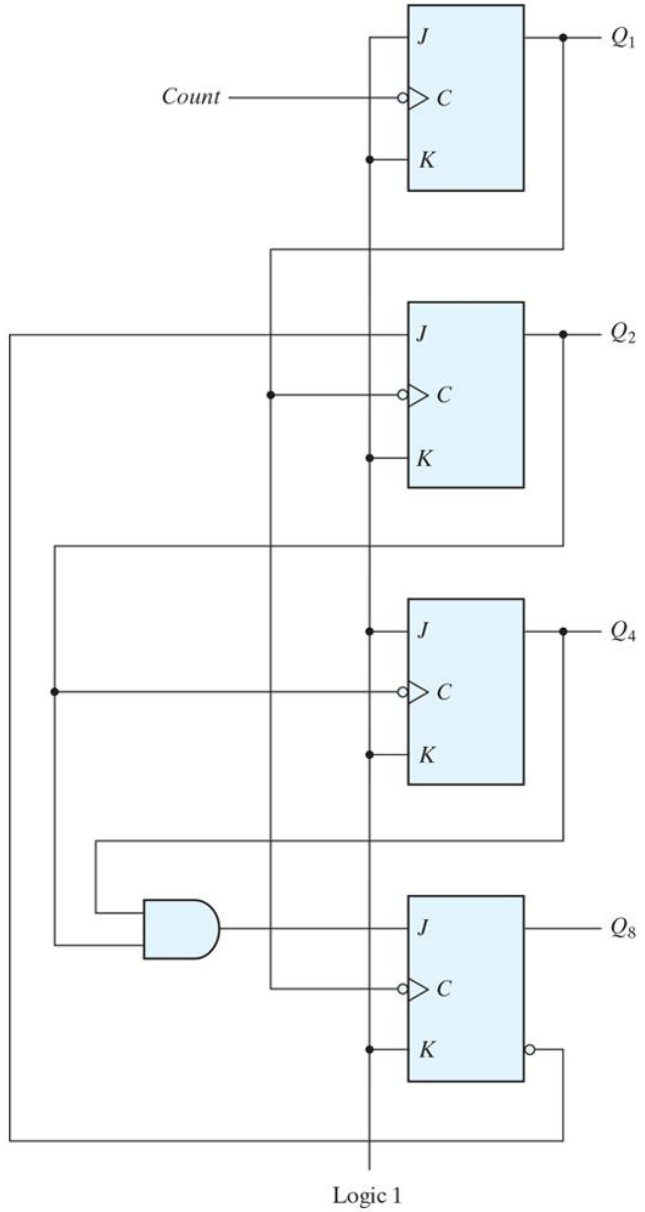


# BCD Ripple Counter

- Logic circuit:
- What does this circuit tell?
  - When are the each Flip-flop triggered?
  - Do you remember the JK flip-flop characteristic table?

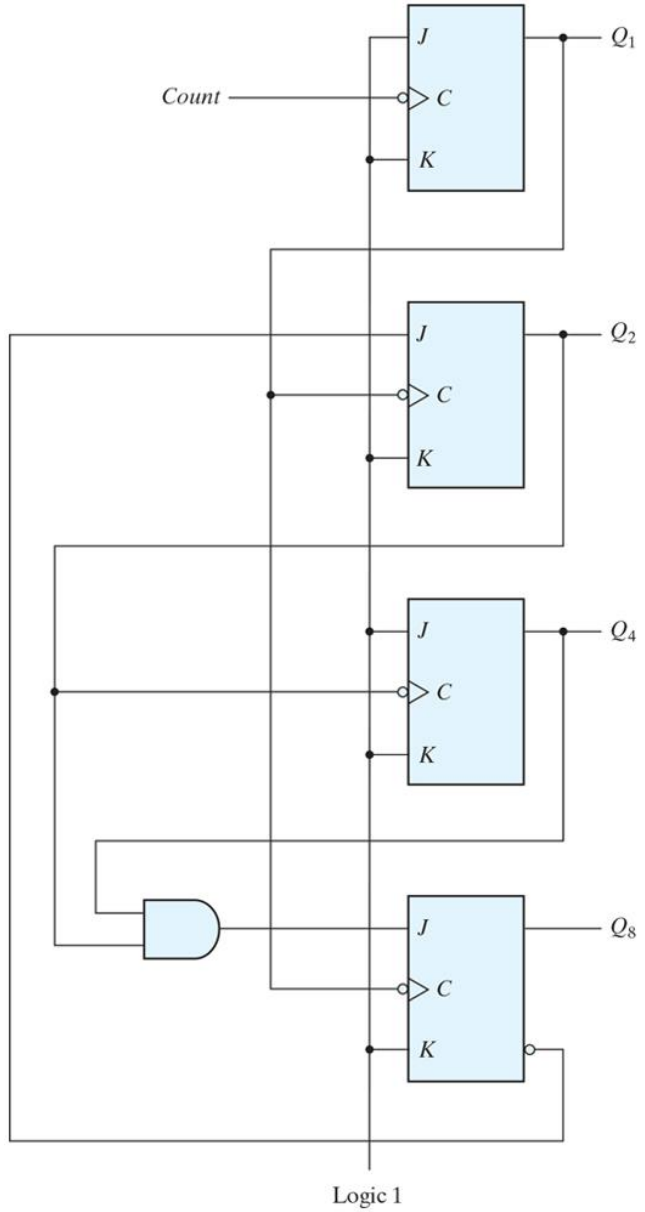
| *JK* Flip-Flop | | | |
|---|---|---|---|
| ***J*** | ***K*** | ***Q*(*t* + 1)** | |
| 0 | 0 | $Q(t)$ | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | $Q'(t)$ | Complement |

  - It is an asynchronous sequential circuit, can not be designed in the same way as the synchronous sequential circuits.



# BCD Ripple Counters

- State transition conditions for each flip-flop:
  1. $Q_1$ is complemented at each negative edge of the counr signal.
  2. If $Q_8$=0 and $Q_1$ goes from 1 to 0 $Q_2$is complemented. If $Q_8$=1 and $Q_1$ goes from 1 to 0 $Q_2$ is reset to 0.
  3. If $Q_2$ goes from 1 to 0 $Q_4$ is complemented.
  4. If $Q_4Q_2$=11 and $Q_1$ goes from 1 to 0 $Q_8$ is complemented. If either $Q_4$ or $Q_2$ is 0 and $Q_1$ goes from 1 to 0 $Q_8$ is reset to 0.



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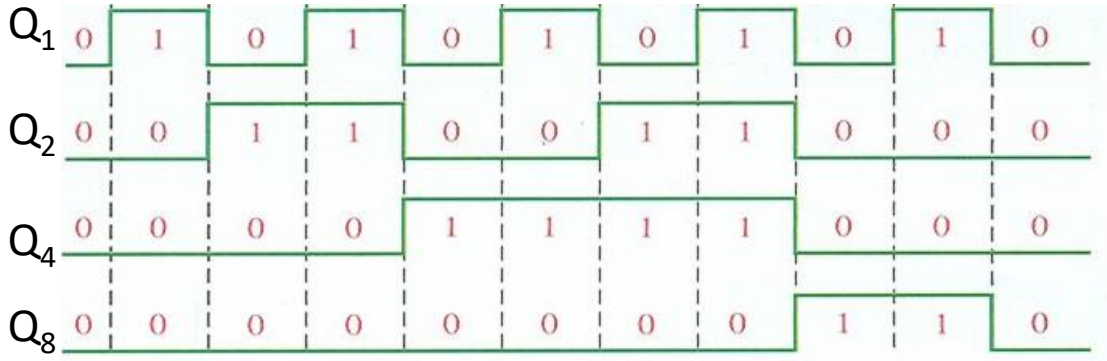
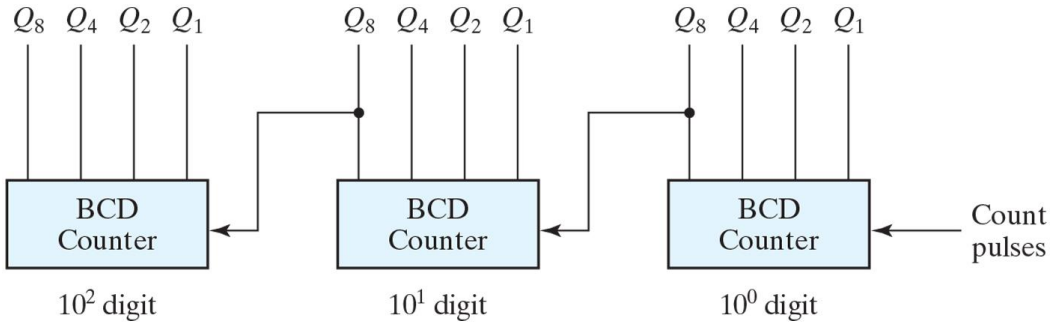


# BCD Ripple Counter

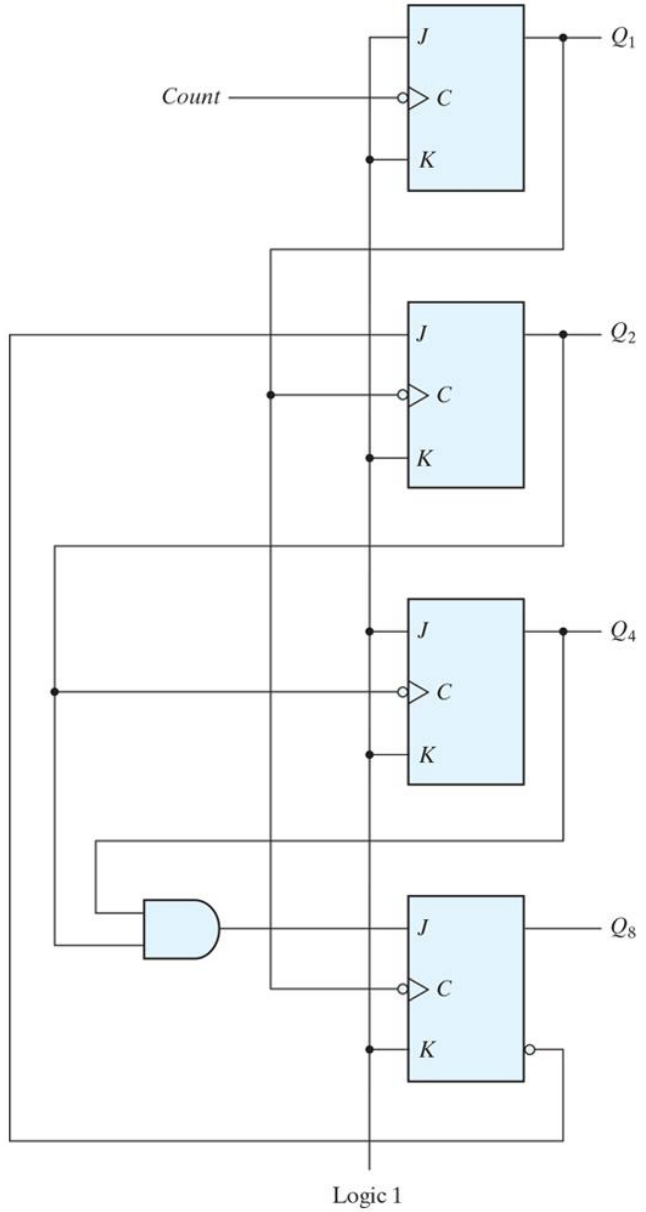
- The counter counts from 0 to 9.
- How to count from 0 to 99:
  - Need two bcd ripple counters
- How to count from 0 to 999:
  - Need three bcd ripple counters.
- Need as many counters as the number of digits.
- The $Q_8$ output of the previous counter is applied as the count pulse to the counter at a higher digit.
- When $Q_8$ goes from 1 to 0 the content of counter goes from 9 to 0 and the counter at the higher order is triggered to start counting. Example: 399→ 400



# Problem

- Which states are the unused states in a BCD Ripple Counter? Determine the next state for each of the unused state. Can the counter correct itself?

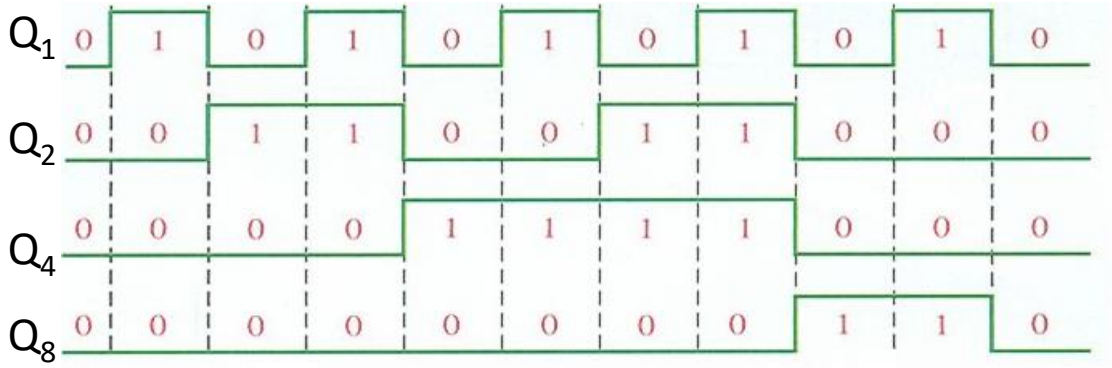
1. $Q_1$ is complemented at each negative edge of the counr signal.
2. If $Q_8$=0 and $Q_1$ goes from 1 to 0 $Q_2$is complemented. If $Q_8$=1 and $Q_1$ goes from 1 to 0 $Q_2$ is reset to 0.
3. If $Q_2$ goes from 1 to 0 $Q_4$ is complemented.
4. If $Q_4Q_2$=11 and $Q_1$ goes from 1 to 0 $Q_8$ is complemented. If either $Q_4$ or $Q_2$ is 0 and $Q_1$ goes from 1 to 0 $Q_8$ is reset to 0.



# Problem..

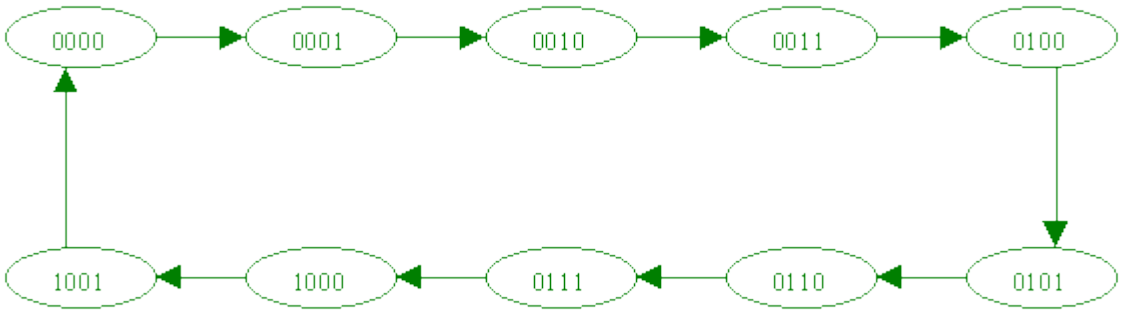
- Unused states: 1010,1011,1100,1101,1110,1111
- Properties of the circuit:
  1. $Q_1$ is complemented at each negative edge of the counr signal.
  2. If $Q_8$=0 and $Q_1$ goes from 1 to 0 $Q_2$is complemented. If $Q_8$=1 and $Q_1$ goes from 1 to 0 $Q_2$ is reset to 0.
  3. If $Q_2$ goes from 1 to 0 $Q_4$ is complemented.
  4. If $Q_4Q_2$=11 and $Q_1$ goes from 1 to 0 $Q_8$ is complemented. If either $Q_4$ or $Q_2$ is 0 and $Q_1$ goes from 1 to 0 $Q_8$ is reset to 0.

| Şimdiki Durum | | | | Sonraki Durum | | | |
|---|---|---|---|---|---|---|---|
| Q8 | Q4 | Q2 | Q1 | Q8 | Q4 | Q2 | Q1 |
| 1 | 0 | 1 | 0 | | | | |
| 1 | 0 | 1 | 1 | | | | |
| 1 | 1 | 0 | 0 | | | | |
| 1 | 1 | 0 | 1 | | | | |
| 1 | 1 | 1 | 0 | | | | |
| 1 | 1 | 1 | 1 | | | | |



- Can the counter correct itself?

| Present State | | | | Next State | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |



# References


- Morris Mano, Digital Design, 2nd edition