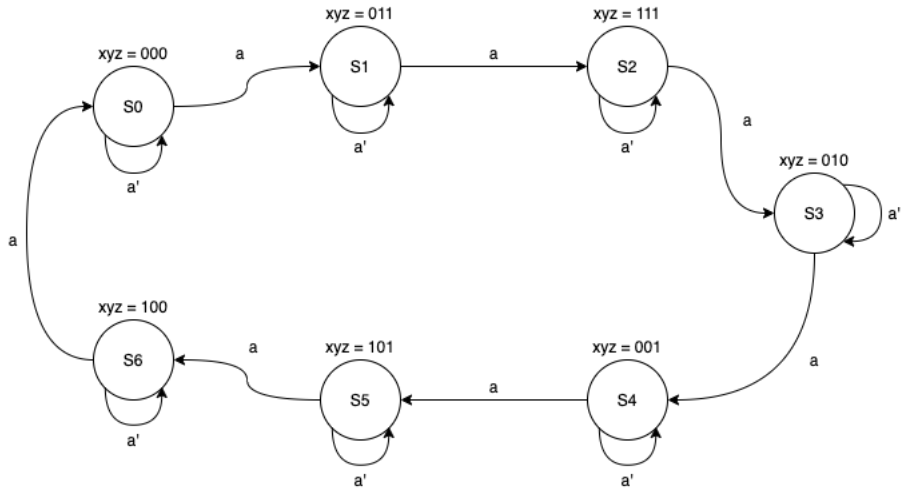
Step 1



Step 2

7 states (3 bits registers)
3 bits for coming states
a is input
x, y, z are output

Step 3

S0 = $\neg s_2 \neg s_1 \neg s_0$
S1 = $\neg s_2 \neg s_1 s_0$
S2 = $\neg s_2 s_1 \neg s_0$
S3 = $\neg s_2 s_1 s_0$
S4 = $s_2 \neg s_1 \neg s_0$
S5 = $s_2 \neg s_1 s_0$
S6 = $s_2 s_1 \neg s_0$

Step 4

inputs				outputs					
s_2	s_1	s_0	a	x	y	z	n_2	n_1	n_0
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	0	1	1	0	1	0
0	1	0	0	1	1	1	0	1	0
0	1	0	1	1	1	1	0	1	1
0	1	1	0	0	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
1	0	0	0	0	0	1	1	0	0
1	0	0	1	0	0	1	1	0	1
1	0	1	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	1	0
1	1	0	0	1	0	0	1	1	0
1	1	0	1	1	0	0	0	0	0
1	1	1	0	Don't care condition					
1	1	1	1	Don't care condition					

Step 5

Kmap for x

s_2s_1 \ s_0a	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	1	1	x	x
10	0	0	1	1

$\implies$ x = $s_1\neg s_0 + s_2 s_0$

Kmap for y

s_2s_1 \ s_0a	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	0	0	x	x
10	0	0	0	0

$\implies$ y = $\neg s_2 s_1 + \neg s_2 s_0$

Kmap for z

s_2s_1 \ s_0a	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	0	0	x	x
10	1	1	1	1

$\implies$ z = $s_2\neg s_1 + \neg s_2\neg s_1 s_0 + \neg s_2 s_1\neg s_0$

Kmap for n_2

s_2s_1 \ s_0a	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	0	x	x
10	1	1	1	1

$\implies n_2 = s_2\neg s_1 + s_2\neg s_0\neg a + s_1 s_0 a$

Kmap for n_1

s_2s_1 \ s_0a	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	0	x	x
10	0	0	1	0

$\implies n_1 = \neg s_1 s_0 a + \neg s_2 s_1\neg s_0 + s_1\neg s_0\neg a + s_1 s_0\neg a$

Kmap for n_0

s_2s_1 \ s_0a	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	0	x	x
10	0	1	0	1

$\implies n_0 = s_0\neg a + \neg s_2\neg s_0 a + \neg s_1\neg s_0 a$

Logic Circuit