1 Question 1

1.1

A	B	C	D	$minterms$	
0	0	0	0	$\neg A\neg B\neg C\neg D$	(m_0)
0	0	0	1	$\neg A\neg B\neg CD$	(m_1)
0	0	1	0	$\neg A\neg BC\neg D$	(m_2)
0	0	1	1	$\neg A\neg BCD$	(m_3)
0	1	0	0	$\neg AB\neg C\neg D$	(m_4)
0	1	0	1	$\neg AB\neg CD$	(m_5)
0	1	1	0	$\neg ABC\neg D$	(m_6)
0	1	1	1	$\neg ABCD$	(m_7)
1	0	0	0	$A\neg B\neg C\neg D$	(m_8)
1	0	0	1	$A\neg B\neg CD$	(m_9)
1	0	1	0	$A\neg BC\neg D$	(m_{10})
1	0	1	1	$A\neg BCD$	(m_{11})
1	1	0	0	$AB\neg C\neg D$	(m_{12})
1	1	0	1	$AB\neg CD$	(m_{13})
1	1	1	0	$ABC\neg D$	(m_{14})
1	1	1	1	$ABCD$	(m_{15})

1.1.a

$F_1(A,B,C,D) = \Sigma m(0,1,4,5,8,9,10,12,13)$

AB \ CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	1	1	0	0
10	1	1	0	1

$$F_1(A,B,C,D) = A\neg B\neg D + \neg C$$

1.1.b

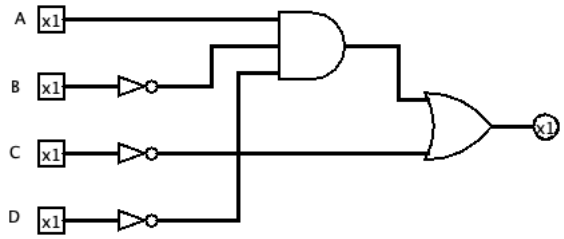
$F_2(A,B,C,D) = \Sigma m(3,5,7,8,9,10,11,13,15)$

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	1	1	0
11	0	1	1	0
10	1	1	1	1

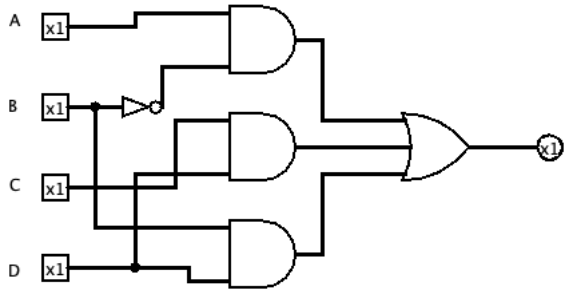
$$F_2(A,B,C,D) = A\neg B + BD + CD$$

1.2

Logic circuit of F_1

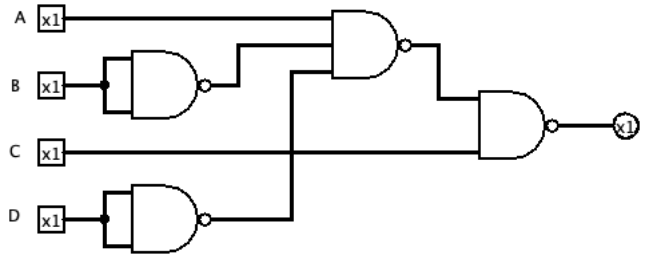


Logic circuit of F_2

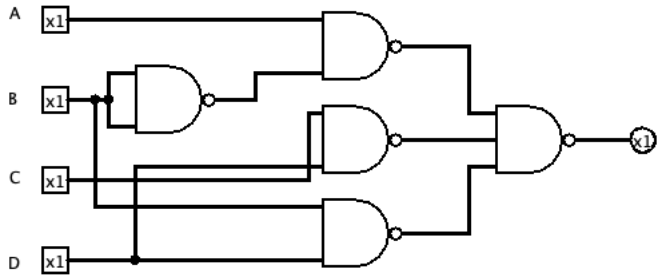


1.3

Logic circuit of F_1 with only NAND gate



Logic circuit of F_2 with only NAND gate



2 Question 2

2.1

$$F = A\neg B(C+\neg C)(D+\neg D) + AD(B+\neg B)(C+\neg C) + BC(A+\neg A)(D+\neg D) + C\neg D(A+\neg A)(B+\neg B) + \neg A\neg B\neg C\neg D$$
$$= A\neg BCD + A\neg BC\neg D + A\neg B\neg CD + A\neg B\neg C\neg D + ABCD + AB\neg CD + ABC\neg D + \neg ABCD + \neg ABC\neg D + \neg A\neg BC\neg D + \neg A\neg B\neg C\neg D$$

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

2.2

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	0	1	1	1
10	1	1	1	1

2.3

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	0	1	1	1
10	1	1	1	1

$$F = \neg B\neg D + BC + AD$$

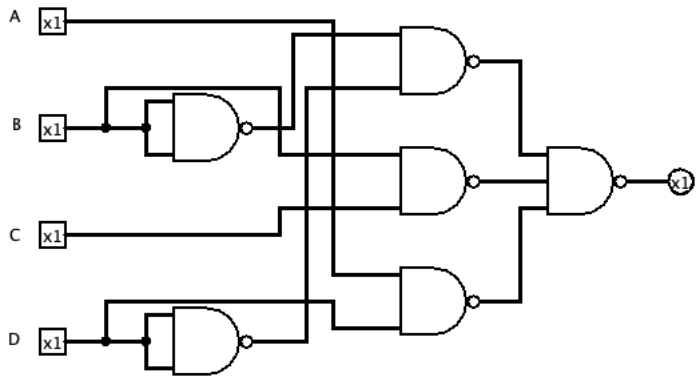
2.4

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	0	1	1	1
10	1	1	1	1

$$\neg F = \neg A \neg B D + \neg A \neg C D + B \neg C \neg D$$

2.5

Logic circuit of F



Logic circuit of $\neg F$