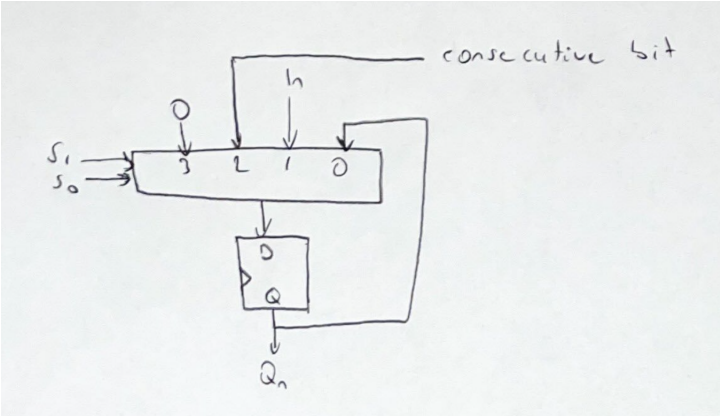
Step 1

4 operations: maintain, load, swap, clear
→ 4x1 mux

Step 2

s1	s0	Operation
0	0	Maintain
0	1	Load
1	0	Swap
1	1	Clear

Step 3



Step 4

inputs			outputs		
cl	ld	sw	s_1	s_0	operations
0	0	0	0	0	maintain
0	0	1	1	0	swap
0	1	x	0	1	load
1	x	x	1	1	clear

$s_1 = \text{cl} + \neg\text{cl}.\neg\text{ld}.\text{sw}$
$s_0 = \text{cl} + \neg\text{cl}.\text{ld}$

Logic Circuit