FPGA-based high-precision network time synchronization research and Implementation

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Abstract: *This study is based on the 1588 network clock synchronization technology. Clock synchronization of distributed systems is a very important element in the communications, automation, and testing equipment especially for the current LXI Bus. Now there are some synchronization protocols like NTP. But it just has millisecond synchronization accuracy. In many areas such as instrument system, that accuracy is not enough. Therefore, higher synchronization accuracy is required. This paper presents a model for high accuracy of the clock, detailed analysis of the factors that affect clock synchronization and proposed to solve the key technology and solution. These technologies not only changed the clock operation mode, but also access to technology to improve the timestamp. The results show that the synchronization accuracy can be achieved nanosecond.*
Keywords: *IEEE1588; clock synchronization; ABC Clock*

I. INTRODUCTION

A characteristic of distributed systems is the use of different spatial distribution of the processor, through the network to exchange information, to complete certain functions of the system. Application of distributed systems is now more popular, such as: process control, instrumentation, aerospace and so on. Time coordination of distributed systems is critical, a common practice is to establish a net-based, arrange all the distributed nodes are synchronized to a master clock.

IEEE 1588 clock synchronization algorithm is designed on this principle. Clock synchronization has a lot of difficulties. First of all, the information transmission delay is variable, a processor can not immediately know the distance of each clock value. Secondly, even if all the clocks began at the same time, the drift rate problem still existed. The processors cannot always keep pace. In addition, the drift rate will change due to aging and temperature changes. Therefore, clock synchronization problem analysis and research has important practical significance.

IEEE 1588 Precision Time Synchronization Protocol (PTP) can achieve accurate clock synchronization by network communication. IEEE1588 can support multicast network particularly suitable for Ethernet architecture in industrial distributed control system. Software-based solution due to the network delay instability, the crystal frequency drift, the interrupt service routine response time constraints and other factors difficult to achieve nanosecond level synchronization accuracy. This paper describe a method of IEEE1588 synchronization algorithm which based on FPGA implementation of the sub-microsecond synchronization accuracy to meet High real-time, high-precision synchronization requirements.

II. IEEE 1588 ANALYSIS

A. The mathematical model of the clock synchronization

Set nodes in a distributed system is P clock function, T is the actual time or master clock time, $p(t)$ is defined relative to the maximum offset.

$$\left|c_p(t) - T\right| = p(t) \qquad \forall t = t_0 \tag{1}$$

If $p(t)$ =0, called master-slave clock is fully synchronized. An absolute synchronization does not exist in reality. Therefore, the actual in the master-slave clock synchronization to be required as small as possible and limited to a certain range, so the definition of synchronization accuracy α, requirements $\left|p(t)\right| \le \alpha$ .According to the formula (1), to make the master-slave clock synchronization need to determine the clock offset $p(t)$ from the master clock.

But in the actual network transmission formula (1) there is two problems:

Question 1: In the actual network transmission, the formula (1) T contains a network of time-related delays, defined as $d_\varepsilon(t)$ so the formula (1) should instead as follows:

$$\left|c_p(t) - (T + d_\varepsilon(t))\right| \le \alpha \tag{2}$$

$d_\varepsilon(t)$ as a time variable, so to keep within a certain range.

Question 2: For the impact of environmental conditions, the node will have certain long-running clock frequency drift, which will affect the clock synchronization. Here we define the clock frequency drift rate ρ sec/SEC, the formula (2) to be instead equation (3).

$$\left|c_p(t)\rho - (T + d_\varepsilon(t))\right| \le \alpha \tag{3}$$

Definition of clock rate $\nu_p(t) = dc_p(t)/dt$

Ideally $\nu_p(t) = 1$, so Frequency drift ρ is defined relative to the deviation of the ideal rate of 1 , for the

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low-cost network nodes crystal, generally there $\rho_{ma,x} \in [10,100]$ ppm. From formula (3) can be seen, to meet the nanosecond clock synchronization accuracy, we must do three things:

(1) calculate network latency and keep the delay constant;

(2) clock drift ρ compensation;

(3) calculate the synchronization offset $p(t)$

while meeting the synchronization accuracy ;

B . Process Analysis of IEEE 1588

In the PTP synchronization algorithm, the network packet information includes time information and on each information with the time stamp. With timestamp, the receiver can calculate its own clock error and delay.

PTP protocol defines four types of information: Sync, Follow_Up, Delay_Req, and Delay_Resp, from each network node by exchanging synchronization information to synchronize.

Synchronization process is divided into two stages, the first stage shown in Figure 1, computing time from the clock offset.

In the first stage, the master clock Sync message sent periodically (usually once every two seconds), it contains the required master clock properties. Sync information is includes a timestamp, an accurate description of the expected time of packets sent.

Because the time information is contained in the network packet and not the real issue of time, so the master clock sent the true time Sync information TM1 in the subsequent Follow_Up which sent to the slave clock. And slave nodes recorded real time TS1. With TM1 and TS1, the slave can calculate the time difference from the master clock , and correct the slave clock. If there is no delay in the transmission path, and now the two clock synchronization.

The second phase of the synchronization process is the network delay measurements, shown in Figure 2.This stage measure the network delay from the master clock. Slave clock in the TS3 issued Delay_Req, Master clock at the time of receipt of the TM3, then issue Delay_Resp, which include the TM3 .With TS3 and TM3, Slave nodes calculated network delay from the master.

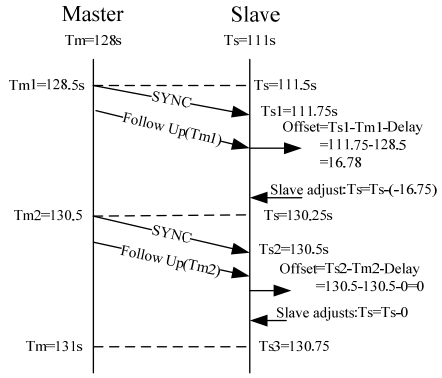

Fig. 1 Offset calculation

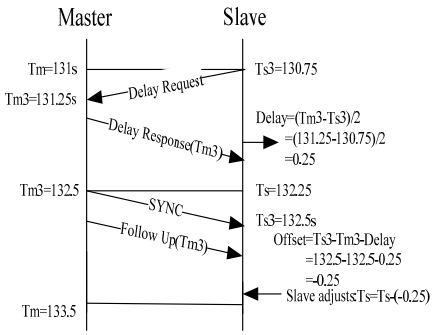

Fig .2 Delay calculation

C. Defects of the algorithm

According to the 1588 description, the algorithm calculate network synchronization delay, deviation from the clock $p(t)$. However, the algorithm by default the network delay is constant, in the software-based clock synchronization scheme, the time stamp for the general MAC layer from the network, it would be impact the network delay of master-slave clock , so the calculation of network delay is uncertain. Therefore algorithm does not solve the problem of network delay constancy.

Commonly due to counter of CPU is unstable, with the drift changes in objective circumstances, such as temperature, vibration and other external conditions, so system calculated arrival time of network packets is uncertain. 1588 did not solve the equation (3) referred to the symmetry of the network delay and clock skew problems.

III. FPGA-BASED HARDWARE-ASSISTED ALGORITHM FOR CLOCK SYNCHRONIZATION

According to the formula (2), a fundamental condition of the network clock synchronization is constant network delay as possible, that is $|d_\varepsilon| \le \gamma$, such a synchronization model usually referred to as bounded delay model. To achieve this purpose,

Therefore, the overall design of the hardware shown in Figure 3.we use Cirrus Logic's EP9315 CPU. The FPGA mainly the identification and capture network packed at the PHY layer. So network latency can regarded as constant. Adder-based ABC (Adder Base Clock) can compensate for clock drift.

Therefore, the design of tasks is the key technology of the program.

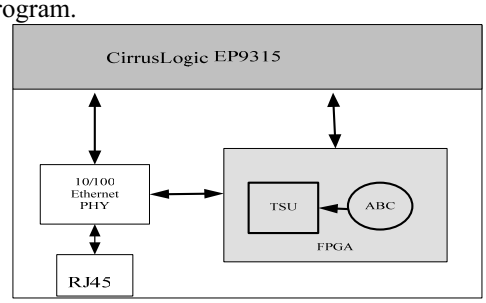

Fig. 3 Hardware Design

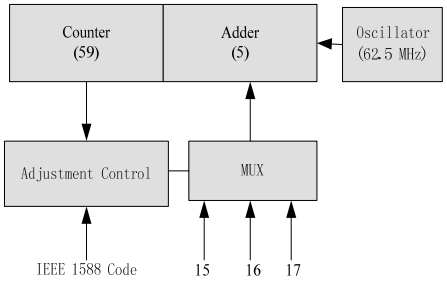

Fig. 4 ABC clock

A. Adder-Based Clock Technology

In an ordinary crystal-driven counters, because of the crystal in the temperature and pressure changes in circumstances, in general, ± 100ppm of the error, so if in the system to use ordinary crystal to record the time value would be bound to impact on the synchronization precision. Therefore, the clock should be adjusted. There are many ways the clock adjustment, mainly in the following three:

1. using VCO to adjust the clock;
2. Using software algorithms regulation;
3. Used to adder adjust clock

Among them, using the method of VCO is difficult, and the cost is relatively high. Adjusted by software algorithms have great random error, adjust the clock by the adder is relatively straightforward and easy to implement, so we design the adder in FPGA implement clock adjustment, the principle shown in Figure 4.

In the FPGA, design a 64 bit counter, a 5-bit adder, a 62.5MHz clock, calibration control unit and the selector. Designed digital clock frequency of 62.5MHz, under normal circumstances, MUX selection of 16, each clock cycle through the adder plus 16, then the adder maximum bit is 1, equivalent to generate a carry, then the counter plus 1.Under the 1588 agreement, each second FPGA to capture a timestamp, according to the timestamp, 1588 algorithm adjust the value of the MUX. For example, if the clock fast 10ns, MUX would be set 15, as opposed to the normal value of 16, the clock is slow 10ns. This way effective compensates the clock drift ρ .

B 1588 stamp interception

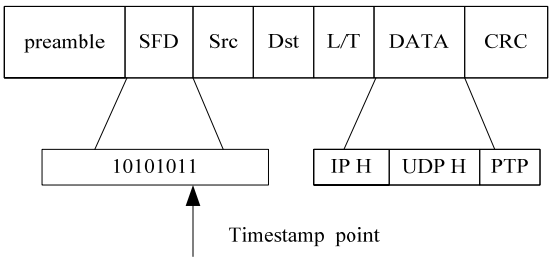

Fig.5 1588 timestamp format

The format of the data packet 1588 shown in Figure 5.in the 1588 clock synchronization algorithm, the key factor is the constant of network latency and network symmetry, so the capture 1588 data packet timestamp as close as possible to the bottom of the network protocol, that is, PHY layer, so the design scheme, the time stamp interception on the MII (media independent layer), FPGA detect each packet after the SFD unit, and records the current count value, which as PTP timestamp.

IV. RESULT

Verification of clock synchronization mainly use two methods, the first way generates a pulse per second (commonly referred as 1PPS), which is fed to the input of an oscilloscope to compare the time deviation of the two nodes. The second way use the formula $\left|c_p(t)-T\right|=p(t)$ .In the master and slave nodes to run for some time, computation $\left|p(t)\right|$, and statistical synchronization accuracy α.This paper described experimental by the second method.

The test hardware consists of two nodes, PC computer within the NI 1588 sync card, which built-in TXCO can be used as the master clock, and other node with EP9315 processor, built-in self-designed FPGA clock unit, as slave clock. The latter is used for running a IEEE1588 compatible synchronization stack. The FPGA implements an Adder Based Clock synchronization core with the modified timestamp units as described in the previous section, the synchronization interval was set to 1 second, all data communications between nodes via Ethernet to complete.

By experimental time of 2 hours, the number of 3990 data. In figure 6, histogram of the horizontal axis represents the synchronization deviation from the master node and slave node, and the vertical axis represents the distribution of $\left|p(t)\right|$. It can be seen from the figure, the synchronization accuracy $\alpha\in[-100,100]$, meet the design requirements between point to point.

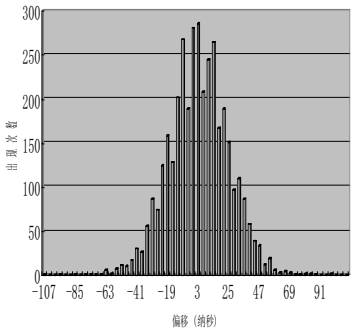

Fig. 6 Histogram of data synchronization

V. CONCLUSION

Precision clock synchronization of distributed systems by many aspects, but one of the most important factor is the stability of the crystal, there are several ways to

improve, but the most direct way is to use ABC clock design. This design method can effectively adjust the clock drift. Next, clock synchronization algorithm could be impacted by the asymmetry of the network. In this way, network data packets arrive timestamp could be captured in network PHY layer. This method could eliminate the impact of asymmetry.

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