Computer Organization Lab 4

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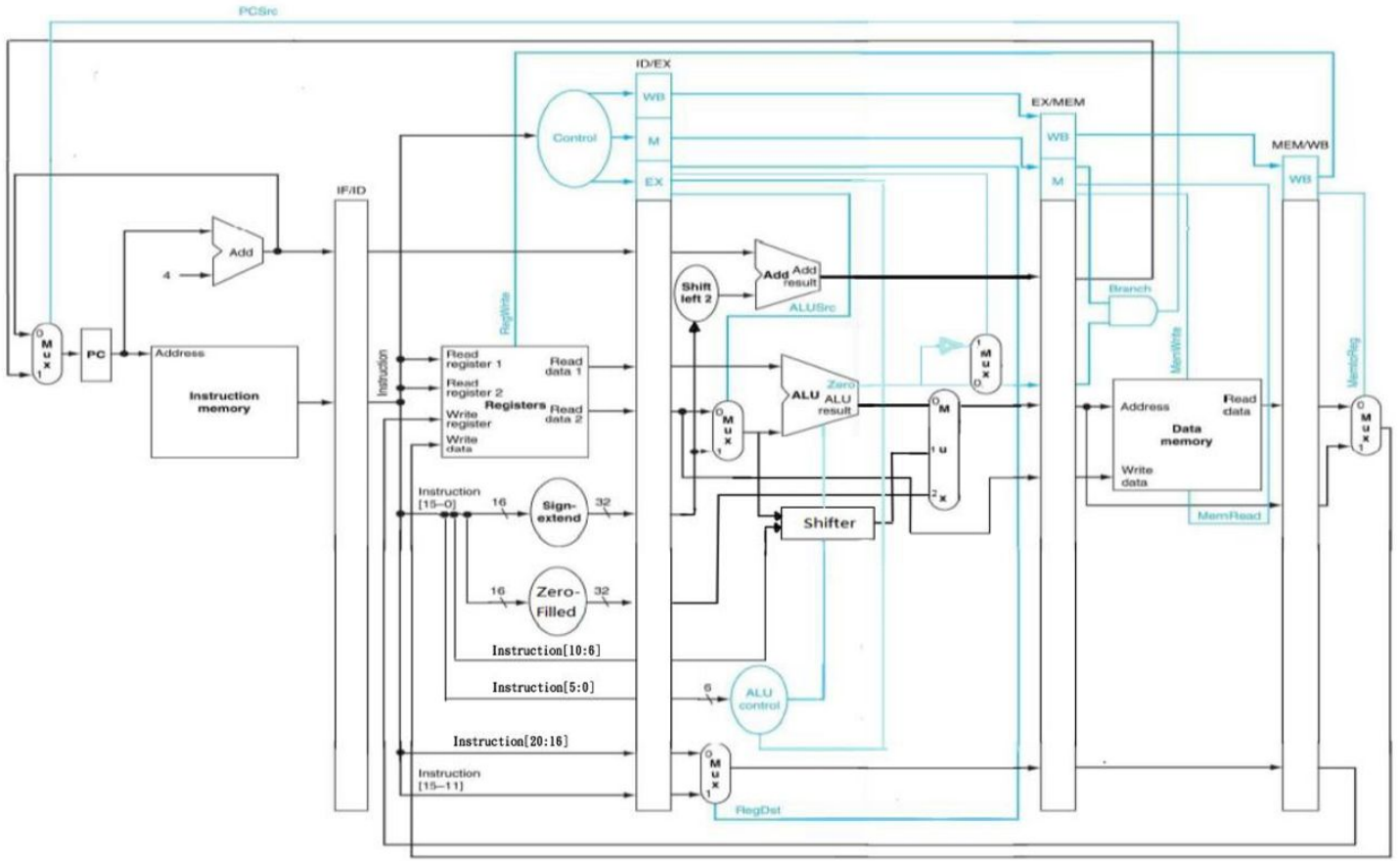
Objective

In this lab, we are going to modify the single cycle processor designed in previous lab to a pipelined processor.

Pipelined CPU Architecture Diagram(1/2)(80%)



Pipelined CPU Architecture Diagram(2/2)

- According to the previous diagram, we are going to implement a five stage pipelined processor with **IF, ID, EX, MEM, and WB** stages.
- You should insert a pipeline register between each two stages.
- Each pipeline register should contain the fields for data and control signals.
- The pipeline registers are written when the positive clock edge occurs.
- It should be no operation when read nop instruction(32'b0).
- Rename Simple_Single_CPU.v to Pipeline_CPU.v

Pipeline Register Description

- Please design four pipeline registers. Each pipeline register must be “**positive edge triggered**”, and has default value 0.
- Insert these pipeline registers into your single-cycle CPU designed in Lab4 to accomplish the pipelined CPU required in this lab.
- **Do not** set any delay time for the sequential circuits of the pipelined registers designed by you.

Report(20%)

There’s no restriction about the report format, but please answer the following questions:

1. Describe the input fields of each pipeline register(10%)
2. Explain your control signals in the **sixth cycle(**both test data test_1.txt and test_2.txt are needed**)**(10%)

Demands

- Please use **iverilog** as your HDL simulator.
- Reg_file(postive edge triggered), Programm_Counter, and TestBench are supplied.
- Please use these modules and modules in Lab3 to accomplish the design of your CPU
- For each pipeline register, it should contain the fields for **data and control signals**.

Test

- We will test the following instructions:
  - **add, sub, and, or, nor, slt, sll, srl, addi, lw, sw**
- There are 2 test files, test_1.txt and test_2.txt.

Submission

- Compress all the ***.v files and HW4_{studentID}.pdf** into one zip file, and name your zip file as **HW4_{studentID}.zip (e.g. HW4_0811510.zip)**
- **Wrong format will have 10% penalty.**
- **Any assignment work by fraud will get a zero point.**
- **No late submission (deadline: 8/16 23:55)!**