Digital Circuit Design
數位電路設計

Jean Shann (單智君)
Dept. of Computer Science
NCTU
Spring 2022

J.J. Shann

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Class

- Class:
  - 2-hour in-person/on-site class: Wed. 34 (EC122)
    - *** On-line class for the first two weeks by google meet!**
    - Google meet: https://meet.google.com/wsu-mbhr-hxy
  - 1-hour/2-hour asynchronous on-line class:
    - Course Video

(每週 兩小時實體課程 + 一或兩小時非同步線上課程)

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Office & Office Hour
♦ Office:
EC516, ext. 31832
e-mail: jjshann@cs.nctu.edu.tw (or e3)
♦ Office Hours:
Wed. 1:30PM~3:00PM
Google meet: https://meet.google.com/wsu-mbhr-hxy
(or making an appointment via e-mail)

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Teaching Assistant & TA Hours
♦ 陳芷羚學姐 vivian96385@gmail.com
– Mon. 6:30PM~8:30PM
– Google meet: https://meet.google.com/nde-caut-ozp
♦ 潘冠蓁學姐 pennypan644@gmail.com
– Tue. 6:30PM~8:30PM
– Google meet: https://meet.google.com/kxy-rgcr-sqy
♦ 李璨宇學長 frank.cs08@nycu.edu.tw
– Thur. 6:30PM~8:30PM
– Google meet: https://meet.google.com/fko-zkfn-raz
* May set up an appointment via e-mail

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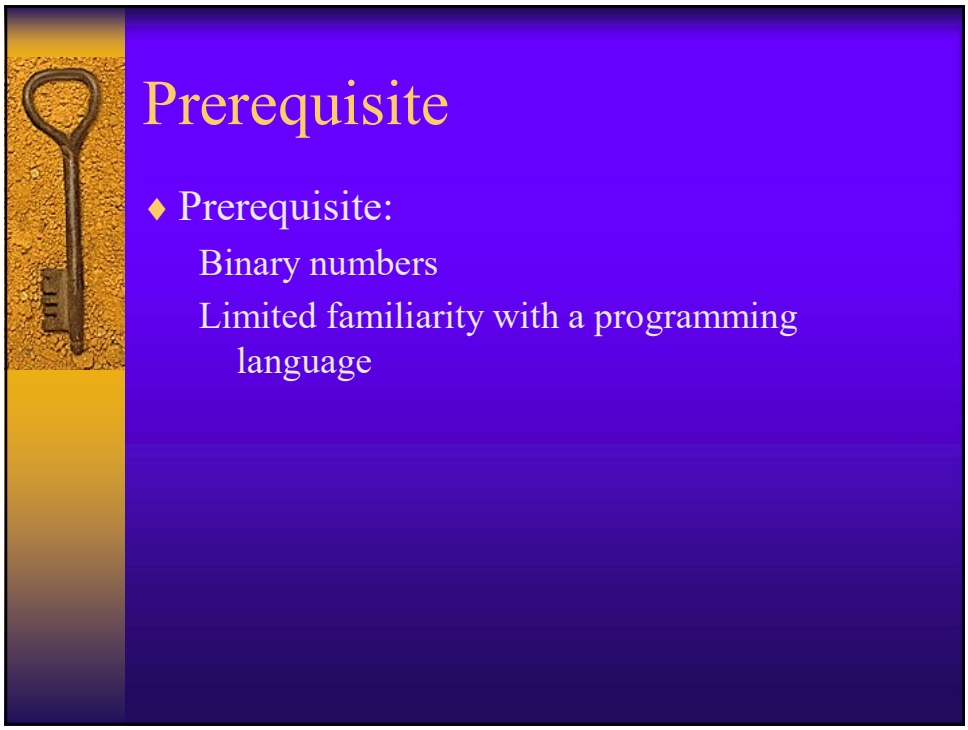
Prerequisite
♦ Prerequisite:
Binary numbers
Limited familiarity with a programming language

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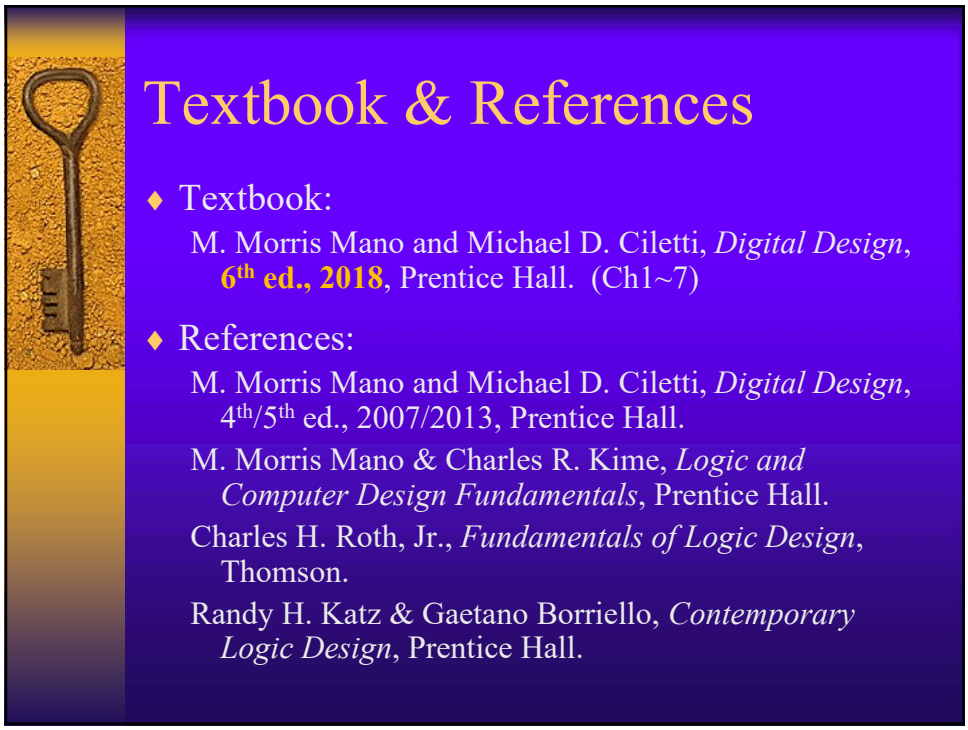
Textbook & References
♦ Textbook:
M. Morris Mano and Michael D. Ciletti, Digital Design, 6th ed., 2018, Prentice Hall. (Ch1~7)
♦ References:
M. Morris Mano and Michael D. Ciletti, Digital Design, 4th/5th ed., 2007/2013, Prentice Hall.
M. Morris Mano & Charles R. Kime, Logic and Computer Design Fundamentals, Prentice Hall.
Charles H. Roth, Jr., Fundamentals of Logic Design, Thomson.
Randy H. Katz & Gaetano Borriello, Contemporary Logic Design, Prentice Hall.

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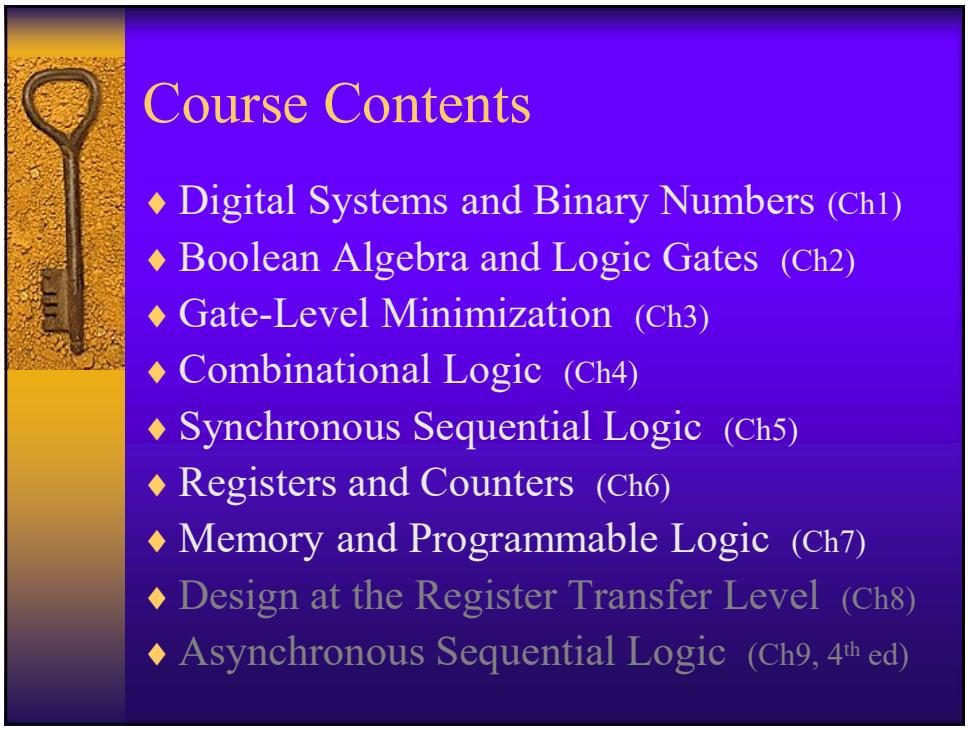
Course Contents
♦ Digital Systems and Binary Numbers (Ch1)
♦ Boolean Algebra and Logic Gates (Ch2)
♦ Gate-Level Minimization (Ch3)
♦ Combinational Logic (Ch4)
♦ Synchronous Sequential Logic (Ch5)
♦ Registers and Counters (Ch6)
♦ Memory and Programmable Logic (Ch7)
♦ Design at the Register Transfer Level (Ch8)
♦ Asynchronous Sequential Logic (Ch9, 4th ed)

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Grading Policy & Course Information
* Adjust flexibly in response to the epidemic of COVID-19!
♦ Grading Policy:
– Examinations: 3, 60% ~ 80%
* The 6th, 11th, 16th weeks
(3/23 Wed. 34) (4/27 Wed. 34) (6/1 Wed. 34)
– Lab Units/Quizzes/Homework: 20% ~ 40%
• Lab Units: 3~4 (Verilog)
• Quizzes: 8~10 (?)
• Homework: ... (?)
– Participation/Advancement
♦ Course Information:
https://e3.nycu.edu.tw (e3 數位教學平台)

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課程關聯–計算機硬體基礎課程
一上
一下
二上
二下
三上
Physics I
物理(一)
Physics II
物理(二)
Electronics I
電子學(一)
Physics Lab I
電子實驗(一)
Electronics II
電子學(二)
Physics Lab II
電子實驗(二)
Digital Circuit Design
數位電路設計
Digital System Design
數位系統設計
Computer Organization
計算機組織
Digital Circuit Lab
數位電路實驗
Microprocessor System Lab
微算機系統實驗

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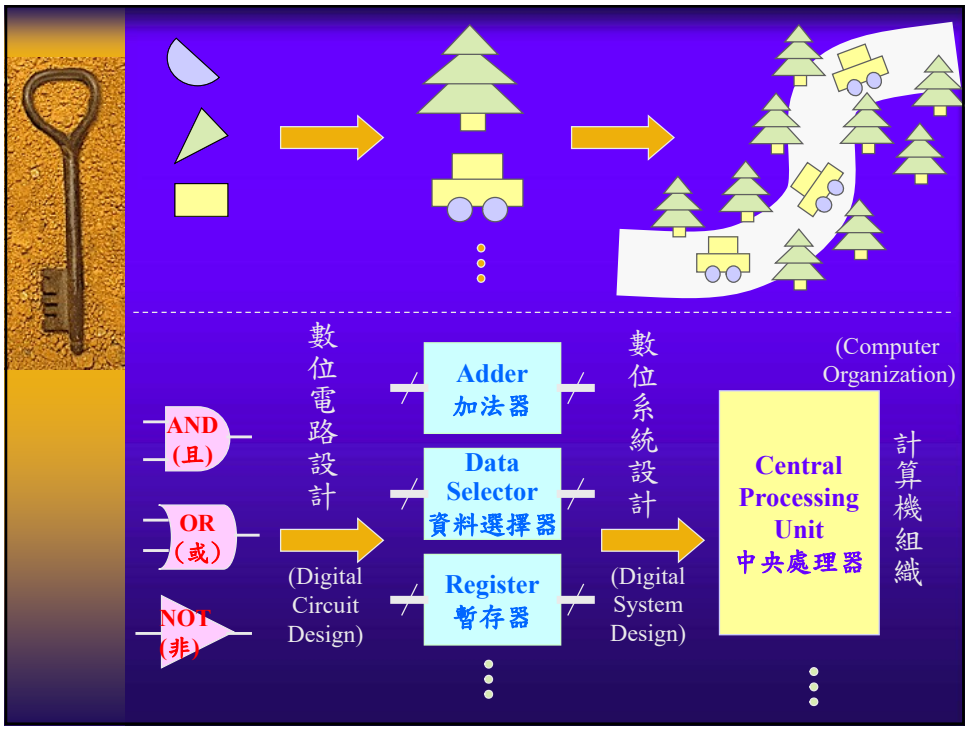
AND
(且)
OR
(或)
NOT
(非)
數位電路設計
(Digital Circuit Design)
Adder
加法器
Data Selector
資料選擇器
Register
暫存器
數位系統設計
(Digital System Design)
Central Processing Unit
中央處理器
(Computer Organization)
計算機組織

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Overview of Digital Circuits

- Combinational circuits
- Sequential circuits
  - Synchronous sequential circuits
  - Asynchronous sequential circuits

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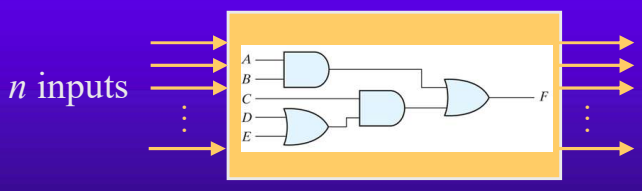
Combinational Circuits

- Combinational ckt: logic gates
  - It outputs at any time are determined from the present inputs. (no feedback paths or memory elements)

(inputs) $\Rightarrow$ (outputs)



- Examples:
  - Parallel adder, Encoder, Decoder, Multiplexer, …

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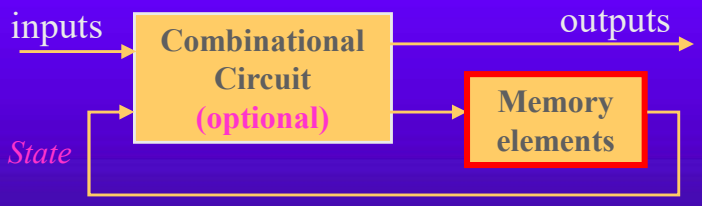
Sequential Circuits

- Sequential circuit:

  (inputs, present state) ⇒ (outputs, next state)



Memory elements: devices capable of storing binary information (*states*)

- Synchronous vs. Asynchronous
- Examples: Vendor machine, Serial adder, …

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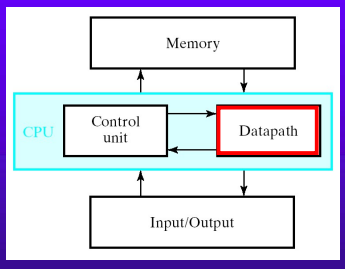
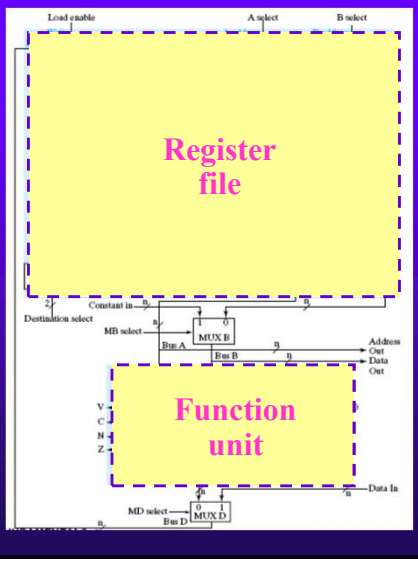
An Example of Digital Systems

- Digital computer:





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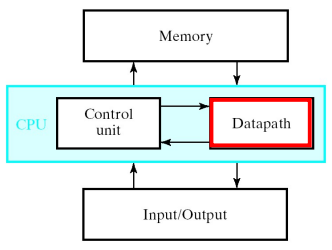
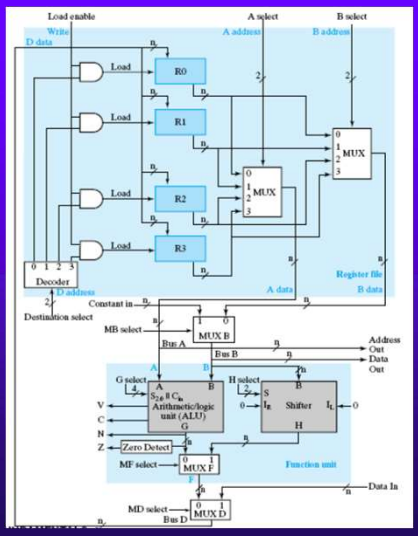
An Example of Digital Systems

- Digital computer:





Revolution in Hardware Design

- Pervasive use of software tools to assist in the process of hardware design
  - Hardware description language (HDL)
  - Computer-aided design tools
    - * Hardware design looks like software design
- Emergence of rapid implementation circuit technology
  - Programmable logic