Lab0：Verilog HDL 模擬器(Icarus Verilog 與 Vivado)之安裝與使用

(The Setup and Use of Verilog Simulators, Icarus Verilog and Vivado)

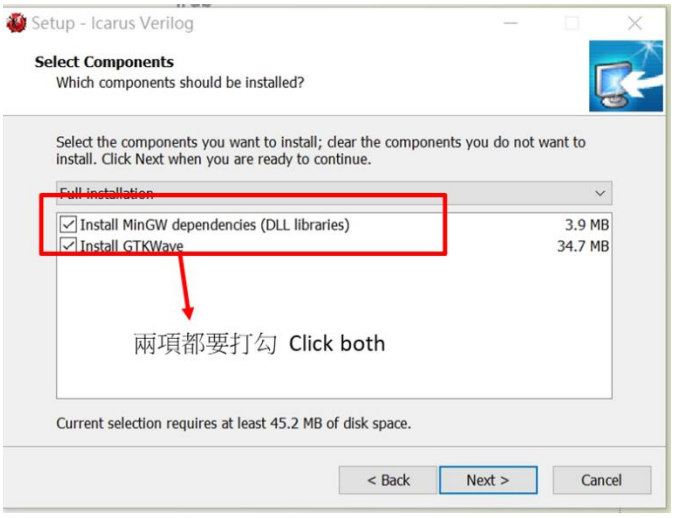
A. Icarus Verilog (iVerilog) & gtkwave

1. Windows 環境下的安裝 (Download under Windows system)

(a) 下載網址(Download here)：http://bleyer.org/icarus/ ∨ ∨

- ✓ 64 bit：iverilog-10.1.1-x64_setup.exe [9.77MB]
- ✓ 32 bit：iverilog-10.0-x86_setup.exe [11.1MB]

(b) 安裝步驟 (Installation Steps)



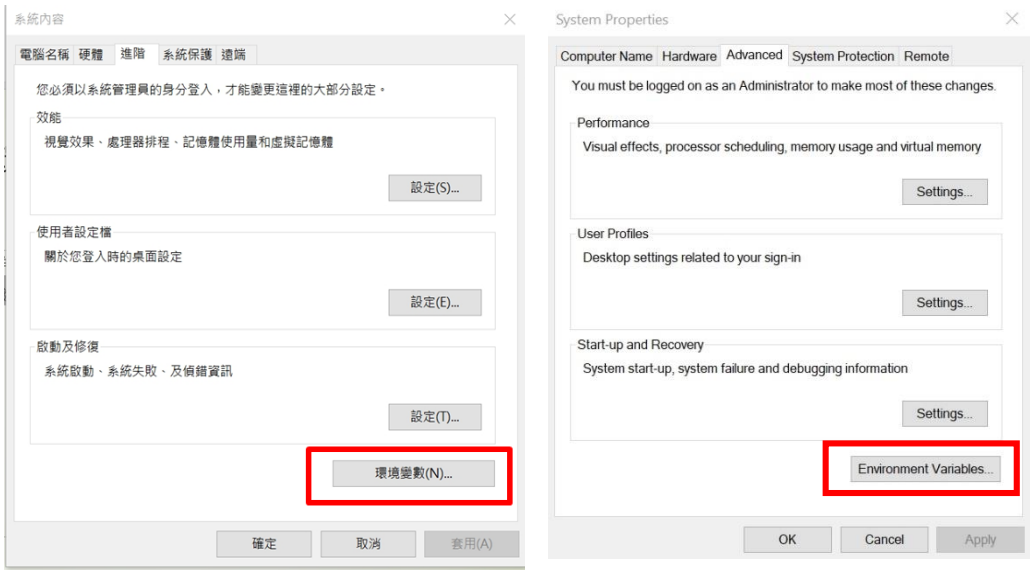
(c) 新增環境變數(Add Environment Variable)

i. 打開控制台 (System(Control Panel))

ii. 搜尋「進階系統設定」(search **Advanced system settings)**

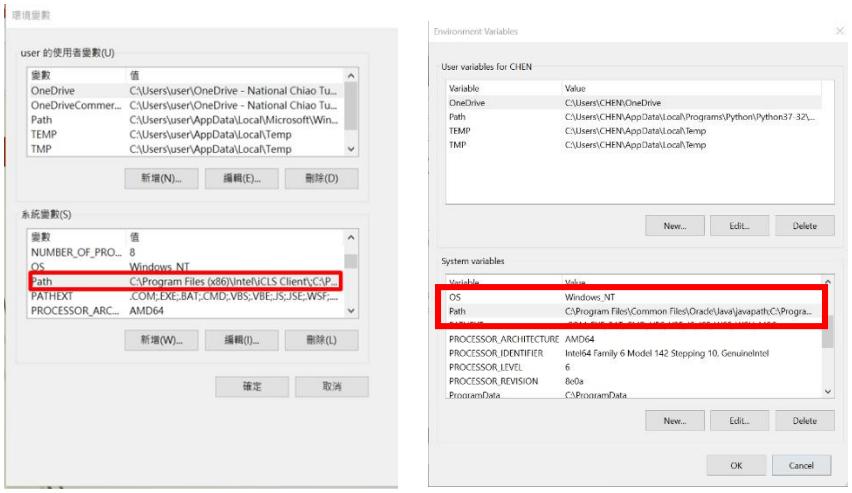
iii. 點選「檢視進階系統設定」(Click **View advanced system settings)**

iv. 點選「環境變數」(Click **Environment Variables)**



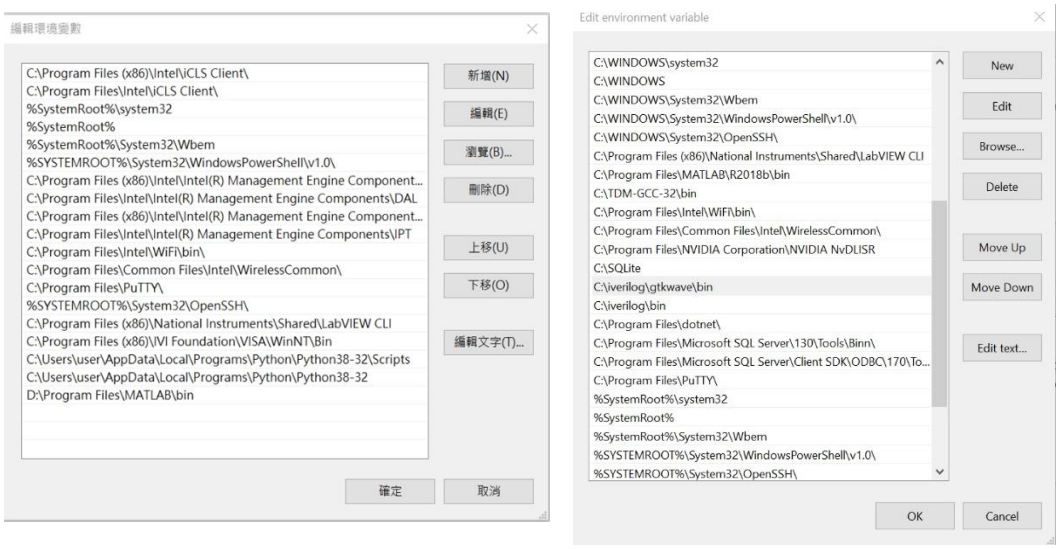
v. 於系統變數中找到「Path」 (find **PATH** in the section System Variables)

點一下後按編輯(Click it and edit)

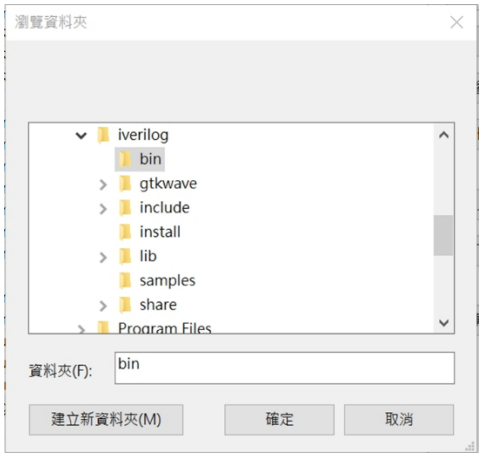


vi. 點選「新增」(Click **New)**

之後點選「瀏覽」(Click **Browse)**



vii. 找到 iverilog/bin 後按確定(Find iverilog/bin and click OK)



viii. 點選「新增」(Click **New)**
之後點選「瀏覽」(Click **Browse)**
找到 iverilog/bin 後按確定(Find **iverilog/gtkwave/bin** and click OK)

ix. 按確定後即新增成功，之後須將電腦重新啟動 (After clicking OK, restart the computer)

2. MacOS 環境下的安裝(Download under MacOS system)

(a) 安裝 iverilog (Download iverilog)

✓ Install Homebrew

```
$ /usr/bin/ruby -e "$(curl -fsSL
https://raw.githubusercontent.com/Homebrew/install/master/install)"
```

✓ Install icarus-Verilog

```
$ brew install icarus-Verilog
```

```
brew install icarus-verilog
==> Downloading https://homebrew.bintray.com/bottles/icarus-verilog-11.0.big_sur.bottle.tar.gz
Already downloaded: /Users/huyufang/Library/Caches/Homebrew/downloads/1a884851278dc1005155256471b110e028ff786e
adc3f6b6940327609ac6c1b4--icarus-verilog-11.0.big_sur.bottle.tar.gz
==> Pouring icarus-verilog-11.0.big_sur.bottle.tar.gz
  /usr/local/Cellar/icarus-verilog/11.0: 56 files, 6.6MB
which iverilog
/usr/local/bin/iverilog
```

✓ 版本過舊問題 (Version Error)

若安裝過程遇到 CLT (CommandLineTools) 版本過舊的問題，可以執行下面兩條指令解決

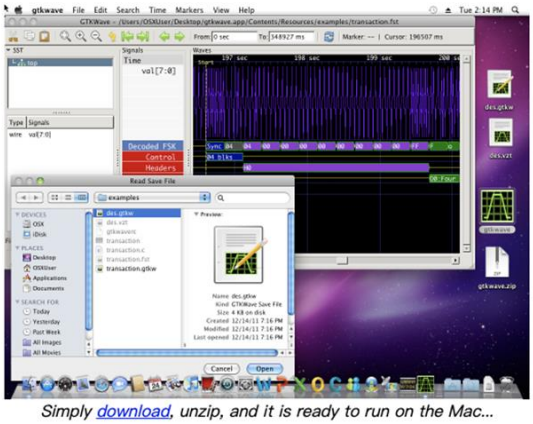
Following two commands can solve the CLT version Error

```
$ sudo rm -rf /Library/Developer/CommandLineTools
# 刪除原有的 CLT (delete own CLT)
$ sudo xcode-select --install        # 安裝新的 CLT (Install new CLT)
```

```
Error: Your CLT does not support macOS 11.2.
It is either outdated or was modified.
Please update your CLT or delete it if no updates are available.
```

(b) 安裝 gtkwave (Download gtkwave)

i. 下載網址 Download here：http://gtkwave.sourceforge.net/
點選 download (click **download**)



Simply download, unzip, and it is ready to run on the Mac...

ii. 解壓縮 gtkwave.zip，會看到應用程式 gtkwave
按住 **control**，打開 gtkwave
Unzip **gtkwave.zip** you'll see gtkwave
Press **control** and open gtkwave

iii. 接著會跳出警告視窗，點選打開
Click open on the warning window

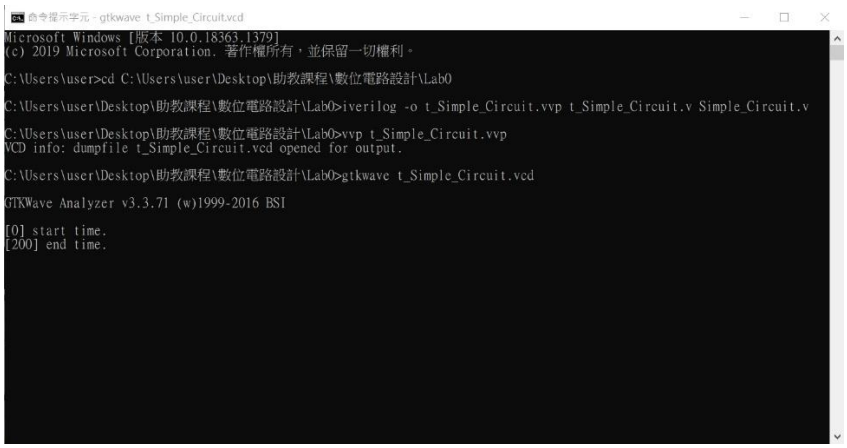
3. Iverilog 與 gtkwave 使用方式(Usage of iverilog and gtkwave)

i. 下載 提供的兩個檔案: Simple_Circuit.v 和 t_Simple_Circuit.v
Download files provided on E3 (Simple_Circuit.v & t_Simple_Circuit.v)

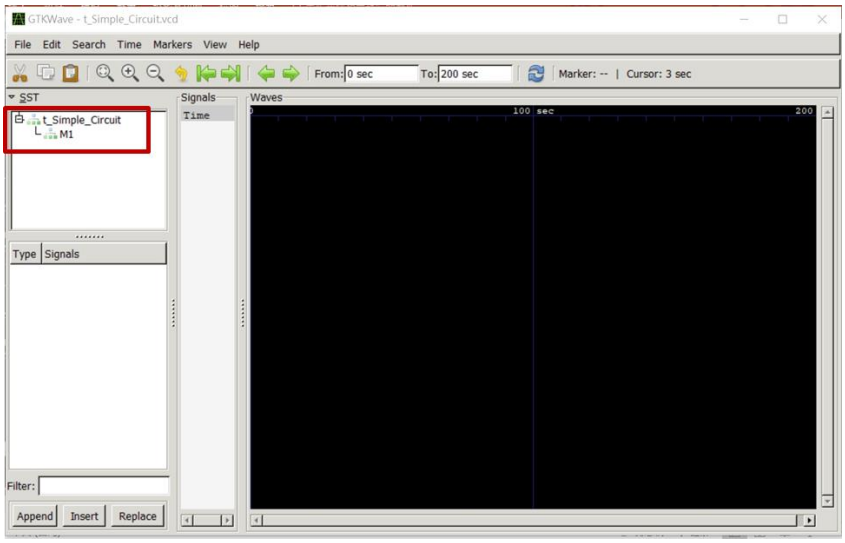
ii. 打開「命令提示字元」(終端機)
open **Command Prompt**

iii. 使用 cd [路徑]到達 Simple_Circuit.v 和 t_Simple_Circuit.v 所在資料夾
move to the directory your files at

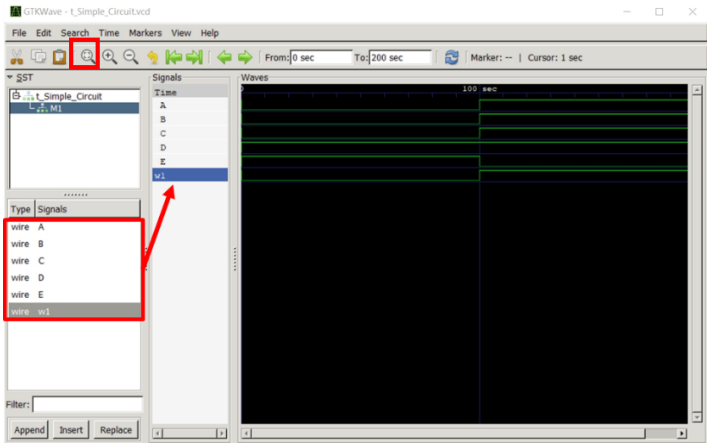
- ✓ iverilog -o t_Simple_Circuit.vvp t_Simple_Circuit.v Simple_Circuit.v
- ✓ vvp t_Simple_Circuit.vvp
- ✓ gtkwave t_Simple_Circuit.vcd



iv. gtkwave 視窗出現之後，點選 t_Simple_Circuit 旁邊的 ＋
並點選 M1
click＋next to t_Simple_Circuit and click **M1**



將下方出現的五個變數拖至右側 Signals 欄
點選左上方的 讓波型以最適合螢幕大小的方式顯示
Drag variables below to the **Signals** section
Click so the waveform fit the window size properly.



4. 撰寫 verilog 並編譯及執行的步驟 (Steps to compile Verilog code and run)

i. 使用任意文字編輯器撰寫 module 及 testbench 並將副檔名皆存成.v
Use any text editot to finish your module and testbench. Stores them as .v file
E.g. notepad++、VSCode…

ii. 撰寫 testbench 務必於 initial begin 之後加入
Remember to add following lines in testbench after initial begin
```
$dumpfile("filenameA.vcd");
$dumpvars;
```

iii. 打開命令提示字元，使用 cd [路徑]到達.v 所在資料夾
Open Command Prompt and move to the directory your .v files at
```
iverilog -o filenameB.vvp testbench_filename.v module_filename.v
vvp filenameB.vvp
gtkwave filenameA.vcd
```

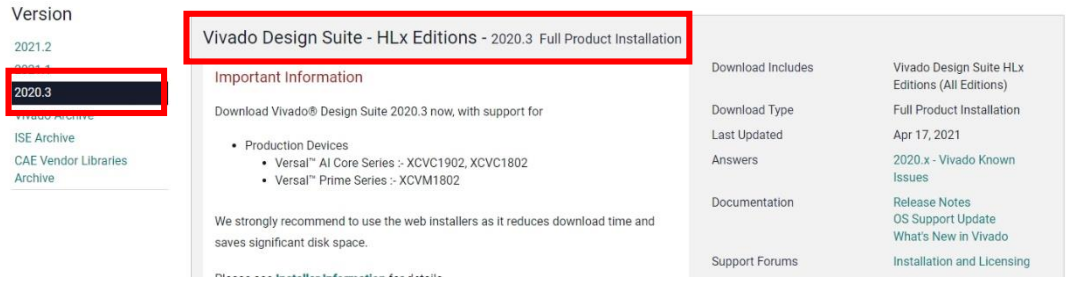
B. Vivado

需在 Windows 系統下使用(Alowed only under Windows)

1. Vivado 之下載、安裝及取得授權 (Download, Setup, and Authorization of Vivado)

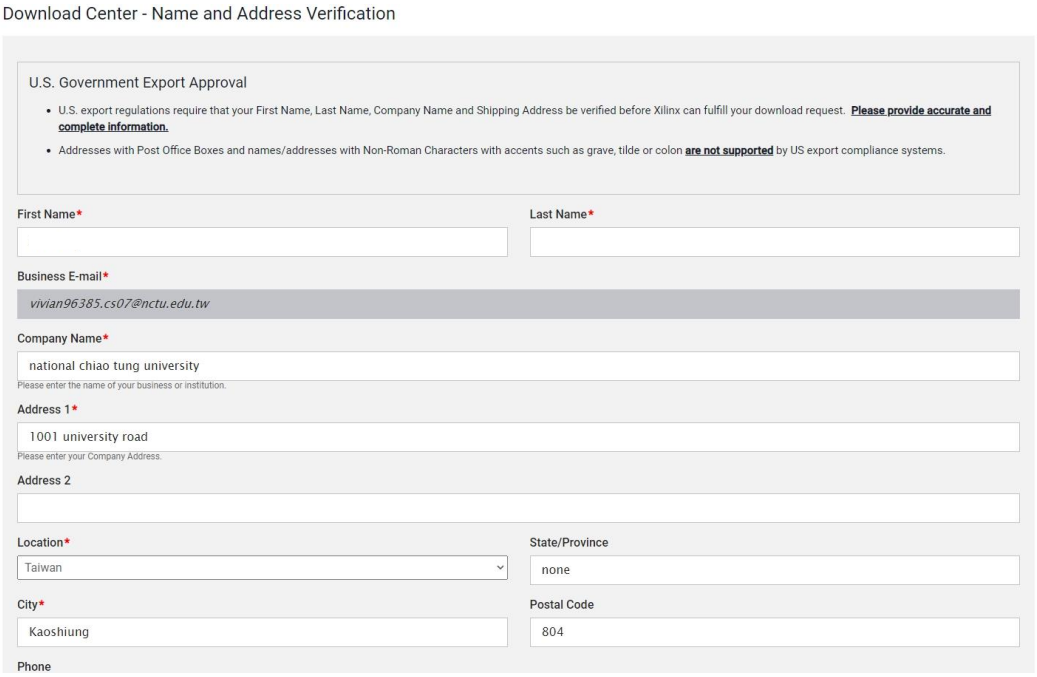
(a) 連結至「https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2020-3.html」，如下圖所示，並確定下載的是 2020.3 版本。

Connect to https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2020-3.html , and the following page will be shown, be sure to download 2020.3version.



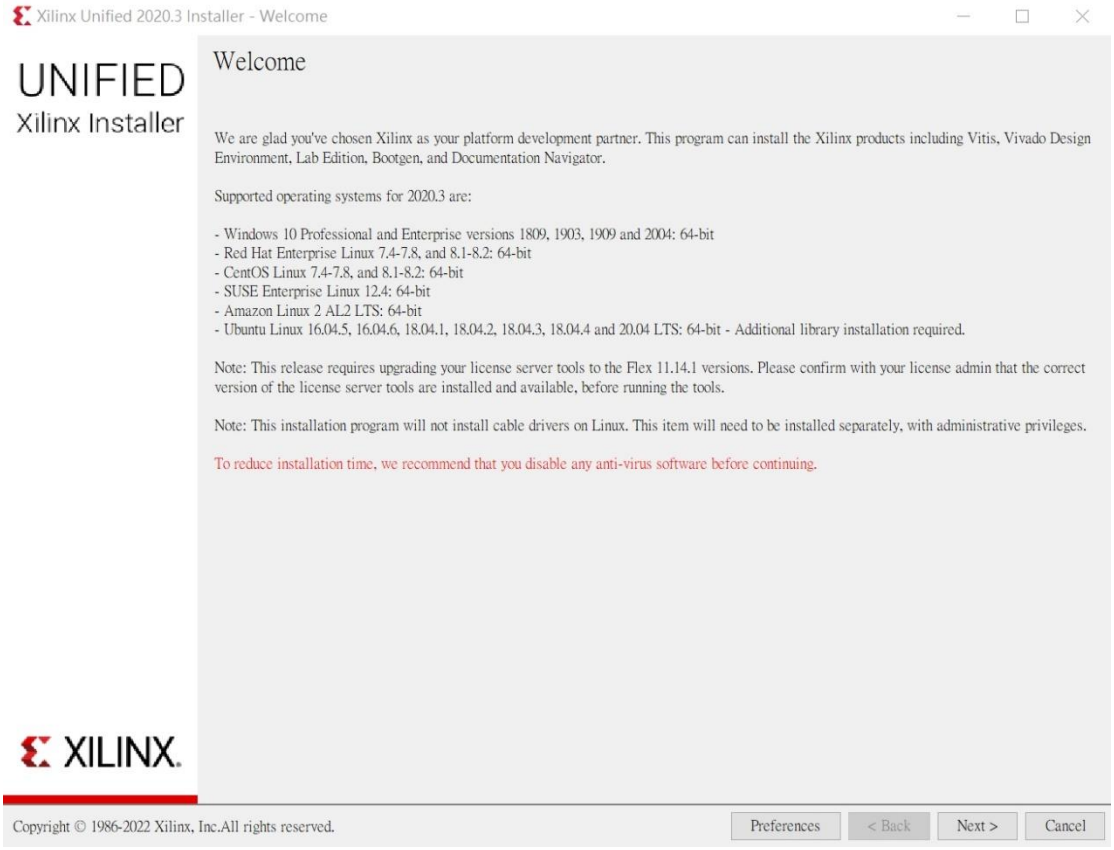
(b) 登入 Xilinx；若無帳號，則以學校的電子郵件註冊之。填寫認證資料。

Sign in to Xilinx, or register one with school's email if you don't have an account. Fill out your personal information in the page.



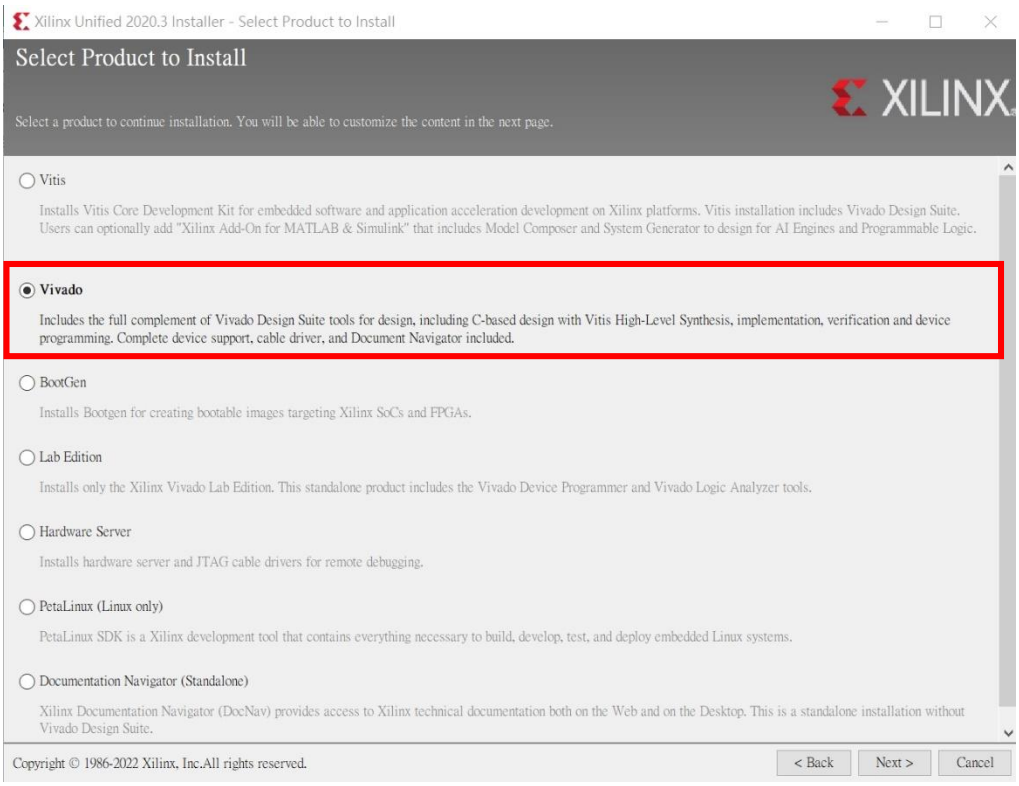
(c) 開始下載，如下圖所示:

Start to download, as shown in the following figure:



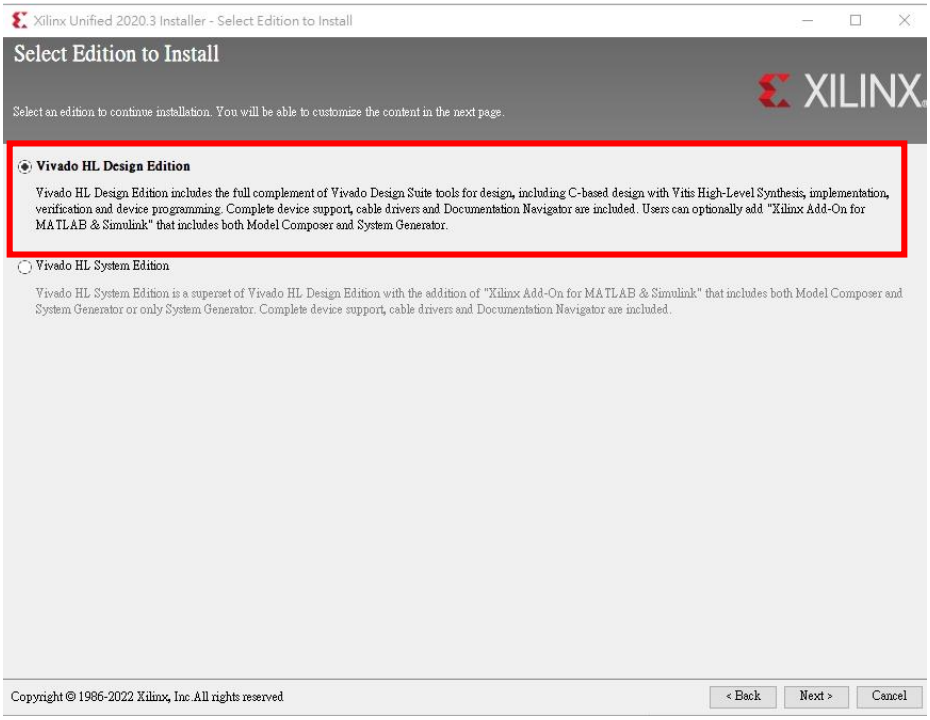
(d) 在產品選擇時選擇 Vivado。

Choose Vivado at “Select Product to Install”.



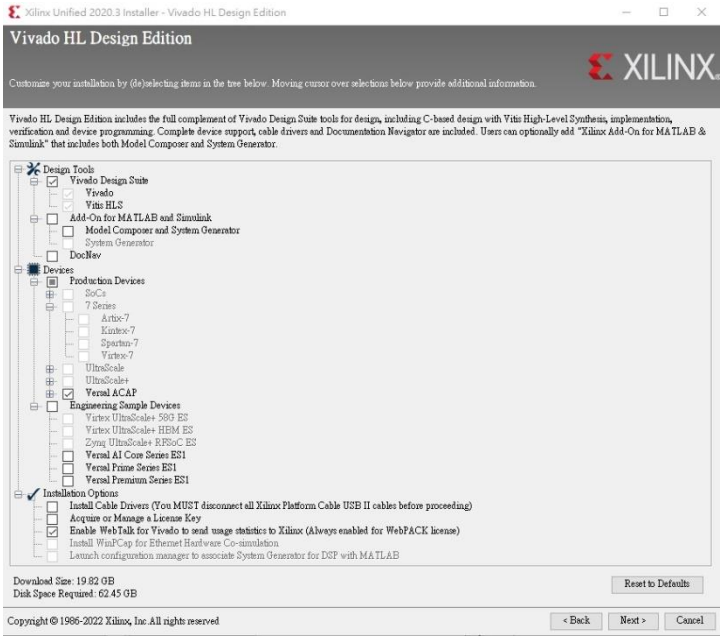
(e) 在版本選擇時請選 Vivado HL Design Edition。

Choose Vivado HL Design Edition at “Select Edition to Install”.



(f) 之後的選擇如下圖所示。因為這門課不會連到板子，所以 Device 可以任選一個

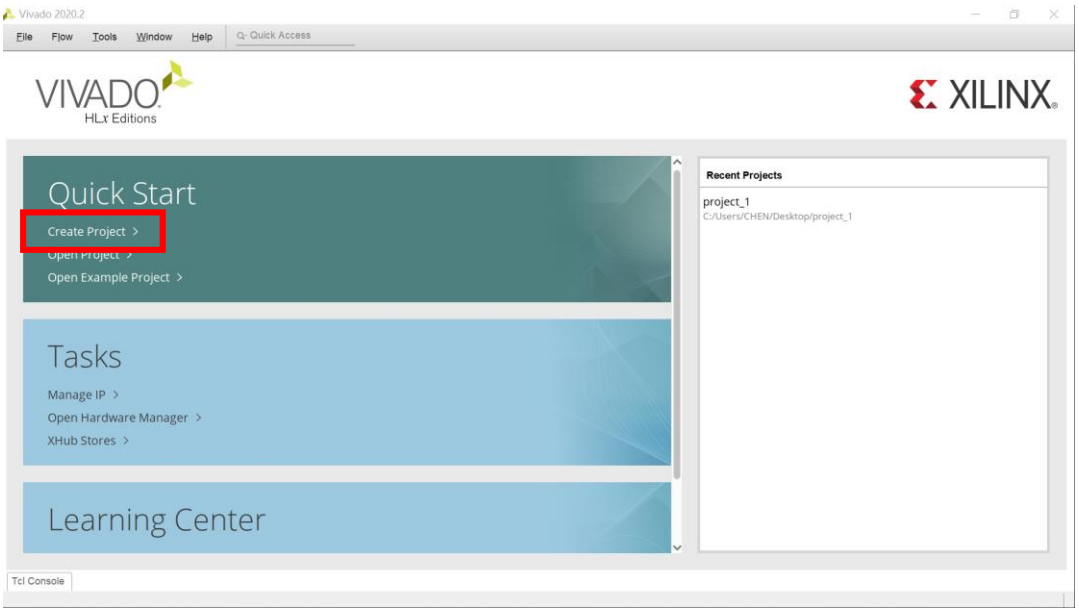
After that, click your selection as shown in the following figure. Since we will not connect to any board in this course, you may choose any one listed in the “Devices” part, and at least one should be selected.



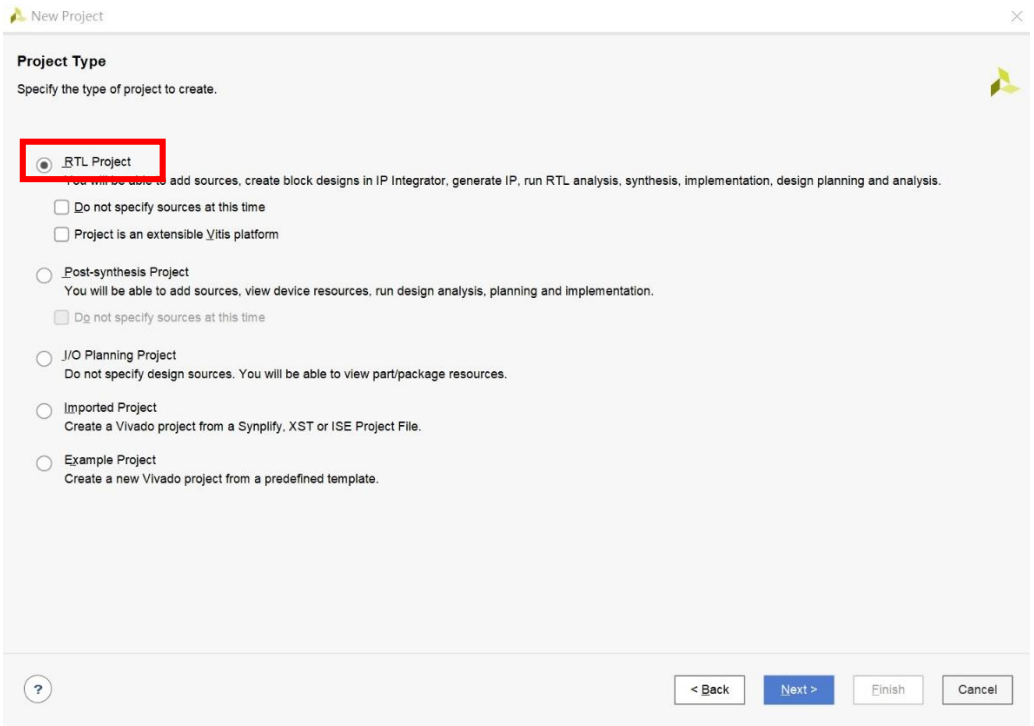
2. Vivado 之專案建立、程式編譯及執行模擬 (Project Creation、Program Compilation and Simulation on Vivado)

(a) 建立專案 (Project Creation)

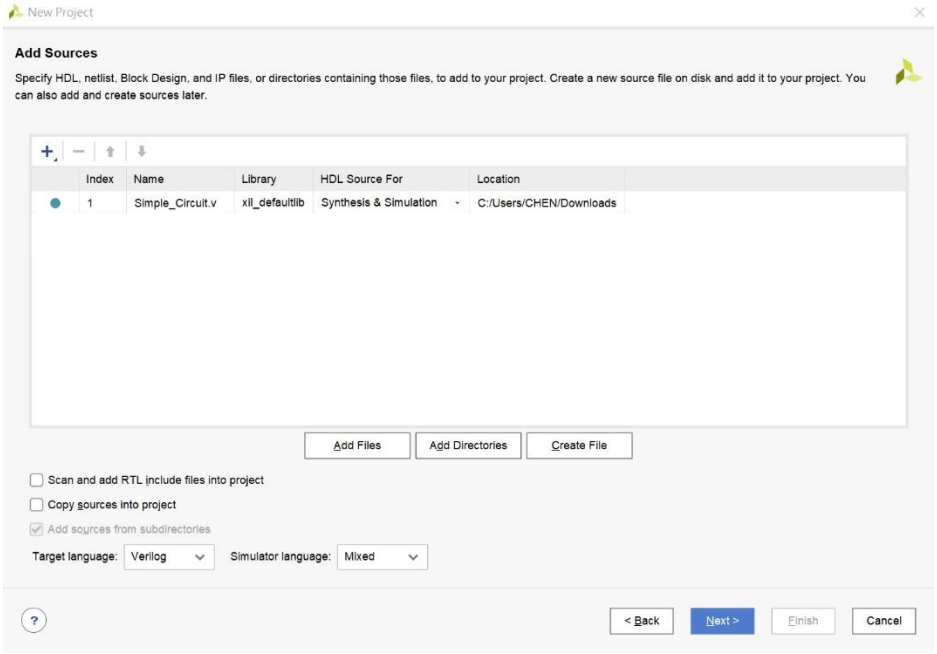
i. 新增專案 (Create a new project)



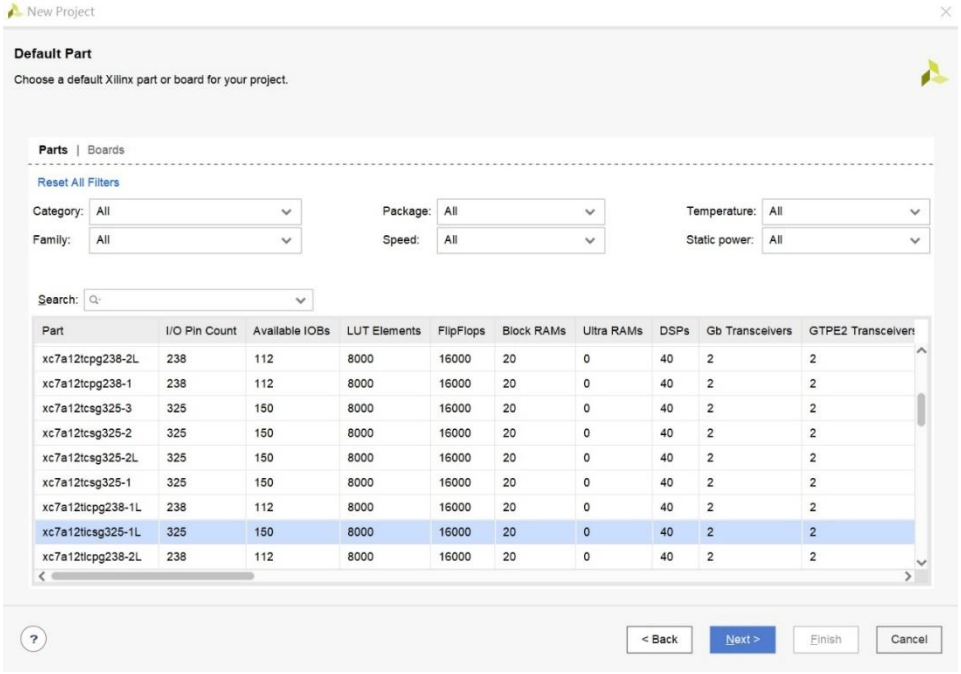
ii. 選擇 RTL Project (Choose RTL Project)



iii. 加入相關檔案或創建檔案 (Add source files or create some files)

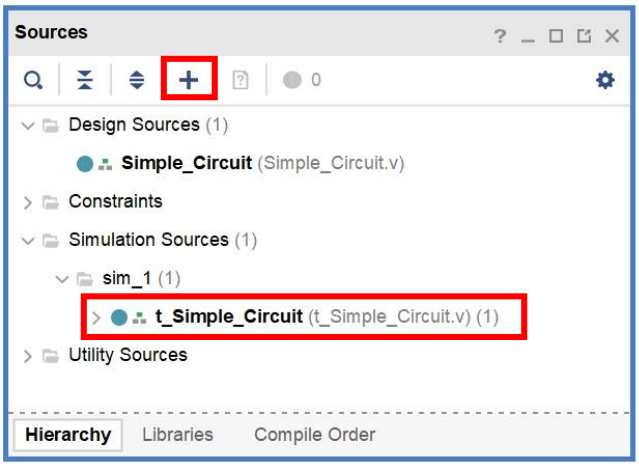


iv. Default Part 不需作更改 (No need to make changes in the "Default Part")

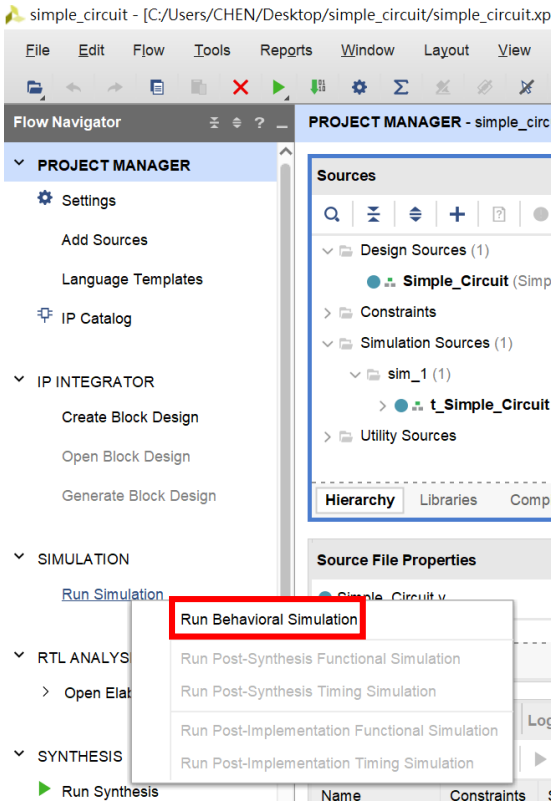


(b) 執行模擬 (Simulation)

i. 按下上面的「＋」加入 testbench 為 simulation source (Add your testbench as simulation source by clicking the ＋ shown on top of the screen of “Sources”.)



ii. 按下畫面左方工具列的 Run Simulation → Run Behavioral Simulation



iii. 完成模擬，觀察結果之波形圖 (Complete simulation and observe the waveform of simulation results.)