Lab 4

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Section 75C9

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* Prelab Questions:

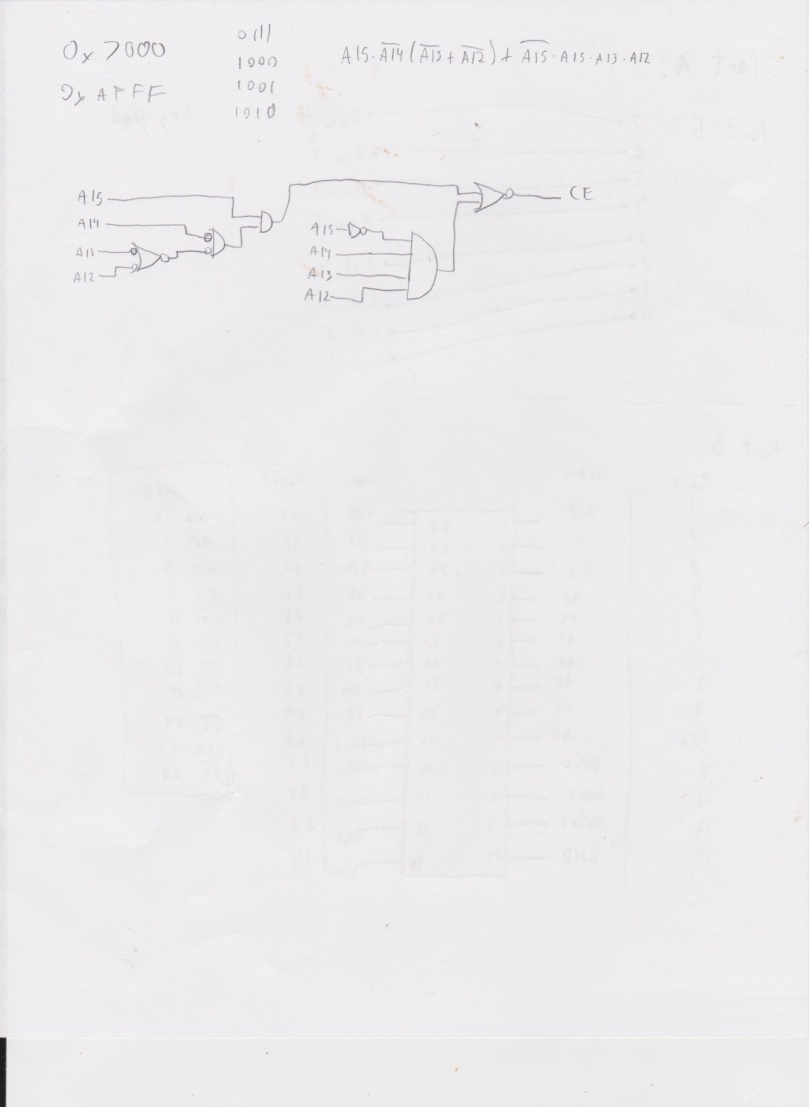
1. What is the size CS1 used in this lab?

*The size of CS1 is 64k.*

2. Which address lines MUST be present in the SRAM chip-enable equation for **full address decoding**?

*A23:0 would need to be present for full address decoding.*

3. Draw a schematic of a 16k x 8 RAM expansion starting at address 0x7000. **You may only use address lines for decoding.**



4. On the uPAD Proto Base board, is the CPLD required for interfacing with the SRAM? If not, explain.

*You don't need the CPLD to decode the SRAM, we can use the CS pins.*

5. The simple memory test program described above is not very good. It checks for neighboring data pins that are shorted or left unconnected, but we have no idea if the address bus is working. Describe a procedure for testing the address lines. Are there any limitations to your procedure (for example, does your procedure test **all** of the address lines)? Explain.

*We can input the values of the addresses inside each address line. This way we can tell which addresses are connected poorly.*

6. In this lab, we configure CS1 to be bigger than the SRAM so that we can divide it for multiple devices. If we want to connect many devices to the memory bus, this is a good way to conserve XMEGA chip select outputs. Suppose we wanted to configure CS1 to span from 0x1A0000 to 0x1BFFFF instead. Is this a valid range for an XMEGA chip select? With the hardware on your uPAD Proto Base as it is now, can we divide this new CS1 the same way do in this lab? Why or why not?

*No, because the CS has a range of 64k and this span exceeds the 64k.*

* Problems Encountered:

I had trouble setting the PINnCTRL for the Keypad

* Future Work/Applications:

I learned how to use the keypad and to setup the SRAM.