DIGITAL DESIGN

ASSIGNMENT 2

Deadline: *22:30, Wednesday 17 November 2021*

Lab sessions & Location:

1. **Lychee Garden 6, Room 409 (Wednesday 14:00-15:50 pm)**
2. **Lychee Garden 6, Room 404 (Thursday 10:10-12:10 am)**
3. **Teaching Building 2, Room 205 (Friday 10:10-12:10 am)**
4. **Lychee Garden 6, Room 402 (Friday 14:00~15:50 pm)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Given the Boolean functions F1 and F2, show that
    a. The Boolean function E = F1 + F2 contains the sum of the minterms of F1 and F2
    b. The Boolean function G = F1 · F2 contains only the minterms that are common to F1 and F2.
2. Convert each of the following to the other canonical form.
    a. F(x, y, z) = ∑(3, 5, 7)
    b. F(A, B, C, D) = ∏(3, 5, 8, 11, 12, 15)
3. Write the following Boolean expressions in:
    a. (b’ + d)(a’+ b’+ c)(a’ + c) SOP form
    b. xy + x’z’+ x’yz POS form
4. Determine whether the following Boolean equation is true or false. Show your process.
    a. y’z’ + yz’ + x’z = x’ + xz’
    b. x’y+ xz + y’z’= xy’ + x’z’ + yz
5. Simplify the following Boolean functions and expressions, using four-variable Karnaugh maps:
    a. F (w, x, y, z) = ∑ (8, 10, 12, 13, 14)
    b. F (A, B, C, D) = ∑ (0, 2, 5, 7, 8, 10, 13, 15)
    c. AB’CD + AD + AC’ + BCD
    d. A’B’C’D + ABCD + A’BC’ + AB’C + AB’D
6. Implement the following logical functions with two-level NOR gate circuits. Write down the simplification process, then draw the circuit diagram.
    a. F(A, B, C, D) = A’B’C’D + CD’ + AC’D
    b. F(A, B, C, D)= A’+ AB + B’C + ACD
7. Simplify the following Boolean function F, together with the don’t-care conditions d, and then express the simplified function in sum-of-minterms form:
    a. F(A, B, C, D) = ∑(4, 12, 7, 2, 10) with d(A,B,C,D)= ∑(0, 6, 8)
    b. F(A, B, C, D) = ∑(2, 4, 10, 12, 14) with d(A,B,C,D)= ∑(0, 1, 5, 8)

8. Implement the following Boolean expression with exclusive-OR and AND gates, draw the circuit diagram:
   F = A'BC'D + AB'CD' + ABC'D' + A'B'CD

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys develop platform (xilinx FPGA chip artix 7 inside) to design a combinational logic circuit and do the testing.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1. 'Ch2-Boolean Algrebra-ICs-SUSTC.ppt' and 'CH3-Minimisation-SUSTC' in Black Board site.

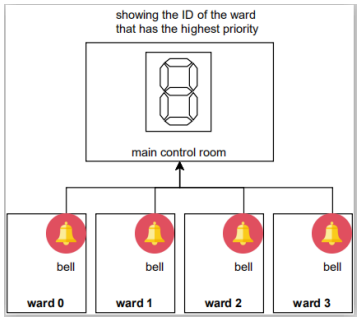
2. 'Digital design lab5', 'Digital design lab6' and 'Digital design lab7' in Black Board site.

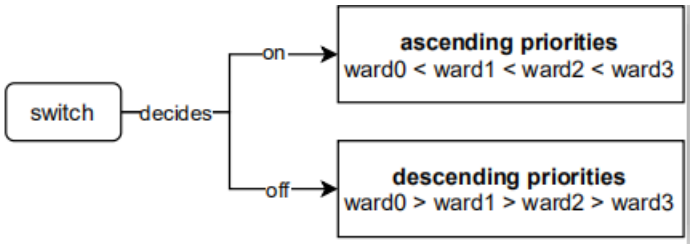
3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

There are 4 wards, which are numbered from 0 to 3 respectively. Each room has a call bell, which can be turned on and turned off. In the main control room there is a 7-seg tube that shows the ID of the room whose bell is on with the highest priority.





The priority order of wards are determined by a switch: while the switch is on, it means priority increases as the number increases (the #0 ward has the lowest priority, and the #3 has the highest priority), while the switch is off, it means priority increases as the number decreases (the #0 ward has the highest priority, and the #3 has the lowest priority)

For example, if the priority increases as the number increases(the #0 ward has the lowest priority, and the #3 has the highest priority), both the call bell of room#0,#1 and #2 are on, the 7-seg tube only show number 2, because in this situation the highest priority is ward #2.

Write a circuit to realize this function and test.

- Do the design.
- Create the constraint file.
- Do the synthetic and implementation, generate the bitstream file, connect the PC which run the vivado project with Minisys develop board and program the device, then test on the Minisys develop board.
- While Testing the circuit, at least four test scenarios need to be considered:
    i. Only one ward's call bell is turned on
    ii. Two or more wards whose call bells are turned on while the priority order is set as priority increases as the number decreases.
    For example, the call bell of ward #1, #2, #3 are turned on, number 1(the highest priority among 1, 2 and 3) is expected to be showed on the 7-seg tub.
    iii. Two or more wards whose call bells are turned on while the priority order is set as priority increases as the number increases.
    For example, the call bell of ward #1, #2, #3 are turned on, number 3(the highest priority among 1, 2 and 3) is expected to be showed on the 7-seg tub.
    iv. No ward's call bell is turned on

NOTE:

1. If the call bells of all the wards are off, the 7-seg tube should be off (doesn't show any information)
2. Only one 7-seg tube be used on the Minisys develop board in this assignment.

TASK2:

Implement the circuit and test its function: F(a,b,c) = a^b^c

- Write its true-table and K-map, using K-map to simplify the circuit if possible.
- Using data flow to Realization of circuit design in SOP and POS style respectively
- Write testbench in Verilog and do the simulation to verify the function of design

SUBMISSION

Submit your assignment report to the BlackBoard on *Corresponding site* ("Digital Logic Fall 2021(Lab)" by the deadline. NOTE: There is ONLY 1 DDL on BlackBoard.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	4
Question 2	4
Question 3	4
Question 4	4
Question 5	8
Question 6	8
Question 7	4
Question 8	4
Total	40 marks

Lab: 60%

Task 1: Design in Verilog	5 marks
Task 1: Constrains file	5 marks
Task 1: Photos about test result on Minisys develop board and description on inputs and outputs. 4 test at least	5*4 marks
Task 2: Truth-table and K-map of the circuit	5*2 marks
Task 2: Design in Verilog in data flow style with SOP and POS in one module	5 marks
Task 2: Test bench in Verilog, simulation result and its description	5*2 marks
Problem and solution. if there is no problem, suggestions or solutions is asked.	5 marks
Total	60 marks