Parking Lot Management System

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DEPT. OF COMPUTER SCIENCE AND ENGINEERING

Contents

1 Development Plan

Among the topics provided, we have chosen the parking lot management system as our project, which requires us to design a rather complex FSM and thus the process of completing this project gave us a lot of improvement in our understanding of digital logic and our ability to code.

1.1 Task Assignments & Contribution of Members

As a whole, in this project, the three group members had a similar workload, and there were sufficient and timely communications and mutual assistance during the implementation process. Due to the heavy functionality of our selection (parking lot management system), for complex modules, the leading member of implementation is listed below, while the rest of the modules were reasonably evenly distributed. After all, we summarize the percentage of group members' contributions as 33 % - 33 % - 33 %.

Li Zinan	① Overall design of FSM and its Verilog implementation ② Main coder of administrator part
He Zean	① Music player & keyboard module & data storage mechanisms ② Report & slides
Tang Xinyu	① Rollable seg-tube display module ② Continuous keyboard input

1.2 Schedule & Execution Record

Date	Topic	Check
Nov. 30	① FSM design, data structure and other technique details	✓
Dec. 12	① FSM ~30 % ② basic modules finished ③ complex modules ~50 %	✓
Dec. 17	① All modules basically completed ② synthesize FSM	✓
Dec. 29	① Final check ② prepare for presentation	✓

2 Project Design

2.1 设计

本次项目几乎实现了文档中所有描述的功能：

① **进场模式** 闲置状态下，系统滚动显示剩余车位等信息，并允许用户在进场时选择停入 A 区或 B 区。若无剩余车位则拒绝停入，否则将占用一个车位并返回标识码。

② **出场模式**

2.2 Structure Design

2.2.1 主状态机

接口和变量描述 主状态机接收 6 个输入，分别为时钟信号 clk2 (1Hz)，clk3 (500Hz)，使能信号 enable，5-bit 按钮 button，30-bit 键盘输入 key，键盘输入结束信号 finish。其输出 16 个信号，分别为显示模式 displayMode，剩余车位 left，起始价格 st，时价 per，VIP 用户 ID id1,id0，VIP 余额 remain1,remain0，以及七段数码显示管 x7,x6,x5,x4,x3,x2,x1,x0。

状态机现态和次态使用 6 位寄存器储存，并且将每个状态设为参数，便于理解。主要状态如下所示：

```
parameter Idle = 6'b000001;
parameter InputVip = 6'b000010;
parameter Register = 6'b000011;
parameter VipRecharge = 6'b000100;
parameter VipInterface = 6'b000101;
```

2.3 Verilog Designs & Port Constraints

2.3.1 Music player

The music player, basically, is a FSM that

3 On-board Verifications

4 Summary & Optimization Prospects

References

Disclaimer: All references used in this project are only for the purpose of guiding the direction of exploration and ensuring correctness, any code appearing in the referenced web pages has not been used directly, unless explicitly stated.