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Q1.

(1) Offset of cache have 5-bit length.
Thus cache block size is $2^5 = 8$ words

(2) Index of cache have 5-bit length
Thus entries number is $2^5 = 32$ entries

(3)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Tag	0	0	0	0	0	0	1	0	0	3	0	2
Hit/Miss	N	Y	Y	N	N	N	N	N	Y	N	Y	N
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

(4) hit ratio = $4/12 = \frac{1}{3}$

(5) 0, 3, mem[3072]
4, 2, mem[2176]
5, 0, mem[160]
7, 0, mem[224]

Q2. (1)

Address	17	32	2	2059	4124	65	2067	2200	30	0	4102	360
Index	1	2	0	0	1	4	1	9	1	0	0	22
Tag0	0	0	0	0	0	0	1	1	1	0	0	0
Tag1	\	\	\	1	2	\	2	\	0	1	2	\
Hit/Miss	N	N	N	N	N	N	N	N	N	Y	N	N
Replace	N	N	N	N	N	N	Y	N	Y	N	Y	N

(2) cache size = $2 \times 2^9 \times 2^1 = 2^{12} = 4096$ word

(3)

Index	Tag	Data	Tag	Data
0	0	mem[0]	2	mem[4096]
1	1	mem[2064]	0	mem[16]
2	0	mem[32]	\	
4	0	mem[64]	\	
9	1	mem[2192]	\	
22	0	mem[352]	\	

Q3. (1) Page size $= 2^{12} = 4$ KiB

PTEs $= 2^{(43-12)} = 2^{31}$

(2) PTE size $\times$ PTEs $= 2^{33} = 8$ GiB

Q4. (1) Because $128 = 2^7$, we need $7+1=8$ parity bits to protect it.

(2) $0x5C6 = 010111000110$

The parity bit is 0110

$p_1 = 0$, $\underline{0}10111000110$ there are two 1, is correct
$p_2 = 1$, $0\bar{1}0\bar{1}1\bar{1}00\bar{0}1\bar{1}0$ there are four 1, is correct
$p_3 = 1$, $0\bar{1}\bar{0}111000110$ there are three 1, is wrong
$p_4 = 0$, $0101\bar{1}\bar{1}\bar{0}\underline{0}\underline{1}\underline{1}\bar{0}$ there are two 1. is correct

Thus, the 4-th bit is wrong, it should be 0100011000110