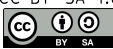


1	2	3	4	5	6
A					A
B					B
C					C
D					D

DESIGNED FOR:  
2 layer stackup (1.6mm) - JLCPCB  
Core Er = 4.6 @ 1 GHz  
Core Loss Tan = 0.025 @ 1 GHz

Top Solder Mask		0.01
Top Layer		0.035
Core		1.5
Bottom Layer		0.035
Bottom Solder Mask		0.01

REV1 BUGS / THINGS TO IMPROVE:

Project Name: PCB Log Periodic Antenna (0.8–6 GHz)			BYTECHLAB RESEARCH
Sheet Name: Root			
Sheet Path: /			CC BY-SA 4.0 
File Name: LOG_PERIODIC_PCB.kicad_sch			
Size: A4	Date: 2026-01-03	Rev: 1	
Designed By: Andrzej Laczewski	Website: www.bytechlab.com	Id: #/1	