Characteristics of general inverter VTC:

Threshold voltages:

* V_IL - is the maximum allowable input voltage such that the gate is off
* V_IH -is the min allowable input voltage such that the gate is on
  * The above threshold voltages are found by setting dVo/dVi = -1
  * undefined logic level between : V_{IL} <= Vi <= V_{IH}
* V_{OH} = output when vi=0
* V_{OL} = output when vi=VoH

$V_{tw} = V_{IH} - V_{IL}$

* A good logic gate has a small transition width

$V_{ls} = V_{OH} - V_{OL}$

* A good logic gate has a large logic swing

Noise Margin: ability of a digital logic circuit to maintain its logic state under varying voltage levels

Noise Margins:

$NM_H - V_{OH} - V_{IH}$

$NM_L - V_{IL} - V_{OL}$

$NM = minNM_L, NM_H$

Example : VTC of ideal inverter

$V_{OH} = V_{CC}$

$V_{OL} = 0$

$V_{IH} = V_{IL} = V_{CC}/2$

$NM_H = \frac{V_{DD}}{2}$

$NM_L = \frac{V_{DD}}{2}$

$V_{ls} = V_{DD}$

$V_{tw} = 0$

$\frac{Vo}{Vi}|_{V_{OL} and V_{OH}} = \infty$

Propagation Delays:

$t_p = \frac{t_{PHL}+t_{PLH}}{2}$ = Max pulse rate for transmission thru it

t_{PHL} = time at 50% output Vo falling - time at 50% input rising Vi

t_{PLH} = time at 50% output Vo rising - time at 50% input falling Vi

t_r = rise time (10%-> 90%)*Vo (just look at output)

t_f = fall time (90% -> 10%)*Vo (just look at output)

$CircuitBandwidth = \frac{.35}{t_r}$

Diode:

$I_D = I_s(e^{V_D/(\eta * V_T)} - 1$

Models of diode:

(1) ideal switch diode model

(2) ideal switch with voltage offset
  * we use this on in this course

(3) piecewise linear
  * $I_{off} <= .01 I_{on}$
  * $V_{off} = .6V, V_{on} = .7V$

Limitation of Diode digital Circuits

* Can't implement, NOT, NOR or NAND gates
* They have problems, voltage drop across them

MOSFETS

Enhancement MOS - channel isn't already built in (normally off)

Depletion MOS - channel is already present (normally on)

NMOS:

Triode section : $V_{GS} > V_T and V_{DS} <= V_{GS} - V_T$

$I_{DS} = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

Saturation region -

$V_{GS} > V_T and V_{DS} >= V_{GS} - V_T$

$I_{DS} = k(V_{GS} - V_T)^2$

$k = (1/2)\mu_N C_{ox} * (W/L)$ [A/V^2]

$k = (1/2)k'(W/L)$

Body Effect

$V_T = V_{T0} + \gamma * (\sqrt{2|\phi_F| * V_{SB}} - \sqrt{2|\phi_F|})$

PMOS - like NMOS but S(VDD) and D(GND)

Triode section :

$V_{SG} > |V_T| and V_{SD} <= V_{SG} - |V_T|$ |

* $I_{SD} = k[2(V_{SG} - |V_T|)V_{SD} - V_{SD}^2]$

Saturation region :

$V_{SG} > |V_T| and V_{SD} >= V_{SG} - |V_T|$ |

$I_{SD} = k(V_{SG} - |V_T|)^2$

MOS Equiv circuits:

Transconductance: Q = saturation

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}|_{\Delta V_{DS}=0}$

$=> g_m = 2k * (V_{GS} - V_T)$

$=> g_m = 2\sqrt{kI_D}$

Dynamic Resistance(ac): Q = Saturation

$=> r_d = \frac{1}{k(V_{GS}-V_T)^2\lambda}$

Static Resistance(dc): Q= any

$R_DS = V_{DS}/I_{DS}$

MOS inverters (body -source connected)

(Note) - Vo is taken across ML(S) and MD(D)

Resistive E-NMOS inverter

* The Resistor (load) is connected to Vdd, this is then connected to the drain of the E-NMOS (driver)
* It takes up to much space

Saturated Enhancement load E-NMOS

* The E-NMOS (ML) its drain con.to Vdd, its gate connected V_{GL} to V_{SL}, this is then connected to the drain of the E-NMOS (M_D), Vi = V_GD
* lower Voh, lower NM, small V_{ls} large V_{tw}, decr exp graph

Linear Enhancement Load

* two batteries

Depletion load NMOS inverter

* The D-NMOS(ML), its drain->Vdd, ML's gate is connected to its source, That source terminal connected to drain of driver (MD).
* Only uses one batt.

Example Problems :

$k_D(V_i - V_{TD})^2 = k_L[2|V_{TL}|(V_{DD} - V_o) - (V_{DD} - V_o)^2]$

$K_R = geometricratio = \frac{k_D}{k_L}$

Design NOR and NAND - using NMOS inverter (M_L config like inv)

NAND - M_{D1} .. M_{Dn} in series
* drivers are the same trans

NOR - M_{D1} ..M_{Dn} in parallel
* driver are the same trans

CMOS inverter

* $I_{D,max} = I_D(Vi = Vo)$
* $V_M = V_i = \frac{V_{TN}+\sqrt{K_R}(V_{DD}-|V_{TP}|)}{1+\sqrt{K_R}}$

Symmetrical CMOS inverters

* $V_{TN} = |V_{TP}|, k_p = k_N, Coxsame, V_M = V_{DD}/2$
* $=> K_R = k_p/k_N = 1 => \frac{\mu_N}{\mu_p} = \frac{(W/L)_p}{(W/L)_N}$

* Usually \mu_p} = 2.5 => (W/L)_p = 2.5*(W/L)_L_p $(W/L)_p = 2.5 * (W/L)_{Lp}$ W/L)_p = 2.5*(W/L)_L_p $W/L)_p = 2.5 * (W/L)_{Lp}$ L)_p = 2.5*(W/L)_L_p $L)_p = 2.5 * (W/L)_{Lp}$ _p = 2.5*(W/L)_L_p $p = 2.5 * (W/L)_{Lp}$ = 2.5*(W/L)_L_p $$ = 2.5*(W/L)_L_p $$$$ 2.5*(W/L)_L_p $2.5 * (W/L)_{Lp}$ .5*(W/L)_L_p $.5 * (W/L)_{Lp}$ * (W/L)_L_p $*(W/L)_{Lp}$ W/L)_L_p $W/L)_{Lp}$ L)_L_p $L)_{Lp}$ _L_p $_{Lp}$ _p p $

Design NOR and NAND - using CMOS inverter

Two input NOR gate (2 Mps and 2 MNs)

* M_p's connected in series(top near V_DD, (G_N) M_N's connected in parallel, M_p1 and M_N1 source and drain connected
  Gates of M_p1 and M_N1 are connected, N_N2 and M_p2 gates are connected.
  Output taken across M_p1 and M_n1
* $1/G_p = 1/g + 1/g => g = 2G_p$
* $(W/L)_{p,tot} = 2(W/L)_p$
* $(W/L)_{N,tot} = (W/L)_N$

Two input NAND gate (2 Mps and 2 MNs)

* M_N's connected in series near GND, Output is taken across the intersection of M_N1 and M_P1, M_P1 and M_P2 are connected in parallel, gates are connected from each M_Ni to M_pi like inverter.
* $1/G_N = 1/g + 1/g => g = 2G_N$
* $(W/L)_{N,tot} = 2(W/L)_N$
* $(W/L)_{p,tot} = (W/L)_p$

CMOS VTC Regions

V_i	$0 < V_i < V_{TN}$	$V_{TN} < V_i < V_M$	V_M	$V_M < V_i < V_{DD} - \|V_{TP}\|$	$< V_i$
M_p	Ohmic	ohmic	sa t	sat	off
M_N	OFF	sat	sa t	ohmic	ohmi c

Examples(NMOS - CMOS gates):

EE 307 Solved Examples 1: Design of NMOS and CMOS Gates

- Gate designs are based on good inverter designs.

1. For a depletion NMOS inverter and a depletion NMOS 4-input NAND gate with equal logic levels, $K_D' = 45\mu A/V^2$, $K_L' = 40\mu A/V^2$; $V_{TNO} = 1.5V$, $V_{TDO} = -3V$. For the inverter, $(\frac{W}{L})_D = 2$. The body effect is to be ignored and $V_{OL} = 0.25V$ for both gates when $V_{DD} = 5V$.

(a) Complete the design of the inverter by finding its $(\frac{W}{L})_L$.

(b) Complete the design of the 4-input NMOS NAND gate by finding its $(\frac{W}{L})_D$ & $(\frac{W}{L})_L$.

(a) Solution

$V_O = V_{OL} => V_i = V_{OH} = V_{DD} = 5V$; $V_{TD} = V_{TNO} = 1.5V$; $V_{TL} = V_{TDO} = -3V$

For Driver: $V_{DSD} = V_{OL} = 0.25V < (V_{GSD} - V_{TD}) = (5 - 1.5)V$ => ohmic

$I_{DD} = \frac{1}{2}K_D'(\frac{W}{L})_D[2(V_{GS} - V_{TD})V_{OL} - V_{OL}^2] = \frac{1}{2}K_D'[2](3.5)(0.25) - (0.25)^2]$

$I_{DD} = 1.6875 K_D'$

For Load: $V_{DSL} = V_{DD} - V_{OL} = 4.75V > (V_{GSL} - V_{TL}) = (0 - (-3))$ => saturation

$I_{DL} = \frac{1}{2}K_L'(\frac{W}{L})_L[0 - (-3)]^2 = 4.5K_L'(\frac{W}{L})_L$

$I_{DD} = I_{DL} => 1.6875 K_D' = 4.5 K_L'(\frac{W}{L})_L$

$(\frac{W}{L})_L = 0.422$

(b) (i) Load for inverter and NAND are identical $=> (\frac{W}{L})_L = 0.422$

(ii) $(\frac{W}{L})_D$ increases proportionately with # of inputs

$(\frac{W}{L})_D = 4 \times (\frac{W}{L})_D$ for inverter

$(\frac{W}{L})_D = 8$

CMOS GATE DESIGN

Example 2: For a symmetrical CMOS inverter and a Symmetrical 3-input CMOS NOR gate with a 5 μM process, $\frac{\mu_n}{\mu_p} = 2.5$ and $(\frac{W}{L})_N = \frac{20\mu M}{5\mu M}$ for the inverter.

a Find W_P & L_P for the PMOS transistor in the inverter

b Sketch the 3-input CMOS NOR gate and find W_N & L_N for its NMOS transistors

c Find W_P & L_P for the PMOS transistors in the 3-input NOR gate.

(a) Solution

For the inverter, $(\frac{W}{L})_P = \frac{\mu_n}{\mu_p}(\frac{W}{L})_N = 2.5(\frac{20\mu M}{5\mu M})$

$(\frac{W}{L})_P = \frac{50\mu M}{5\mu M}$ => $W_P = 50\mu M, L_P = 5\mu M$

$(\frac{W}{L})_N$ is same for inverter & each NMOS in the NOR gate

$(\frac{W}{L})_N = \frac{20\mu M}{5\mu M}$

$W_N = 20\mu M, L_N = 5\mu M$

b.

(c) For the 3-input MOS NOR, $(\frac{W}{L})_P = 3(\frac{W}{L})_{P,inverter} = \frac{150\mu M}{5\mu M}$

$W_P = 150\mu M, L_P = 5\mu M$

Example 3: CMOS NOR & NAND CHANNEL Areas on a Chip For a symmetrical CMOS inverter with a 5μm process, $\frac{\mu_n}{\mu_p} = 2.5$, $(\frac{W}{L})_N = \frac{20\mu M}{5\mu M}$. 4-input CMOS NOR & CMOS NAND are designed based on the inverter design such that at the same V_{DD}, they all have same logic levels.

(a) Sketch the CMOS NOR & the CMOS NAND

(b) Determine the PMOS & NMOS areas on the chip for the inverter

(c) Determine the PMOS & NMOS areas on the chip for the 4-input CMOS NOR.

(d) Determine the PMOS & NMOS areas on the chip for the 4-input CMOS NAND.

Solution

(a)(i) Sketch of 4-input CMOS NOR: Extend sketch of 3-input CMOS NOR of example 2 by one more input.

(ii) Sketch of 4-input CMOS NAND

(b) PMOS & NMOS Areas on chip for inverter

$\frac{\mu_n}{\mu_p} = 2.5$; $(\frac{W}{L})_N = \frac{20\mu M}{5\mu M}$ (given)

$(\frac{W}{L})_P = \frac{\mu_n}{\mu_p}(\frac{W}{L})_N = 2.5(\frac{20\mu M}{5\mu M}) = \frac{50\mu M}{5\mu M}$

$A_N = 20 \times 5\mu M^2 = 100\mu M^2$

$A_P = 50 \times 5\mu M^2 = 250\mu M^2$

(c) PMOS & NMOS areas on chip for 4-input CMOS NOR

$G_{N,gate} = G_{N,inverter} => (\frac{W}{L})_{N,gate} = (\frac{W}{L})_{N,inverter} = \frac{20\mu M}{5\mu M}$

$G_{P,gate} = 4G_{P,inverter} => (\frac{W}{L})_{P,gate} = 4(\frac{5\mu}{5}) = \frac{200\mu M}{5\mu M}$

$A_N = 20 \times 5\mu M^2 = 100\mu M^2$

$A_P = 200 \times 5\mu M^2 = 1000\mu M^2$

(d) PMOS & NMOS Areas on Chip for 4-input CMOS NAND

$G_{N,gate} = G_{N,inverter} => (\frac{W}{L})_{N,gate} = (\frac{W}{L})_{N,inverter} = 4(\frac{20}{5}) = \frac{80\mu M}{5\mu M}$

$G_{P,gate} = G_{P,inverter} => (\frac{W}{L})_{gate} = (\frac{W}{L})_{inverter} = \frac{50\mu M}{5\mu M}$

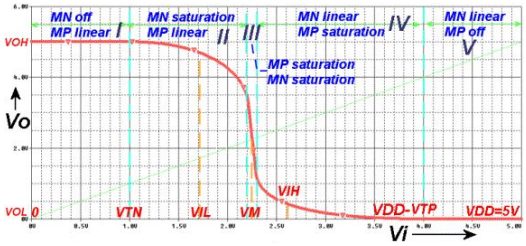
$A_N = 80 \times 5 = 400\mu M^2$

$A_P = 50 \times 5 = 250\mu M^2$

(e) Comparison

Gate type	Areas in MM2 A_N	A_P
Inverter	100	250
4-input NOR	100	1000
4-input NAND	400	250

(f) Areas of both CMOS NOR & CMOS NAND increase with fan-in (# of inputs), but areas increase faster for NOR. Thus NAND is preferred in CMOS; NAND is standard gate in CMOS.


MN off
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IV
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VOH
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VOL 0
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VM
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VDD-VTP
VDD=5V
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