Current- mode Logic Families

Basic ECL circuit (Differential amplifier)

Configuration:

* Q1 - input transistors
* Q2 - reference transistor
* Emitter of both connected
  * R_E connected to E node to $-V_{EE}$
* Two R_C's

R_C and R_E are chosen such that for V_r = V_i, Q1=Q2=active

Note: usually ignore base current

$\Delta V = V_{BE1} - V_{BE2} = V_i - V_R$

$I_{C1} = \frac{\alpha * I_E}{1+exp(-\Delta V/V_T}$

$I_{C2} = \frac{\alpha * I_E}{1+exp(\Delta V/V_T}$

$\frac{I_{C1}}{I_{C2}} = \frac{V_{BE1}-V_{BE2}}{V_T}$

Case 1 (V_i = V_R) (both active)

* $I_{C1} = I_{C2}$
* $V_{C1} = V_{C2} = V_{CC} - I_{C1}R_C$

Case 2 (V_i > V_R)

* $I_{C1} rises => V_{C1} drops$
* $I_{C2} falls => V_{C2} incr$

Case 3 (V_i < V_R)

$I_{C2} rises => V_{C2} drops$

$I_{C1} falls => V_{C1} incr$

I_E is approx constant

$\Delta V = +120mV$ turns off Q2

$\Delta V = -120mV$ turns off Q1

$V_{C1} - V_{C2}$ is proportional to V_i - V_R

Basic Integrated Circuit ECL OR/NOR Gate

Configuration:

* Q1A, Q1B - input transistors
* Q2 - reference transistor($V_R = V_{BB}$)
* Q3 - its base connected to V_{C1}
* Q4 - its base connected to V_{C2}
* R_{E3}, R_{E4} - connected to - V_EE
* R_{C1}, R_{C2}
* R_{E} connected to V_E to -V_EE
* NOR output - V_{E3}
* OR ouput - V_{E4}

Purpose of Q3 and Q4:

* so if you add load ECL gates they can be driven
  * Between Cutoff and active region
* They operate in active mode and lower V_{C1} and V_{C2} by BE junction drops

How to find $V_{OH} and V_{OL}$

For V_OH

1.)Set V_{A} and V_{B} > V_{R}

2.)0-V_{E3} = .7 = V_{OH}

For V_OL

1.) set $V_A = V_{OH}, V_B = 0$

2.) Find V_E

3.)get $I_E = I_{C1}$

4.) $I_{C1} => V_{C1}$

5.) $V_{OL} = V_{E3} = V_{C1} - .7$

For V_BB

$V_R = \frac{V_{OH}+V_{OL}}{2}$

How to find $V_{IH} and V_{IL}$

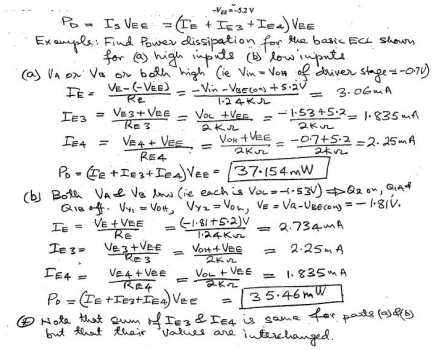
* $V_{IH} = V_R + .12$
* $V_{IL} = V_R - .12$

Disadvantages

* power dissipation is much higher than Saturating logic fams(active mode)

Power: $P_D = I_S V_{EE}$

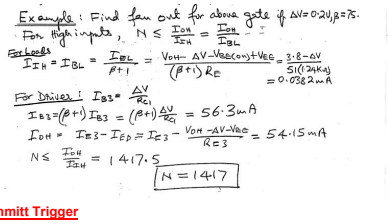
Example: Find Power for ECL NOR/OR IC gate



Fan-out

* calculated when inputs at logic low.
* Using output at Q3

Example: Find Fan out of a ECL NOR/OR IC gate



Schmitt Trigger

* They convert slowly varying voltage waveforms to well - defined logic levels with sharp transitions.
* $R_{C1} > R_{C2}$

Example: Find V_{OH}, V_{OL}, V_{tl} and V_{tu} for schmitt trigger

Case 1 ($0 < V_i < V_{tu}$)- [$V_i = 0, Q_1 = OFF, Q_2 = SAT$]

* $I_{C1} = I_{B2}$
* $V_o = V_{C2} = V_{OL} = V_{CC} - I_{C2}R_{C2}$

Steps(finding V_{tu})

$\frac{V_E}{R_E} = \frac{V_{CC} - (V_E + .8)}{R_{C1}} + \frac{V_{CC} - (V_E + .1)}{R_{C2}}$

solve for V_E

$V_{OL} = V_E + V_{CE2} = 1.92V$

Case 2 ($V_i = V_{tu}$) - [$V_i = V_E + .6, Q_1 = almostSat, Q_2 = OFF$]

* $V_{CE1} = V_{BE2} = .1V$
* $V_{OH} = V_{CC}$

Steps Continued(finding V_{tu})

$V_i = V_{tu} = V_E + .6$

Case 3 ($V_i = V_{tu}$)[$V_{BE2} = .6V$, $V_{BE1} = decr, Q_1 = OFF, Q_2 = active$]

Steps(finding V_{tl})

$V_i is decreased$

$I_{C1} = I_E = \frac{V_{CC} - .6}{R_{C1} + R_E} = .88mA$

$V_E = R_E * I_E$

$V_i = V_{tl} = V_E + .7 = 1.58$

The 555 Timer Integrated Circuit

Configuration:

* Two comparators C1 and C2
* RS latch F(using !Q)
* One BJT (Q1), R_B
* Output driver (inverterting amp)
* $V_{tu} = (2/3)V_{CC}$
* $V_{tl} = (1/3)V_{CC}$
* Three resistors near comps input R_T
* R - input Comp 1
* S - input comp 2

Monostable Multivibrator Operation(one shot)

* $V_{Th} = V_{cap}$

Stable Case V_o = 0

* S and R are logic low
* !Q = 1
* $V_{trig} > V_{CC}/3$
* C is discharged by Q1 which is on

Unstable Case V_o != 0

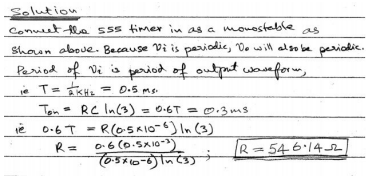
* $V_{trig} < V_{CC}/3$
* comp C2 goes high => sets
* !Q = 0 => Q1 isn't on C does not discharge
* At time T , $V_{Th} = V_{+,C1} == (2/3)V_{CC}$
  * R is set and !Q = 1

$T = RCln(3)$

Example: Monostable 555 Timer conf

Given: C=.5uF, f_{input} = 2kHz, dutyC_{input} = 95%, 0-5V pulse

Find: Design a circuit such that when above the output is 60 duty cyc 0-5V



Astable Multivibrator Operation(running free)

* $V_{cap} = V_{+,C1} = V_{-,C2}$
* R_{A} connected at V_{CC}
* R_B at node connecting discharge, and R_A
* C node below R_B
* Trigger input and threshold input are both connected Cap

!Q = high case

* Cap discharges via R_B

!Q = low

* Cap charges via R_A and R_B

Operation reapeats (Assume !Q=0 initially)

* Cap begins to charge toward V_{CC}
  * With $= (R_A + R_B)C$

At $V_C = V_{tl} = (1/3)V_{CC}$

* C_2 = logic low (no effect on F)

At $V_C = V_{tu} = (2/3)V_{CC}$ (discharging)

* C_1 = output logic high (resetting latch)
* Q_1 = on, cap begins to discharge
* toward zero with init val of (2/3)V_{CC}
  * With $= R_B * C$

At $V_C = V_{CC}/3$ (output of C2) changes logic high

* !Q goes low and latch is set

Equations:

$T_{on} = (R_A + R_B)Cln(2)$

$T_{off} = R_B * Cln(2)$

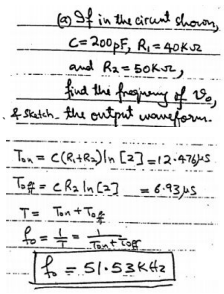
Period of the square wave becomes:

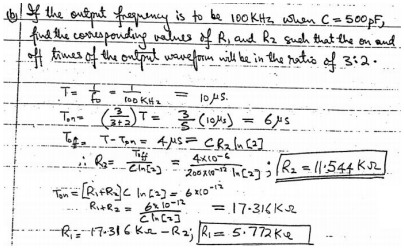
$T = T_{on} + T_{off} = (R_A + 2R_B)C * ln(2)$

$Duty\ Cycle = \frac{T_{on}}{T} = \frac{R_A + R_B}{R_A + 2*R_B}$

Example: (a)Find frequency of Vo

(b) Find R1 and R2 such that





Examples:

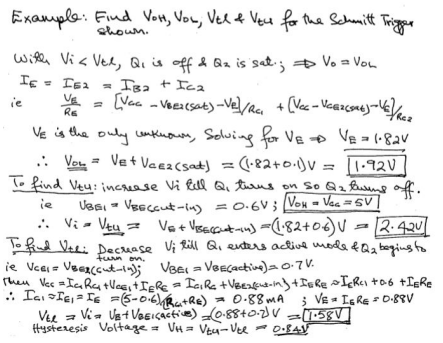
At Complete the design of 555 astable mv by choosing RA and RB

Given: V_{CC}, C, $DC_{output} = .60, f = 2khz$

$T_{off} = \frac{1}{f} - \frac{DC}{f} = R_B * C * ln(2)$

$T_{on} = \frac{DC}{f} = (R_A + R_B)C * ln(2)$

b. In EC schmitt trigger output Vtu. Find Vtu.



For the depletion NMOS inverter

Given: $k_D, k_L, V_{TD}, V_{TL} and V_{DD}$

a.Find $V_i (V_o = 3.5V)$

$k_D(V_i - V_{TD})^2 = k_L[2|V_{TL}|(V_{DD} - V_o) - (V_{DD} - V_o)^2]$

a.Find $V_{OL} = V_o (V_i = V_{DD})$

Example: advantages

1 ECL over TTL:

* Switching speed a lot faster

1 CMOS gate over TTL:

* Fanout is large for Cmos compared to TTL

5.ECL OR/NOR gate

a.) In ECL gate find R_{C1}, R_{C2} an R_E

Given: $V_{BE(on)}, V_R, V_{OH}, V_{OL}, I_E (Q1A = high, Q1B = off)$

Case 1 : Q_{1A} = active, Q_{1B} = off, Q_2 = off

Solve For R_A

$V_{B3} = V_{C1} = V_{BE3(active)} + V_{OL}$

$I_E = I_{C1} = \frac{V_{CC} - V_{C1}}{R_{C1}}$

Solve For R_E

$V_A - V_E = V_{BEA(active)}$

$I_E = \frac{V_E + V_{EE}}{R_E} = \frac{(V_A - V_{BEA(active)}) + V_{EE}}{R_E}$

Case 2 : Q_{1A} and Q_{1B} off, Q_2 = ON

Solve for R_{C2}

$V_E = V_R - V_{BE(act)}$

$I_E = I_{C2} = \frac{V_{CC} - (V_{BE(act)} - V_{OL})}{R_{C2}} = \frac{V_R - V_{BE(act)} + V_{EE}}{R_E}$

NMOS NOR and CMOS

(i) 3 inputs NOR gate:

NMOS in parallel a depletion nmos for load.

Gate of load connected to its drain.

(ii) 3 inputs CMOS NOR:

NMOS in parallel a depletion nmos for load.

PMOS in series (arrow goes on top facing line)

Finding IDMAX

*M_N and M_p both in sat

*Set Currents equal using Vi=Vo=V_M

*Solve for V_M then plug back into a current