

Configuration:

- * Q1 - input transistors
- * Q2 - reference transistor
- * Emitter of both connected
- * R_E connected to E node to $-V_{EE}$
- * Two R_C's

R_C and R_E are chosen such that for $V_{I1} = V_{I2}$, $Q1=Q2=active$

Note: usually ignore base current

$$\Delta V = V_{BE1} - V_{BE2} = V_I - V_R$$

$$I_{C1} = \frac{\alpha I_E}{1 + \exp(\Delta V / V_T)}$$

$$I_{C2} = \frac{\alpha I_E}{1 + \exp(\Delta V / V_T)}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{V_{BE1} - V_{BE2}}{V_T}$$

Case 1 ($V_I = V_R$) (both active)

- * $I_{C1} = I_{C2}$
- * $V_{C1} = V_{C2} = V_{CC} - I_{C1} R_C$

Case 2 ($V_I > V_R$)

- * I_{C1} rises $\Rightarrow V_{C1}$ drops
- * I_{C2} falls $\Rightarrow V_{C2}$ rises

Case 3 ($V_I < V_R$)

- * I_{C1} rises $\Rightarrow V_{C1}$ drops
- * I_{C2} falls $\Rightarrow V_{C2}$ rises

I_{C1} falls $\Rightarrow V_{C1}$ rises

I_E is approx constant

$\Delta V = +120mV$ turns off Q2

$\Delta V = -120mV$ turns off Q1

$V_{C1} - V_{C2}$ is proportional to $V_{I1} - V_{I2}$

Basic Integrated Circuit ECL OR/NOR Gate

Configuration:

- * Q1A, Q1B - input transistors
- * Q2 - reference transistor ($V_R = V_{BB}$)
- * Q3 - its base connected to V_{C1}
- * Q4 - its base connected to V_{C2}
- * R_{E3}, R_{E4} - connected to $-V_{EE}$
- * R_{C1}, R_{C2}
- * R_{E1} connected to V_{E1} to $-V_{EE}$
- * NOR output - V_{C3}
- * OR output - V_{C4}

Purpose of Q3 and Q4:

- * so if you add load ECL gates they can be driven
- * Between Cutoff and active region
- * They operate in active mode and lower V_{C1} and V_{C2} by BE junction drops

How to find V_{OH} and V_{OL}

For V_{OH}

1.) Set V_{C1} and $V_{C2} > V_{R1}$

2.) $V_{C1} - V_{C2} = 7 = V_{C1} - V_{OH}$

For V_{OL}

1.) set $V_A = V_{OH}$, $V_B = 0$

2.) Find V_E

3.) get $I_E = I_{C1}$

4.) $I_{C1} \Rightarrow V_{C1}$

5.) $V_{OL} = V_{E3} = V_{C1} - 7$

For V_{BB}

$$V_R = \frac{V_{OH} + V_{OL}}{2}$$

How to find V_{IH} and V_{IL}

* $V_{IH} = V_R + .12$

* $V_{IL} = V_R - .12$

Disadvantages

- * power dissipation is much higher than Saturating logic fams (active mode)

Power: $P_D = I_S V_{EE}$

Example: Find Power for ECL NOR/OR IC gate

- $P_D = I_S V_{EE} = (I_E + I_{E3} + I_{E4}) V_{EE}$
- Example: Find Power dissipation for the basic ECL shown for (a) high inputs (b) low inputs
- (a) V_A or V_B on both high (ie $V_{in} = V_{OH}$ of driver stage = 0.7V)
- $$I_E = \frac{V_{E1} - (V_{BE})}{R_E} = \frac{-1.53 - (-1.53)}{2k\Omega} = 3.06mA$$
- $$I_{E3} = \frac{V_{E3} + V_{BE}}{R_{E3}} = \frac{V_{OH} + V_{BE}}{2k\Omega} = \frac{0.7 + (-1.53)}{2k\Omega} = 1.835mA$$
- $$I_{E4} = \frac{V_{E4} + V_{BE}}{R_{E4}} = \frac{V_{OH} + V_{BE}}{2k\Omega} = \frac{0.7 + (-1.53)}{2k\Omega} = 1.835mA$$
- $$P_D = (I_E + I_{E3} + I_{E4}) V_{EE} = 3.7154mW$$
- (b) Both V_A and V_B low (ie each is $V_{OL} = -1.53V$) $\Rightarrow Q2$ on, $Q1A$ off, $V_{in} = V_{OL}$, $V_{Y1} = V_{OL}$, $V_E = V_A - V_{BE(ON)} = -1.81V$
- $$I_E = \frac{V_E + V_{EE}}{R_E} = \frac{-1.81 + (-1.53)}{2k\Omega} = 2.734mA$$
- $$I_{E3} = \frac{V_{E3} + V_{BE}}{R_{E3}} = \frac{V_{OH} + V_{BE}}{2k\Omega} = 2.25mA$$
- $$I_{E4} = \frac{V_{E4} + V_{BE}}{R_{E4}} = \frac{V_{OL} + V_{BE}}{2k\Omega} = 1.835mA$$
- $$P_D = (I_E + I_{E3} + I_{E4}) V_{EE} = 3.546mW$$
- (c) Note that sum of I_{E3} and I_{E4} is same for pairs (a) & (b) but that their values are interchanged.

Fan-out

- * calculated when inputs at logic low.

- * Using output at Q3

Example: Find Fan out of an ECL NOR/OR IC gate

- Example: Find fan out for above gate if $\Delta V = 0.2V$ p.p.s.
- For high inputs, $N \leq \frac{I_{E1}}{I_{E2}}$
- $$I_{E1} = I_{E2} = \frac{I_{E1}}{\beta + 1} = \frac{V_{OH} - V_{BE(ON)} + V_{EE}}{\beta + 1} = \frac{0.7 - (-1.53) + (-1.53)}{51(20k\Omega)} = 0.0722mA$$
- For low inputs: $I_{E3} = \frac{\Delta V}{R_{C1}}$
- $$I_{E3} = (\beta + 1) I_{E2} = (\beta + 1) \frac{\Delta V}{R_{C1}} = 56.3\mu A$$
- $$I_{E1} = I_{E3} - I_{E2} = I_{E3} - \frac{V_{OH} - V_{BE(ON)} + V_{EE}}{\beta + 1} = 54.15\mu A$$
- $$N \leq \frac{I_{E1}}{I_{E3}} = 1417$$

Schmitt Trigger

- * They convert slowly varying voltage waveforms to well - defined logic levels with sharp transitions.

Example: Find V_{OH} , V_{OL} , V_{TH} and V_{TL} for schmitt trigger**Case 1 ($0 < V_i < V_{th}$) [$V_i = 0, Q1 = OFF, Q2 = SAT$]**

- * $I_{C1} = I_{B2}$
- * $V_o = V_{C2} = V_{OL} = V_{CC} - I_{C2} R_{C2}$

Steps (finding V_{th})

$$\frac{V_E}{R_E} = \frac{V_{CC} - (V_E + S)}{R_{C1}} + \frac{V_{CC} - (V_E + 1)}{R_{C2}}$$

solve for V_E

$$V_{OL} = V_E + V_{CE2} = 1.92V$$

Case 2 ($V_i = V_{th}$) [$V_i = V_E + .6, Q1 = OFF, Q2 = OFF$]

- * $V_{C1} = V_{BE2} = .1V$

$$V_{OH} = V_{CC}$$

Steps Continued (finding V_{th})

$$V_i = V_{th} = V_E + .6$$

Case 3 ($V_i = V_{th}$) [$V_{BE2} = .6V, V_{BE1} = decr, Q1 = OFF, Q2 = active$]**Steps (finding V_{th})**

V_{th} decreased

$$I_{C1} = I_E = \frac{V_{CC} - .6}{R_{C1} + R_E} = .88mA$$

$$V_E = R_E * I_E$$

$$V_i = V_{th} = V_E + .7 = 1.58$$

The 555 Timer Integrated Circuit**Configuration:**

- * Two comparators C1 and C2
- * RS latch F (using IQ)
- * One BJT (Q1), R_B
- * Output driver (inverting amp)
- * $V_{th} = (2/3)V_{CC}$
- * $V_{il} = (1/3)V_{CC}$
- * Three resistors near comps input R_T
- * R - input Comp 1
- * S - input comp 2

Monostable Multivibrator Operation (one shot)

- * $V_{TH} = V_{cap}$

Stable Case $V_o = 0$

- * S and R are logic low
- * IQ = 1
- * $V_{TH} > V_{CC}/3$
- * C is discharged by Q1 which is on

Unstable Case $V_o = 1$

- * $V_{TH} < V_{CC}/3$
- * comp C2 goes high \Rightarrow sets
- * IQ = 0 \Rightarrow Q1 isn't on C does not discharge
- * At time T, $V_{TH} = V_{C1} = (2/3)V_{CC}$
- * R is set and IQ = 1
- $T = RC \ln(3)$

Example: Monostable 555 Timer conf

Given: C = 5uF, f_{input} = 2kHz, duty C_{input} = 95%, 0.5V pulse

Find: Design a circuit such that when above the output is 60 duty cyc 0-5V

Solution
Construct the 555 timer in as a monostable as shown above. Because V_i is periodic, V_o will also be periodic.
Period of V_i is period of output waveform,
ie $T = \frac{1}{f_{input}} = 0.5ms$
$T_{on} = RC \ln(3) = 0.6T = 0.3ms$
ie $0.6T = R(0.5 \times 10^{-3}) \ln(3)$
$R = \frac{0.6(0.5 \times 10^{-3})}{(0.55 - 0.6) \ln(3)}$; $R = 54.6k\Omega$

Astable Multivibrator Operation (running free)

- * $V_{cap} = V_{C1} = V_{C2}$
- * R_{A} connected at V_{C1}
- * R_B at node connecting discharge, and R_A
- * C node below R_B
- * Trigger input and threshold input are both connected Cap
- IQ = high case**
- * Cap discharges via R_B
- IQ = low**
- * Cap charges via R_A and R_B

Operation repeats (Assume IQ=0 initially)

- * Cap begins to charge toward V_{CC}
- * With $= (R_A + R_B)C$

$$\text{At } V_C = V_{il} = (1/3)V_{CC}$$

- * C_2 = logic low (no effect on F)

$$\text{At } V_C = V_{th} = (2/3)V_{CC} \text{ (discharging)}$$

- * C_1 = output logic high (resetting latch)
- * Q_1 = on, cap begins to discharge
- * toward zero with init val of $(2/3)V_{CC}$
- * With $= R_B * C$

$$\text{At } V_C = V_{CC}/3 \text{ (output of C2) changes logic high}$$

- * IQ goes low and latch is set

Equations:

$$T_{on} = (R_A + R_B)C \ln(2)$$

$$T_{off} = R_B * C \ln(2)$$

Period of the square wave becomes:

$$T = T_{on} + T_{off} = (R_A + 2R_B)C * \ln(2)$$

$$\text{Duty Cycle} = \frac{T_{on}}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

Example: (a) Find frequency of V_o

(b) Find R1 and R2 such that

(a) If in the circuit shown,
$C = 200pF, R_1 = 40k\Omega$
and $R_2 = 50k\Omega$
find the frequency of V_o
& sketch the output waveform.
$T_{on} = C(R_1 + R_2) \ln(2) = 12.47\mu s$
$T_{off} = C R_2 \ln(2) = 6.93\mu s$
$T = T_{on} + T_{off}$
$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}}$
$f = 51.53kHz$

(b) If the output frequency is to be 100kHz when $C = 500pF$, find the corresponding values of R_1 and R_2 such that the on and off times of the output waveform will be in the ratio of 3:2.

$T = \frac{1}{f} = \frac{1}{100kHz} = 10\mu s$
$T_{on} = \frac{3}{5} T = \frac{3}{5} (10\mu s) = 6\mu s$
$T_{off} = T - T_{on} = 4\mu s = C R_2 \ln(2)$
$\therefore R_2 = \frac{T_{off}}{C \ln(2)} = \frac{4 \times 10^{-6}}{200 \times 10^{-12} \ln(2)} ; R_2 = 11.544k\Omega$
$T_{on} = C(R_1 + R_2) \ln(2) = 6 \times 10^{-6}$
$R_1 + R_2 = \frac{6 \times 10^{-6}}{C \ln(2)} = 17.316k\Omega$
$R_1 = 17.316k\Omega - R_2 ; R_1 = 5.772k\Omega$

Examples:

At Complete the design of 555 astable mv by choosing R_A and R_B

Given: $V_{CC} = 5V, f_{output} = 60, f = 2kHz$

$$T_{off} = \frac{1}{f} - \frac{T_{on}}{f} = R_B * C * \ln(2)$$

$$T_{on} = \frac{T}{f} = (R_A + R_B)C * \ln(2)$$

b. In EC Schmitt trigger output V_{th} . Find V_{th} .

Example: Find V_{OH} , V_{OL} , V_{EH} and V_{EL} for the Schmitt Trigger shown.

With $V_i < V_{EH}$, Q_1 is off & Q_2 is sat; $\Rightarrow V_o = V_{OL}$

$$I_E = I_{E2} = I_{B2} + I_{E2}$$

$$\text{ie } \frac{V_E}{R_E} = \frac{(V_{CC} - V_{BE2(sat)}) - V_{C1}}{R_{C1}} + \frac{(V_{CC} - V_{BE2(sat)}) - V_{C2}}{R_{C2}}$$

V_E is the only unknown, Solving for $V_E \Rightarrow V_E = 1.92V$

$$\therefore V_{OH} = V_E + V_{BE2(sat)} = (1.92 + 0.1)V = 1.92V$$

To find V_{EH} : increase V_i till Q_1 turns on so Q_2 turns off.

$$\text{ie } V_{BE1} = V_{BE2(sat)} - V_{C1} = 0.6V ; V_{OH} = V_{EH} = 6V$$

$$\therefore V_i = V_{EH} = V_E + V_{BE2(sat)} = (1.92 + 0.6)V = 2.42V$$

To find V_{EL} : decrease V_i till Q_1 enters active mode & Q_2 begins to turn on.

$$\text{ie } V_{BE1} = V_{BE2(sat)} - V_{C1} ; V_{BE1} = V_{BE2(sat)} = 0.7V$$

Then $V_E = I_{E1} R_{E1} + V_{BE1} + I_{E2} R_{E2} = I_{E1} R_{E1} + V_{BE2(sat)} + I_{E2} R_{E2} + I_{E1} R_{E1} + 0.6 + I_{E2} R_{E2}$

$$\therefore I_{E1} R_{E1} + I_{E2} R_{E2} = (0.6 - 0.6) R_{E1} + R_{E2} = 0.88mA ; V_E = I_{E1} R_{E1} + 0.88V$$

$$V_E = V_i = V_E + V_{BE2(sat)} = 0.88 + 0.1V = 1.58V$$

Hysteresis Voltage = $V_{EH} - V_{EL} = 0.84V$

For the depletion NMOS inverter

Given: k_D, k_L, V_{TD}, V_{TL} and V_{DD}

a. Find $V_i (V_o = 3.5V)$

$$k_D (V_i - V_{TD})^2 = k_L [2V_{TL} (V_{DD} - V_o) - (V_{DD} - V_o)^2]$$

a. Find $V_{OL} = V_o (V_i = V_{DD})$

Example: advantages

1 ECL over TTL:

- * Switching speed a lot faster
- * CMOS gate over TTL:
- * Fanout is large for CMOS compared to TTL

5.ECL OR/NOR gate

a.) In ECL gate find R_{C1} , R_{C2} and R_E

Given: $V_{BE(on)}, V_R, V_{OH}, V_{OL}, I_E (Q1A = high, Q1B = off)$

Case 1: Q_{1A} is active, Q_{1B} is off, Q_2 = off

Solve For R_A

$$V_{B3} = V_{C1} = V_{BE3(ON)} + V_{OL}$$

$$I_E = I_{C1} = \frac{V_{CC} - V_{C1}}{R_{C1}}$$

Solve For R_E

$$V_A - V_E = V_{BEA(ON)}$$

$$I_E = \frac{V_E + V_{EE}}{R_E} = \frac{(V_A - V_{BEA(ON)}) + V_{EE}}{R_E}$$

Case 2: Q_{1A} and Q_{1B} off, Q_2 = ON

Solve for R_{C2}

$$V_E = V_R - V_{BE(ON)}$$

$$I_E = I_{C2} = \frac{V_{CC} - (V_{BE(ON)} - V_{OL})}{R_{C2}} = \frac{V_R - V_{BE(ON)} + V_{EE}}{R_E}$$

NMOS NOR and CMOS

(i) 3 inputs NOR gate:

NMOS in parallel a depletion nmos for load.