Power Dissipation:

$P_D = I_{CC} * V_{CC}$

NPN BJT parameters:

Table 3.1 Modes of operation for a BJT

EBJ	CBJ	Mode
Forward	Reverse	Forward active
Reverse	Forward	Inverse active
Reverse	Reverse	Cutoff
Forward	Forward	Saturation

$I_C = \beta_i * I_B$

$I_E = (1 + \beta_i) * I_B$

$I_E = I_C + I_B$

β_i = mode that the Q is in

$$\beta = \frac{\alpha}{1-\alpha}$$

Table 4.1 Piecewise linear parameters for the diode and the BJT

Diode:	Cut-in voltage	0.6 V
	Forward voltage	0.7 V
BJT:	$V_{BE(cut-in)}$	0.6 V
	$V_{BE(active)}$	0.7 V
	$V_{BE(sat)}$	0.8 V
	$V_{CE(sat)}$	0.1 V

The BJT RTL Inverter

Unloaded BJT inverter

$V_{IL} = V_{BE(cut-in)} = .6V$

$V_O(V_i = 0V) = V_{OH} = V_{CC}$

$V_O(V_i = V_{CC}) = V_{OL} = V_{CE(sat)} = .1V$

$V_{IH} = I_{B(sat)} R_B + V_{BE(sat)}$

Example: For BJT inverter

Find: NM_H, NM_L

Given: $, V_{CC}, R_B, R_C, V_{CE(SAT)}$

Steps: $V_{IH} = I_{B(sat)} R_B + V_{BE(sat)}$

$\beta * I_{B(sat)} = I_{C(sat)}$

so, $NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

Loaded BJT inverter

k = Base overdrive factor

$k = \frac{I_{B(sat)}}{I_{B(EOS)}}$

* Assume k = 1, if not given

$$N <= \frac{\beta[V_{CC} - V_{IH}]}{k[V_{CC} - V_{CE(sat)}]}$$

Fan out = max number of gates inverter can drive while maintaining output logic high Condition for inverter to operate Properly.

$(NM_H = 0) : V_{OH} >= V_{IH}$

$N <= \frac{\beta * (V_{CC} - V_{IH})}{k[V_{CC} - V_{CE(sat)}]}$

$N_{max} <= \frac{\beta[V_{CC} - V_{BE(sat)}]}{k[V_{CC} - V_{CE(sat)}]} - \frac{R_B}{R_C}$

Example: Calculate Fan out of BJT RTL inv

Find: (a) N_{max}, (b) N (reduces NM_H to NM_L)

Given: β

Steps:

(a) Use N_{max} eqn above

(b) $NM_L = .6 - .1 = .5V$

$NM_H = .5 = V_{OH} - V_{IH} = NM_L$

$V_{IH} = I_{B(sat)} R_B + V_{BE(sat)}$

$I_{B(sat)} = R_B * \frac{V_{CC} - V_{CE(sat)}}{\beta R_C}$

$V_{OH} = 2V$

$\frac{[V_{CC} - V_{OH}]}{R_C} >= N[V_{OH} - V_B E(sat)]/R_B$

=> N = 25

Resistor - Transistor Logic (RTL) gate

NOR gate configuration Description

* Same as RTL inverter configuration but Q1 Is in parallel with Q2

Unloaded RTL NOR gate

$V_{IL} = V_{BE(cut-in)} = .6V$

$V_O(V_i = 0V) = V_{OH} = V_{CC}$

$V_O(V_i = V_{CC}) = V_{OL} = V_{CE(sat)} = .1V$

$V_{IH} = I_{B(sat)} R_B + V_{BE(sat)}$

Loaded RTL gate

$V_{OL} = .1V$

$V_{IL} = .6V$

$V_{IH} = V_{BE(sat)} + I_{B(sat)} R_B$

$V_{OH} = V_C C - N * I_{B(sat)} R_C$

Wired AND in RTL

* ANDing two NOR gates by just connecting their outputs, to a single node

* Wired AND in RTL is equivalent to single level logic with expanded fan-in

Disadvantage of BJT invert and RTL

-Low noise margin ($NM_L = .5V$)

-fan-out (loading) reduces V_{OH} and therefore reduces NM_H

Diode Transistor Logic (DTL):

Early Version of discrete DTL NAND:

Description: D1, D2, R2 at the base of Q, and -V_BB on R2.

Characteristics:

$V_{OH} = V_{CC} = 5V$

$V_{OL} = V_{CE(sat)} = .1V$

$V_{IL} = V_{BE(cut-in)} + 2 * V_{D(on)} - V_{D(on)} = 1.3V$

$V_{IH} = V_{BE(sat)} + 2 * V_{D(on)} - V_{D(on)} = .8V + .7V = 1.5V$

$NM_H = V_{OH} - V_{IH} = 3.5V$

$NM_L = V_{IL} - V_{OL} = 1.2V$

Fan-out:

* Found when Vo of driver is V_{OL}

* $N_{Max} <= \frac{I_{OL}}{I_{IL}}$

Advantages:

* High noise Margins

* Loading does not degrade V_{OH} or NM_H

Example: Calculate Max Fan Out of Discrete DTL

Find: N_{max}

Given: R1 - above input diodes (DA, DB)

RC - collector of Q

R2 - base of Q2, to supply V_BB

Q - saturated

$I_{IL} = \frac{V_{CC} - V_{CE(sat)} - V_{D(ON)}}{R_1} - \frac{V_{CC} - V_{CE(sat)} - 2 * V_{D(ON)} + V_{BB}}{R_2}$

$I_{OL} = \beta * I_B - \frac{V_{CC} - V_{CE(sat)}}{R_C}$

$I_B = I_1 - I_2$

$I_1 = \frac{V_{CC} - V_{BE(sat)} - 2 * V_{D(ON)}}{R1}$

$I_2 = \frac{V_{BE(sat)} - (-V_{BB})}{R_2}$

$N_{Max} <= \frac{I_{OL}}{I_{IL}}$

IC Version of DTL NAND:

Description: Same as Discrete version but with D1 replacing Q1, Q1's collector loop back to base through a resistor. No power supply

Characteristics:

*Same as the Discrete DTL NAND above

Advantages:

- No extra power supply
- Increase in $V_{IL}, and Fanout$

Example: Calculate Max Fan Out of IC DTL

Find: N_{max}

Given: R2 - Q1 loop back through C-B,

R1 - above R2

R3 - base of Q2

R4 - collector of Q2

Q - saturated

$I_{IL} = \frac{V_{CC} - V_{CE1(sat)} - V_{D(ON)}}{R_1 + R_2}$

$I_{OL} = \beta * I_{B2} - \frac{V_{CC} - V_{CE2(sat)}}{R_4}$

$N_{Max} <= \frac{I_{OL}}{I_{IL}}$

Wired - AND implementation DTL gate

Y = Y1*Y2 = ~(A*B)*~(C*D) = ~(A*B+C*D)

*Cant be increased in fan-in of DTL as wired AND was increased in fan-in of RTL

High-Threshold DTL NAND gate

Description:

Increased noise margins of a DTL gate. Using a zener diode reverse bias in place of D1 in IC version DTL.

Advantages:

-Resistances are higher

-Increase in propagation delay

-Higher supply voltage

-High noise margins

Example:Calculate V_IH,V_IH and NM's

Find: NM_H, NM_L

Given: V_{OH} = 15V, V_{OL} = .1V, V_Z = 6.9V

$V_{IH} = V_{BE2(sat)} + V_Z + V_{BE1(active)} - V_{D(ON} = 7.7V$

$V_{IL} = V_{BE2(cut-in)} + V_Z + V_{BE1(ON)} - V_{D(ON)}$

$NM_H = 7.3V$

$NM_H = 7.4V$

Transistor Transistor Logic (TTL):

Multi-emitter Transistor Characteristic:

If all M emitter inputs are logic high - they "Multiple transistor" operate in RA mod; driving Q2 into saturation and drawing logic high current:

$I_{EA} = I_{EB} = -\beta_R * \frac{I_{B1}}{M} = I_{IH}$

Transistor Transistor Standard Logic (TTL):

Description:

Input Stage

* Multi-Emitter Transistor

* Emitter terminals as inputs

Phase-Splitter stage

* Q2, ensures only Q4, or Q3 is turned on for any input, (Totem-Pole)

* Q2, increases the logic low level V_{IL}

Output Stage

* Q4, on top and Q3 on the bottom of pole

Characteristics (3 BPS):

Table 4.2 Modes of operation of transistors in a standard TTL circuit

Input	Q_1	Q_2	Q_3	Q_4
Low (≤ 0.5 V)	Saturation	Off	Off	Active
0.5 to 1.2 V	Saturation	Active	Off	Active
1.2 to 1.6 V	Reverse active	Saturation	Active	Active
High (≥ 1.6 V)	Reverse active	Saturation	Saturation	Off

BP1: $V_i = .5V = V_{IL}$, $V_O = V_OH = 3.8$

BP2: $V_i = 1.2V$, $V_o = 2.6$

BP3: $V_i = 1.6V = V_{IH}$, $V_o = V_{OL} = .1$

$V_{OH} = 3.8V$, $V_{OL} = 0.1V$

Fan out for TTL (2 types):

Given: R1 - base of Q1

R2 - emitter of Q2

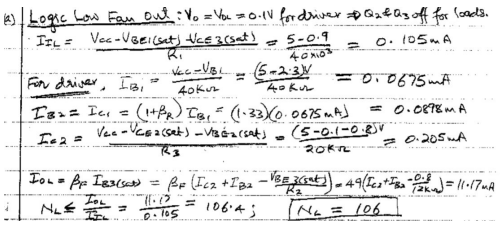
R3 - collector of Q2, base Q4

R4 - collector of Q4

M - number of inputs

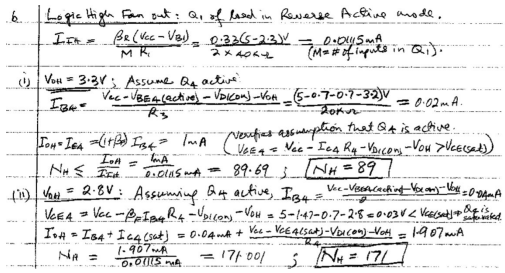
Example: Find Logic Low fan out STD TTL

Determined by the amount of current Q3 can sink (draw) and still be in saturation



Example: Find Logic High fan out STD TTL

Determined by the amount of current Q4, and D1 can provide w/o going out of the active mode



Advantages TTL:

1.) Q2 turns on faster than in basic DTL (smaller propagation delay)

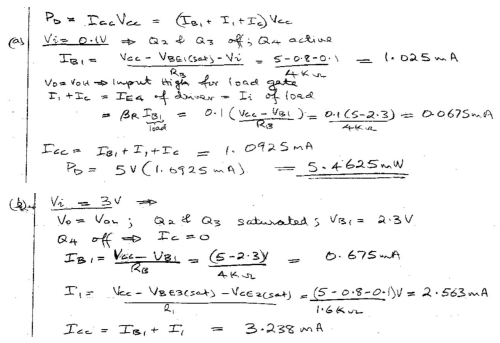
2.) Current gain from Q2 to Q3, fast turn on of Q3 => reduces t_{pHL}

4.) increase Fan out

5.) Smaller Power Dissipation

Q3 and Q4 not on at same time except when one is turning on and the other off

Example:Calculate Power Dissipation STD TTL for a.) Vi = .1V b.) Vi = 3V. R1 is split Q2 and Q4



High-Speed TTL gate:

Advantages:

Q_4 turns on faster because of Q_1, hence faster pull-down and removal of knee of VTC.

Q_3 sub-circuit is squaring circuit, removes knee of VTC, results in narrower transition width.

Q_5 and Q_6 form Darlington pair, hence faster pull-up.

SCHOTTKY Low Power TTL:

Advantages:

Schottky transistors never saturate, hence faster switching.

Q_5 and Q_6 form Darlington pair, hence faster pull-up.

Q_6 does not saturate: $V_{CE5} = V_{BC6} \approx 0.3$ V.

Q_3 - Squaring Circuit results in narrower transition width.

$Y = \begin{cases} \overline{A \cdot B}, \text{if } G = 1 \\ \text{Hi Z, if } G = 0 \end{cases}$

Tri State TTL NAND Gates

Standard TTL Wired AND

:t circuit problem when either x or y is low while the other is high, not recommended.

TTL Wired AND with Open Collector Gates

- R_c is passive pull up common to all the gates.
- R_c should not be too low since $I_{Rc} + I_{OL} \leq I_{csat}$ with only one gate low.
- R_c should not be too high since this would lower V_{OH}.