Computer Architecture and Operating Systems
Lecture 2: Data Representation

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Any Questions?

```
                .text
    __start:   addi t1, zero, 0x18
               addi t2, zero, 0x21
    cycle:     beq t1, t2, done
               slt t0, t1, t2
               bne t0, zero, if_less
               nop
               sub t1, t1, t2
               j cycle
               nop
    if_less:   sub t2, t2, t1
               j cycle
    done:      add t3, t1, zero
```