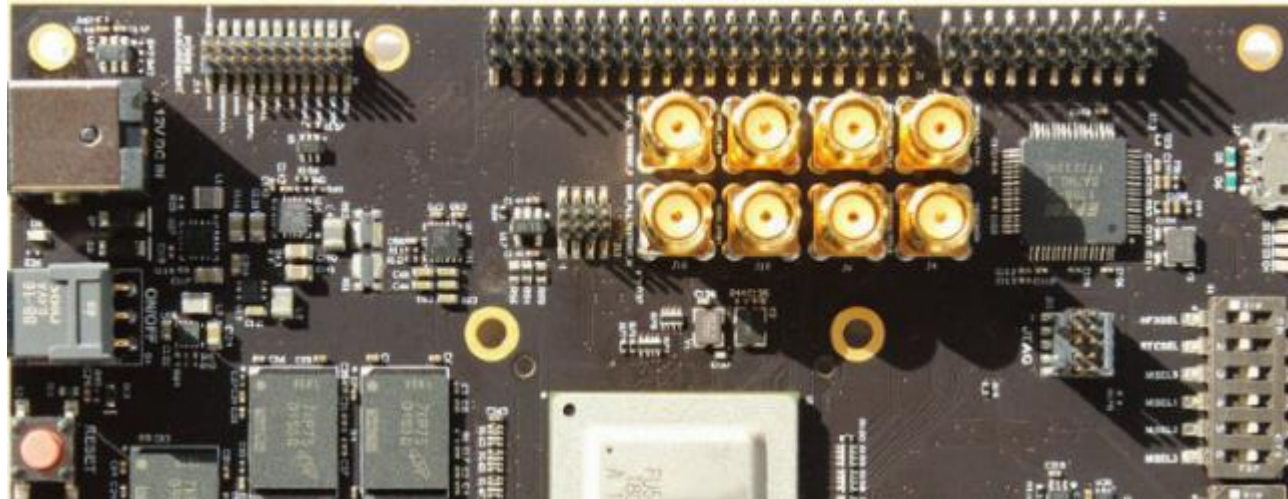# Computer Architecture and Operating Systems
Lecture 1: Introduction

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Course Resources

- **Wiki**

http://wiki.cs.hse.ru/ACOS_DSBA_2020/2021

- **Web site**

https://andrewt0301.github.io/hse-acos-course/

- **Telegram channel**

https://t.me/joinchat/AAAAAFDXhCd-WvYYZwBPGQ

Course Team

Instructors

Andrei Tatarnikov

Assistants

TODO

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Course Outline

Syllabus (see the web site for details)

- Module 3: Computer Architecture
  - Computer architecture
  - Assembly language programming (RISC-V)
  - Home works, quizzes, and test
- Module 4: Operating Systems
  - Operating System Architecture (Linux)
  - System programming in C
  - Home works, quizzes, and test
- Final Exam

Course Motivation

- Increase your computer literacy

- Have an idea how computers under the hood

- Better understand performance

- Be familiar with system programming

- Be familiar with system tools

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Python

Floating-point operations:

$$2 * n^3 = 2 * (2^{10})^3 = 2^{31}$$

Running time:

503.130450 sec.

Performance:

~ 4,27 MFLOPS

```python
import random
from time import time


n = 1024

A = [[random.random()
        for row in range(n)]
        for col in range(n)]
B = [[random.random()
        for row in range(n)]
        for col in range(n)]
C = [[0
        for row in range(n)]
        for col in range(n)]

start = time()
for i in range(n):
    for j in range(n):
        for k in range(n):
            C[i][j] += A[i][k] * B[k][j]
end = time()

print('%0.6f' % (end - start))
```

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Java

Floating-point operations:

$$2 * n^3 = 2 * (2^{10})^3 = 2^{31}$$

Running time:

12.946224 sec.

Performance:

~ 165 MFLOPS

```java
public class Matrix {
    static int n = 1024;
    static double[][] A = new double[n][n];
    static double[][] B = new double[n][n];
    static double[][] C = new double[n][n];

    public static void main(String[] args) {
        java.util.Random r = new java.util.Random();
        for (int i = 0; i < n; i++) {
            for (int j = 0; j < n; j++) {
                A[i][j] = r.nextDouble();
                B[i][j] = r.nextDouble();
                C[i][j] = 0;
            }
        }
        long start = System.nanoTime();
        for (int i = 0; i < n; i++) {
            for (int j = 0; j < n; j++) {
                for (int k = 0; k < n; k++) {
                    C[i][j] += A[i][k] * B[k][j];
                }
            }
        }
        long stop = System.nanoTime();
        System.out.println((stop - start) * 1e-9);
    }
}
```

C Language

Floating-point operations:

$$2 * n^3 = 2 * (2^{10})^3 = 2^{31}$$

Running time:

13.714264 sec.

Performance:

~ 153 MFLOPS

```c
#include <stdlib.h>
#include <stdio.h>
#include <sys/time.h>

#define n 1024
double A[n][n];
double B[n][n];
double C[n][n];

float tdiff(struct timeval *start, struct timeval *end) {
    return (end->tv_sec - start->tv_sec) +
        1e-6*(end->tv_usec - start->tv_usec);
}
int main(int argc, const char *argv[]) {
    for (int i = 0; i < n; i++) {
        for (int j = 0; j < n; j++) {
            A[i][j] = (double)rand() / (double)RAND_MAX;
            B[i][j] = (double)rand() / (double)RAND_MAX;
            C[i][j] = 0;
        }
    }
    struct timeval start, end;
    gettimeofday(&start, NULL);
    for (int i = 0; i < n; i++) {
        for (int j = 0; j < n; j++) {
            for (int k = 0; k < n; k++) {
                C[i][j] += A[i][k] * B[k][j];
            }
        }
    }
    gettimeofday(&end, NULL);
    printf("%0.6f\n", tdiff(&start, &end));
    return 0;
}
```

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C Language: Optimizations

Loop order: i, j, k

```c
for (int i= 0; i < n; i++) {
  for (int j= 0; j < n; j++) {
    for (int k= 0; k < n; k++) {
      C[i][j]+= A[i][k]*B[k][j];
    }
  }
}
```

Running time:
13.714264 sec.
Performance:
~ 153 MFLOPS

Loop order: i, k, j

```c
for (int i= 0; i < n; i++) {
  for (int k= 0; k < n; k++) {
    for (int j= 0; j < n; j++) {
      C[i][j]+= A[i][k]*B[k][j];
    }
  }
}
```

Running time
2.739385 sec.
Performance:
~ 795 MFLOPS

Loop order: k, j, i

```c
for (int i= 0; i < n; i++) {
  for (int j= 0; j < n; j++) {
    for (int k= 0; k < n; k++) {
      C[i][j]+= A[i][k]*B[k][j];
    }
  }
}
```

Running time:
19.074106 sec.
Performance:
~ 113 MFLOPS

Example: Matrix Multiplication (part 5)

| Feature	Specifiction
Model	MacBook Pro 9,1
Processor Name	Quad-Core Intel Core i7
Processor Speed	2,3 GHz
Number of Processors	1
Total Number of Cores	4
Floating-Point Operations per Cycle	4
L2 Cache (per Core)	256 KB
L3 Cache:	6 MB
Hyper-Threading Technology	Enabled
Memory	8 GB

Peak = $(2.3 * 10^9)$ * 1 * 4 * 4 = 36 800 MFLOPS

What affects performance?

| Hardware/Software Component	How It Affects Performance
Algorithm	Determines both the number of source-level statements and the number of I/O operations executed
Programming Language, Compiler, and Architecture	Determines the number of computer instructions for each source-level statement
Processor and Memory System	Determines how fast instructions can be executed
I/O System (Hardware and Operating System)	Determines how fast I/O operations may be executed

History: 0th Generation – Mechanical

- 1834–71: Analytical Engine designed by Charles Babbage

- Mechanical gears, where each gear represented a discrete value (0-9)

- Programs provided as punched cards

- Never finished due to technological restrictions


The Analytical Engine
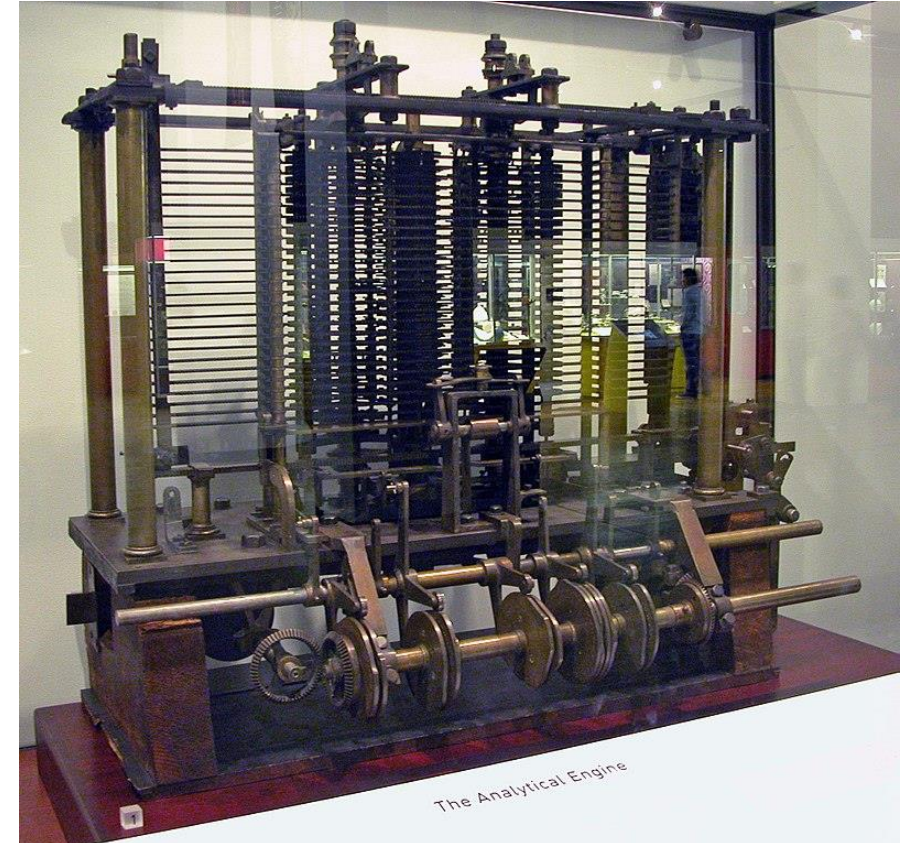
History: 1ˢᵗ Generation - Vacuum Tubes

- 1945–55: first machines were created (Atanasoff–Berry, Z3, Colossus, ENIAC)

- All programming in pure machine language

- Connecting boards and wires, punched cards (later)

- Stored program concept

Input

Arithmetical / Logic Unit

Memory

**Control Unit**

Output

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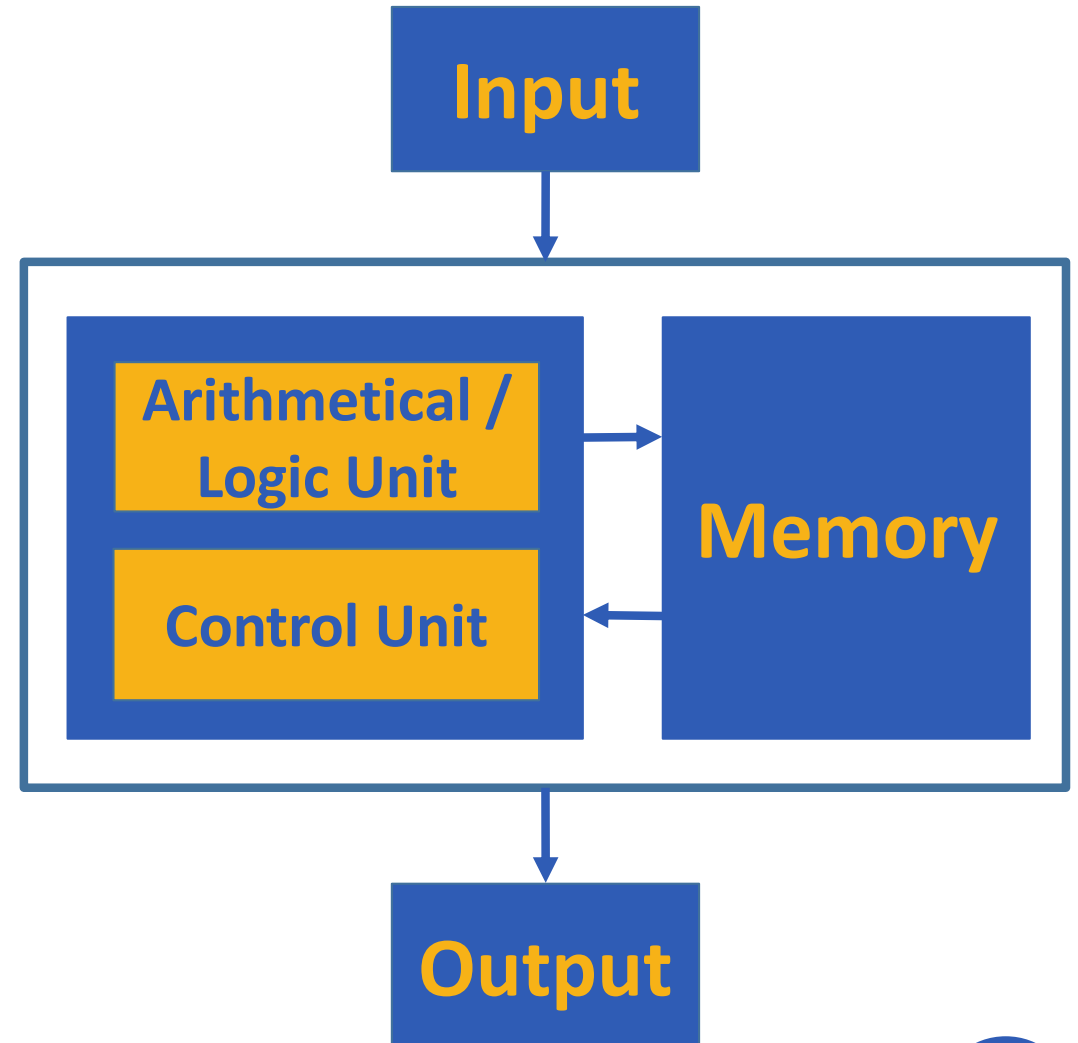
History: 2nd Generation - Transistors

- 1955–65: era of mainframes (e.g. IBM 7094) used in large companies
- Programming in assembly language and FORTRAN
- Batch systems (IO was separated from calculations)
- Punched cards and magnetic tape
- Loaders (OS ancestors)
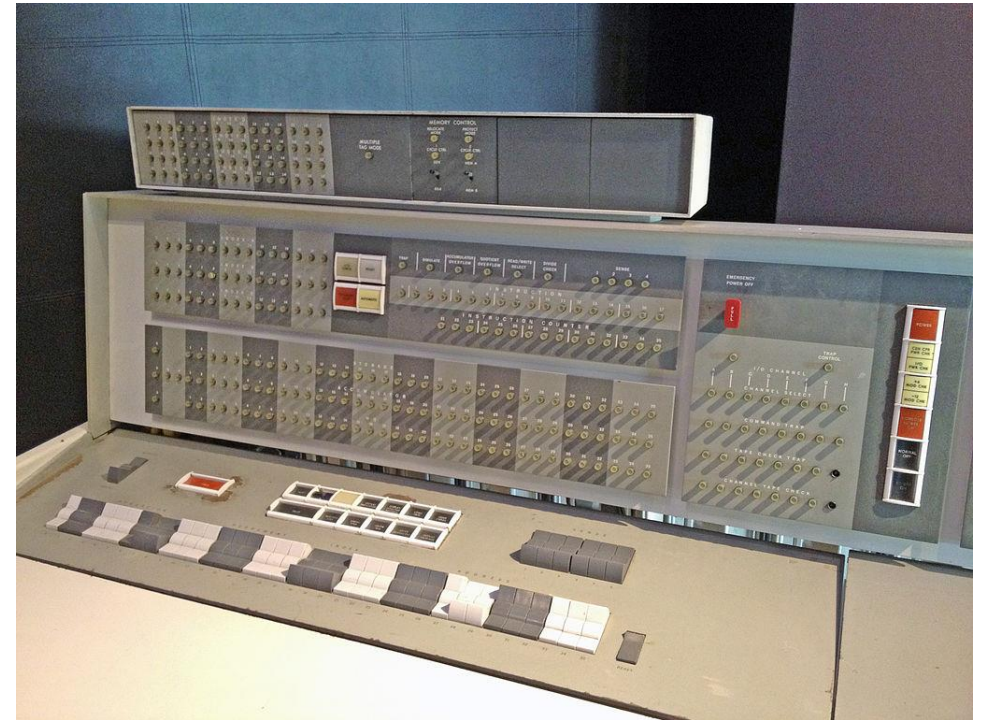
History: 3rd Generation – Integrated Circuits

- 1965–1980: computer lines using the same instruction set architecture (e.g. IBM 360)

- First operating systems (e.g. OS/360, MULTICS)

- Multiprogramming and timesharing

- Computer as utility

- Programming languages and compilers (LISP, BASIC, C)

Job 3
Job 2
Job 1
Operating System

Memory Partitions

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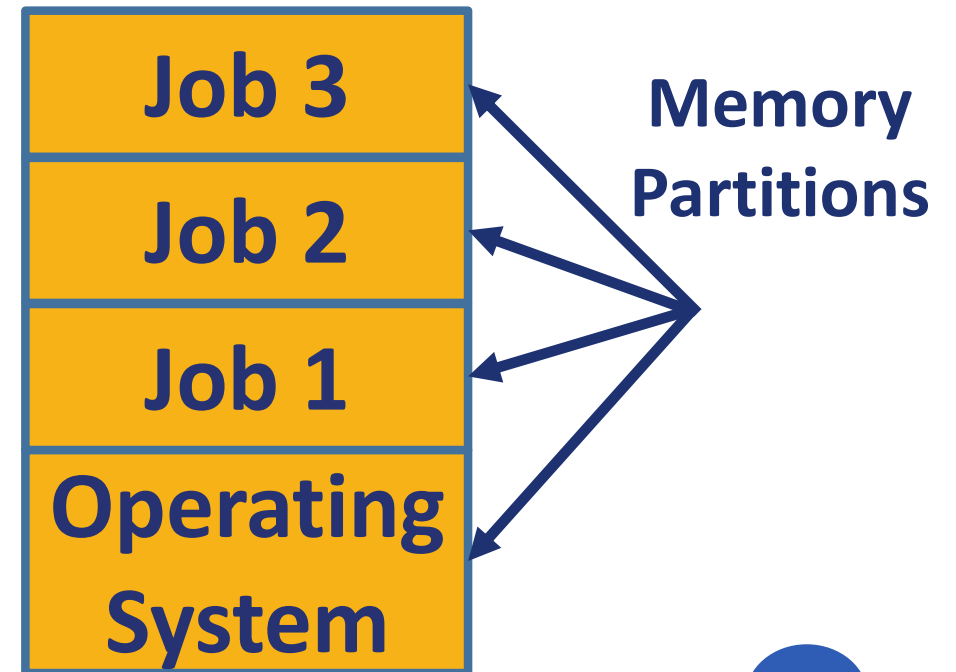
History: 4th Generation – VLSI and PC

- 1980–Present: personal computers, laptops, servers (Apple, IBM, etc.)

- Architectures: x86-64, Itanium, ARM, MIPS, PowerPC, SPARC, RISC-V, etc.

- Operating systems: UNIX (System V and BSD), MINIX, Linux, MacOS, DOS, Windows (NT)

- ISA (CISC, RISC, VLIW), caches, pipelines, SIMD, vectors, hyperthreading, multicore

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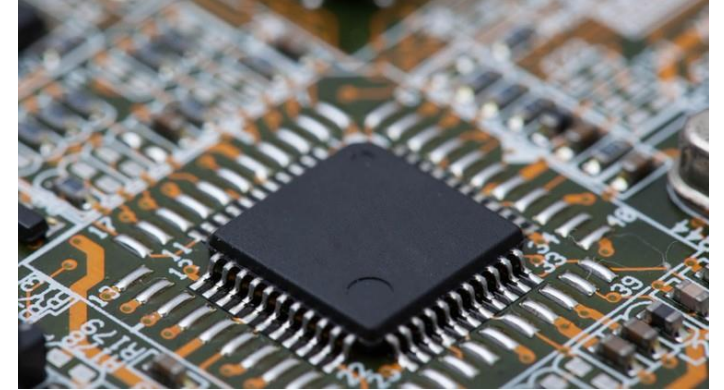
History: 5th Generation – Mobile devices

- 1990–Present: mobile devices, embedded systems, IoT devices

- Custom processors and FPGAs

- Mobile operating systems: Symbian, iOS, Android, Windows Mobile

- Real-time operating systems

Technology Trends

- Electronics technology continues to evolve
  - Increased capacity and performance
  - Reduced cost

Memory capacity
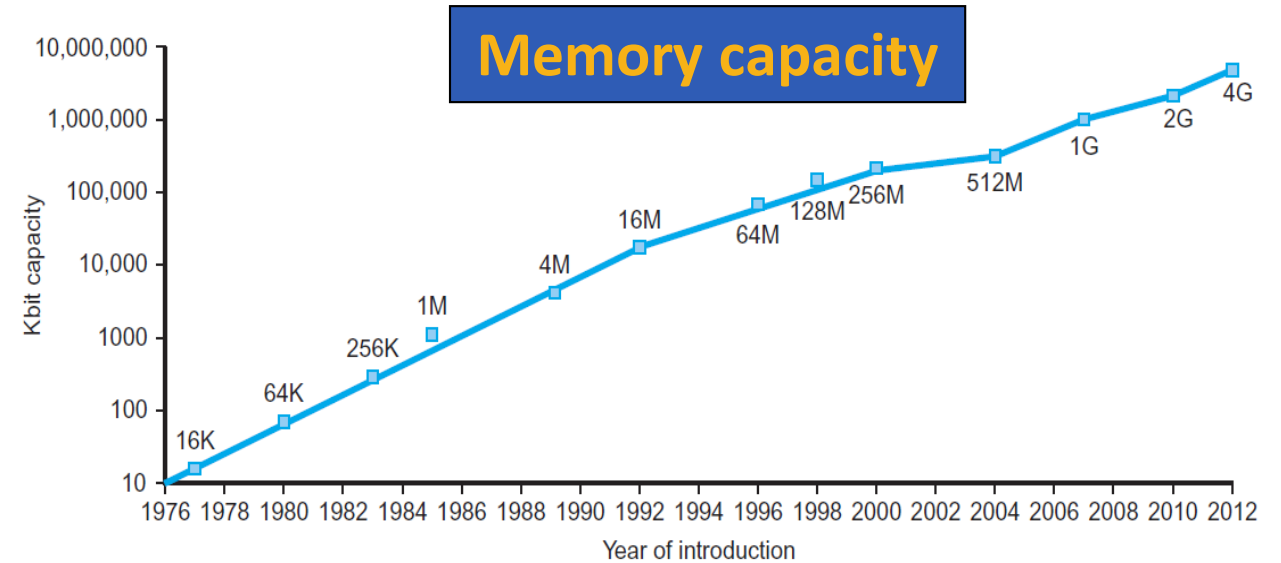
Year	Technology	Relative performance/cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit (IC)	900
1995	Very large scale IC (VLSI)	2,400,000
2013	Ultra large scale IC	250,000,000,000

Moore's Law

- Gordon Moore (1929-…) cofounded Intel in 1968 with Robert Noyce

- **Moore's Law:** number of transistors on a computer chip doubles every year (observed in 1965)

- Limited by power consumption

- Slowed down since 2010

Single Core Performance

Move to multicore

Intel Core i7 4 cores 4.2 GHz (Boost to 4.5 GHz)
Intel Core i7 4 cores 4.0 GHz (Boost to 4.2 GHz)
Intel Core i7 4 cores 4.0 GHz (Boost to 4.2 GHz)
Intel Xeon 4 cores 3.7 GHz (Boost to 4.1 GHz)
Intel Xeon 4 cores 3.6 GHz (Boost to 4.0 GHz)
Intel Xeon 4 cores 3.6 GHz (Boost to 4.0 GHz)
Intel Core i7 4 cores 3.4 GHz (boost to 3.8 GHz)
Intel Xeon 6 cores, 3.3 GHz (boost to 3.6 GHz)
Intel Xeon 4 cores, 3.3 GHz (boost to 3.6 GHz)
Intel Core i7 Extreme 4 cores 3.2 GHz (boost to 3.5 GHz)
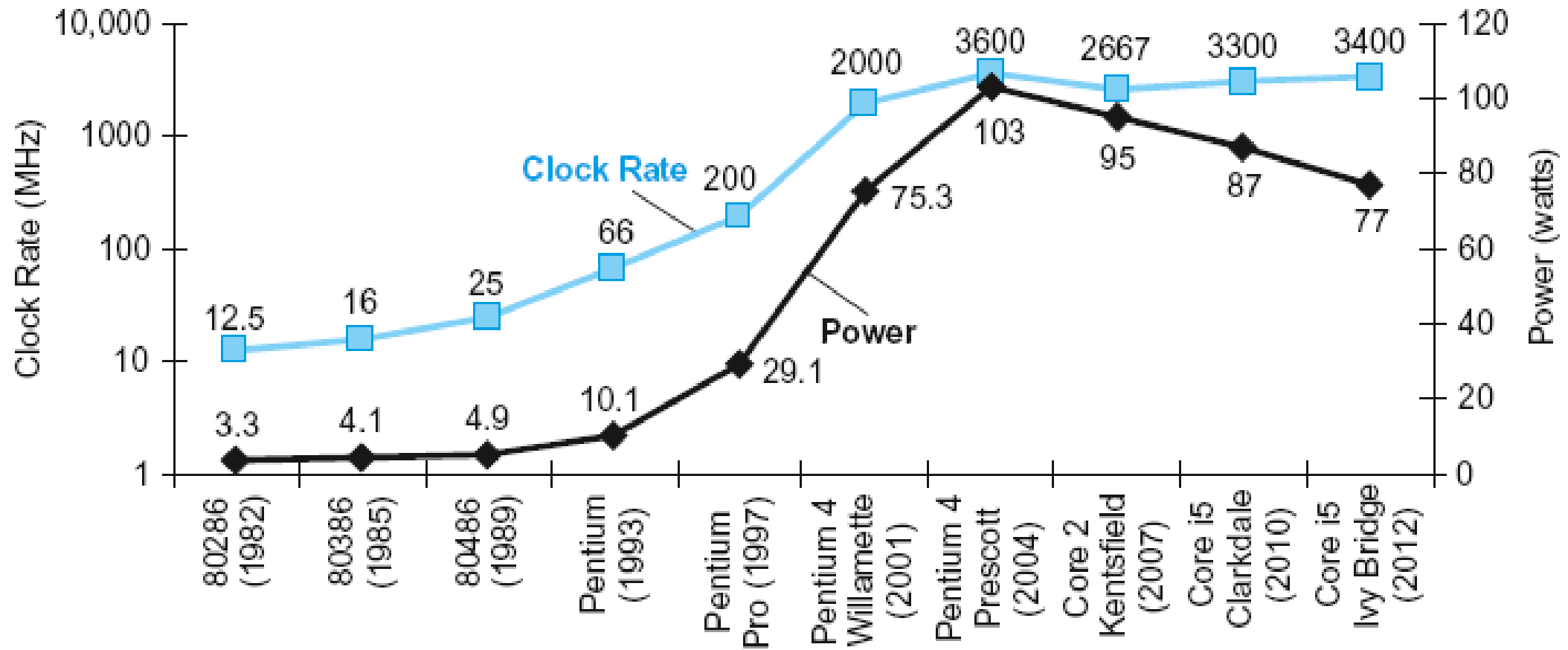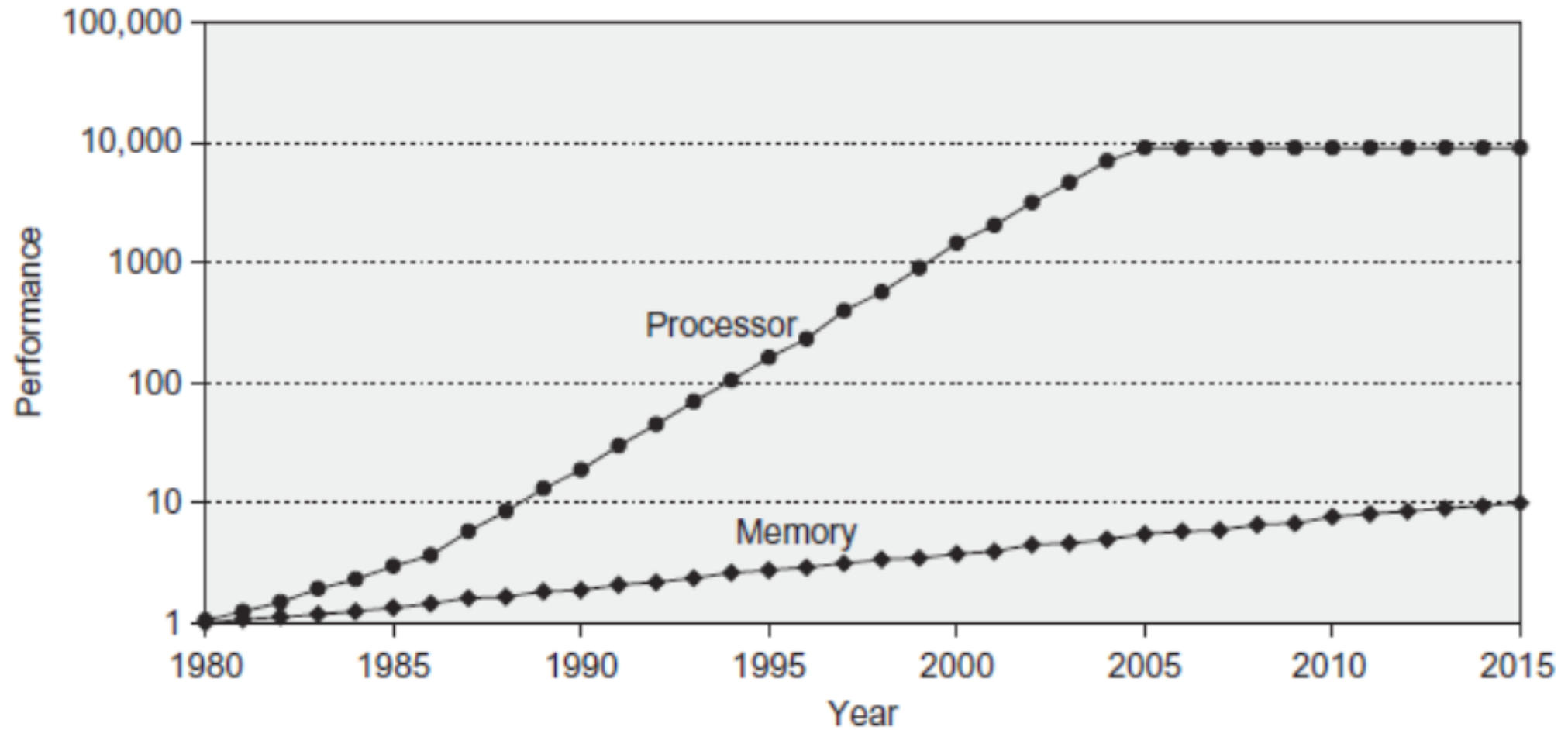Intel Core Duo Extreme 2 cores, 3.0 GHz
Intel Core 2 Extreme 2 cores, 2.9 GHz
AMD Athlon 64, 2.8 GHz
AMD Athlon, 2.6 GHz
Intel Xeon EE 3.2 GHz
Intel D850EMVR motherboard (3.06 GHz, Pentium 4 processor with Hyper-Threading Technology)
IBM Power4, 1.3 GHz
Intel VC820 motherboard, 1.0 GHz Pentium III processor
Professional Workstation XP1000, 667 MHz 21264A
Digital AlphaServer 8400 6/575, 575 MHz 21264
AlphaServer 4000 5/600, 600 MHz 21164
Digital Alphastation 5/500, 500 MHz
Digital Alphastation 5/300, 300 MHz
Digital Alphastation 4/266, 266 MHz
IBM POWERstation 100, 150 MHz
Digital 3000 AXP/500, 150 MHz
HP 9000/750, 66 MHz
IBM RS6000/540, 30 MHz
MIPS M2000, 25 MHz
MIPS M/120, 16.7 MHz
Sun-4/260, 16.7 MHz
VAX 8700, 22 MHz
AX-11/780, 5 MHz

100,000 — 10,000 — 1000 — 100 — 10 — 1

49,935
49,870
39,419
40,967 49,935
34,967
31,999
24,129
21,871
19,484
14,387
11,865
7,108
6,681
6,043
4,195
3,016
1,779
1,267
993
649
481
280
183
117
80
51
24
18
13
9
5

25%/year
52%/year
23%/year
12%/year
3.5%/year

1978 1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016 2018

Constrained by power, instruction-level parallelism, memory latency

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Power Trends

Memory Performance Gap

Current Challenges

- Single core performance improvement has ended
  - More powerful microprocessor might not help
- Memory-efficient programming
  - Temporal locality
  - Spatial locality
- Parallelism to improve performance
  - Data-level parallelism
  - Thread-level parallelism
  - Request-level parallelism
- Performance tuning require changes in the application

Conclusion

- To create software that efficiently deals with big data, we need to understand how hardware is organized and managed by operating system

  - Computer architecture

  - Assembly language

  - Compiler basics

  - Operating systems
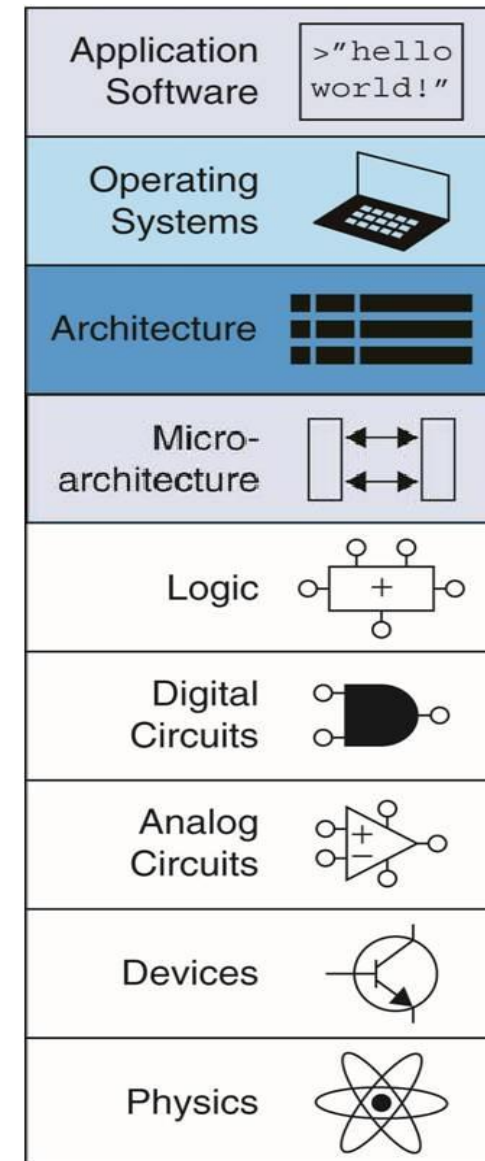
Focus of this course

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Any Questions?

```
                .text
__start:   addi t1, zero, 0x18
           addi t2, zero, 0x21
cycle:     beq t1, t2, done
           slt t0, t1, t2
           bne t0, zero, if_less
           nop
           sub t1, t1, t2
           j cycle
           nop
if_less:   sub t2, t2, t1
           j cycle
done:      add t3, t1, zero
```