Lyon, 69100
France
✳ 26 February 1995
📱 +33 7 70 49 11 98
✉ i.f.lledoux@gmail.com
🌐 bynaryman.github.io
in ledoux-louis
🐦 @L0u1s73doux
○ Bynaryman
ⓘ 0009-0006-3643-2157
Ⓢ JWBIqG8AAAAJ

Louis Ledoux

Philosophiae Doctor
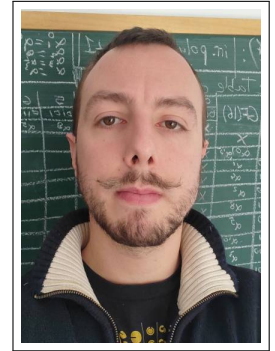
"Post Hoc Ergo Propter Hoc"

Research Interests

○ **Computer Architecture:** Floating-Point Units, Systolic Arrays, Matrix-Matrix Multiply (MMM) Units, GPUs, FPGAs, ASIC Design
○ **Computer Arithmetic:** Number Representations, FloPoCo, Posit & IEEE 754 Standards, Fixed-Point Polynomial Approximations, Accuracy–Energy Tradeoffs
○ **High Performance Computing:** BLAS, GEMMs, Heterogeneous Workloads, Numerical Analysis, Supercomputing
○ **End-to-End Design Philosophy:** From mathematical problem to silicon implementation, integrating MLIR-based compilation and open-source silicon flows for transparent and reproducible design

Experience

2025 – Now   **Postdoctoral Researcher**, *INSA/INRIA – Emeraude*, Lyon

Working on arithmetic compilation and optimization through the integration of *MLIR* and *FloPoCo*. The research focuses on bridging high-level mathematical reasoning with low-level hardware synthesis.

○ Developing multi-level arithmetic transformations from real-valued expressions to fixed-point polynomial approximations for ASIC and FPGA targets.
○ Extending MLIR with custom dialects to support arithmetic abstraction, reasoning, and approximation (RealArith and FixedPointArith).
○ Automating the generation of hardware architectures directly from DSP-oriented code (e.g., Faust), enabling end-to-end lowering from mathematical expressions to silicon.
○ Presented results at *DSD 2025*, *EuroLLVM 2025*, and *EuroLLVM 2026*.

2018 – 2024   **Researcher**, *Barcelona Supercomputing Center (BSC) - RoMoL/CAOS/SONAR*, Barcelona

During the completion of my PhD, I also worked as a researcher, publishing peer-reviewed papers and attending international conferences. The conducted research is summarized as follows:

○ Explored co-designed hardware/software acceleration of posit arithmetic for FPGA and ASIC technologies, and Power9 host.
○ Developed Kulisch/Quire accumulators for any floating-point representation.
○ Conducted accuracy and energy budgeting tailored to workload numerical requirements.
○ Designed Systolic Array architecture for HPC workloads with three directions of data flow, infinite number representations, and tailored internal precision.
○ Proposed very slow and small division units targeting the SIMD/Vector paradigm at the architecture level, further improving the parallelism/latency/energy ratio.

2017 - 2018   **Hardware Engineer**, *b⟨⟩com*, Rennes

Coop student under a professionalization contract during my final year of study. Engaged in one year of R&D focused on FPGA acceleration in the cloud, aiming to evaluate the feasibility of these novel solutions.

○ Successfully integrated an IP (real-time SDR to HDR) to convert video from NVMe to NVMe through cloud FPGA.
○ Developed the IP integration using HDLs and tweaked PCI-e drivers (EDMA and XDMA).
○ Scheduled user processes asynchronously with OpenCL to overlap reads and writes, successfully saturating PCIe bandwidth ($\approx$15.8 GB/s).
○ Traveled to Xilinx XDF Frankfurt 2018 to conduct operational monitoring and analysis.

Keywords: SDAccel, OpenCL, Xilinx FPGA (Ultrascale VU9P), VHDL, SystemVerilog, AWS F1 instances, Linux driver, Linux kernel, PCIe, C++1x, C, DMA, AaaS (Acceleration as a Service), FaaS (FPGA as a Service), Virtual Machine, Docker, PCI-e virtual functions.

July 2017	**Back End Developer**, *WaryMe*, Rennes

Summer internship focused on developing the entire back end of a people security application.
○ Designed and implemented backend services and APIs.
○ Ensured secure data transmission using HTTPS and Let's Encrypt.
○ Deployed and managed the application on AWS with PM2 and Nginx.
○ Automated deployment processes with Jenkins.
○ Collaborated with front-end developers using Angular and TypeScript.
Keywords: Node.js, Git, C++, C, Angular, TypeScript, HTTPS, Let's Encrypt, PM2, Nginx, AWS, Jenkins.

July 2016 **Back End Developer**, *ASKIA*, Paris 10ème
During this summer internship, I developed an automated CLI tool for publishing surveys on popular platforms such as GitHub and Zendesk. **Key Concepts:** Node.js, HTTP(S), REST API, Git, Test-Driven Development (TDD), Event-Driven/Asynchronous Programming, Jasmine Framework, Mocks, Stubs.

July 2014 **Electronics Technician**, *Radio Electronique Rennaise (R.E.R)*, Rennes
As an electronics technician, I was responsible for repairing various electronic devices from customers, with an emphasis on audio equipment. Tasks included soldering, reverse engineering amplifier circuits, welcoming customers, and sorting/ordering electronic parts.

Teaching *(Total teaching load: **96h**)*

2026 **Computer Architecture (ARC)**, *INSA Lyon*, Lyon
Practical sessions in computer architecture for the Telecommunications curriculum, covering instruction execution, pipelining, cache memories, performance evaluation, and RISC-V assembly programming.
Level: 1st year of engineering school (Telecommunications track, 3TC) • Teaching load: 24h

2026 **Operating Systems (SYS)**, *INSA Lyon*, Lyon
Core operating system mechanisms, including kernel and system calls, process scheduling, virtual memory, concurrency, and file systems.
Level: 1st year of engineering school / Bachelor equivalent (Computer Science, INSA 3IF) • Teaching load: 16h

2026 **Long-Term Project in Compilation (PLD-COMP)**, *INSA Lyon*, Lyon
Supervision of long-term group projects on compiler design and implementation, covering intermediate representations, program analysis, and backend code generation.
Level: 2nd year of engineering school / Master 1 (Computer Science, INSA 4IF) • Teaching load: 32h

2025 – 2026 **Computer Architecture (AO)**, *INSA Lyon*, Lyon
Problem-solving and practical sessions on processor organization and instruction set architectures, based on the MSP430 microcontroller, including instruction execution, addressing modes, and memory hierarchy.
Level: 1st year of engineering school / Bachelor equivalent (Computer Science, INSA 3IF) • Teaching load: 12h

2025 – 2026 **Digital Design (AC)**, *INSA Lyon*, Lyon
Exercises and guided sessions on digital circuit design, including combinational and sequential logic, finite state machines, and introductory hardware description languages.
Level: 1st year of engineering school / Bachelor equivalent (Computer Science, INSA 3IF) • Teaching load: 12h

Education

2018 – 2024 **PhD Student**, *Universitat Politècnica de Catalunya (UPC)*, Barcelona
Supervisor: Marc Casas Guix. Thesis title: "Floating-Point Arithmetic Paradigms for High-Performance Computing: Software Algorithms and Hardware Designs". Jury members attributed the **excellent** grade.

2015 – 2018 **Engineering School**, *ESIR*, Université de Rennes
Completed a three-year program culminating in an **Engineer diploma** certified by the CTI (Comité des Titres d'Ingénieurs) and a **Master's degree** (Magister) in Computer Science.

2013 – 2015 **Classe Préparatoire**, *CUPGE ESIR*, Université de Rennes
Intensive program with a strong emphasis on Mathematics and Computer Sciences.

International Peer-reviewed Journals

[Bar+26] B. Barbe, **L. Ledoux**, A. Volkova, and F. de Dinechin, "Reconfigurable constant multipliers: hardware models, optimization algorithm and applications," *Microprocessors and Microsystems*, under review.

[Pop+25] M. Popoff, R. Michon, T. Risset, P. Cochard, **L. Ledoux**, et al., "Frugality and circuit design for digital audio signal processing," *Revue Francophone d'Informatique et Musique*, special issue "Frugalité, pérennité et création," vol. 11, 2025. DOI:10.56698/rfim.961 • HAL:05489376.

[Led+25b] **L. Ledoux**, P. Cochard, and F. de Dinechin, "Towards optimized arithmetic circuits with MLIR," *WiPiEC Journal* (Works in Progress in Embedded Computing), vol. 11, no. 1, 2025, Salerno, Italy. Associated conference presentation at the Euromicro Conference on Digital System Design (DSD). DOI:10.64552/wipiec.v11i1.90 • HAL:04277512.

International Peer-reviewed Conference Papers

[Led25] **L. Ledoux**, "Design-space exploration of serialized floating-point division for DLP architectures," in *28th Euromicro Conference Series on Digital System Design (DSD 2025)*, Salerno, Italy.

[LC23a] **L. Ledoux** and M. Casas, "An open-source framework for efficient numerically-tailored computations," in *33rd International Conference on Field-Programmable Logic and Applications (FPL 2023)*, Gothenburg, Sweden. DOI:10.1109/FPL60245.2023.00011 ● arXiv:2406.02579 ● HAL:04277512.

[LC22] **L. Ledoux** and M. Casas, "A generator of numerically-tailored and high-throughput accelerators for batched GEMMs," in *30th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2022)*, May 2022, pp. 1–10, New York, USA. DOI:10.1109/FCCM53951.2022.9786164 ● HAL:04103774.

Contributions to Publications

[Ven24] Significant contributor (not a listed author) to: M. Venn, "Tiny Tapeout: a shared silicon tapeout platform accessible to everyone," *IEEE Solid-State Circuits Magazine*, 2024. Initiated manuscript drafting, ensured academic formatting, and contributed to revision. URL: ieeexplore.ieee.org/document/10584359 ● Evidence: github.com/mattvenn/tt-ieee-paper.

Poster Presentations

[Led+26b] **L. Ledoux**, P. Cochard, and F. de Dinechin, "Floating-point datapaths in CIRCT via FloPoCo AST export and flopoco-arith-to-comb lowering," in *EuroLLVM Developers' Meeting 2026*, Dublin, Ireland.

[Led+26a] **L. Ledoux**, P. Cochard, and F. de Dinechin, "Arithmetic lowering with Emeraude-MLIR: bridging tensor and DSP kernels to silicon datapaths," Aussois, France. HAL:05489427.

[Led+25a] **L. Ledoux**, P. Cochard, L. Forget, and F. de Dinechin, "Towards multi-level arithmetic optimizations," in *EuroLLVM 2025*, Berlin, Germany. HAL:05063466.

[LC24b] **L. Ledoux** and M. Casas, "LLMMMM: large language models matrix–matrix multiplications characterization on open silicon," in *11th BSC Severo Ochoa Doctoral Symposium 2024*, Barcelona, Spain. HAL:04592229.

[LC24a] **L. Ledoux** and M. Casas, "The grafted superset approach: bridging Python to silicon with asynchronous compilation and beyond," in *4th Workshop on Open-Source Design Automation (OSDA 2024)*, hosted at *DATE*, Valencia, Spain. HAL:04587458.

[LC23b] **L. Ledoux** and M. Casas, "Open-source GEMM hardware kernels generator: toward numerically-tailored computations," in *10th BSC Severo Ochoa Doctoral Symposium 2023*, Barcelona, Spain. arXiv:2305.18328 ● HAL:04094835.

Invited Talks & Seminars

[LC25] **L. Ledoux** and P. Cochard, "FloPoCo and MLIR: a multi-level compilation framework for many intents," Holigrail Seminar, Sorbonne University, Paris, France, September 18, 2025.

[Led24] **L. Ledoux**, "The walls and the dark silicon era: an arithmetic perspective," seminar at Inria Rennes (Team TARAN), Rennes, France, December 2, 2024.

[LC19] **L. Ledoux** and M. Casas, "Accelerating DL inference with (Open)CAPI and posit numbers," in *Open-POWER Summit Europe 2019*, Lyon, France. HAL:04094850.

Conference Organization Experience

LAC25 **Linux Audio Conference**, Lyon, France (2025). *Technician.* Responsible for sound, YouTube streaming, and microphone management. https://jimlac25.inria.fr/lac/

JIM25 **Journées de l'Informatique Musicale**, Lyon, France (2025). *Technician.* Responsible for sound, YouTube streaming, and microphone management. https://jimlac25.inria.fr/jim/

HC32 **HotChips 32nd**, Remote (Digital), SARS-CoV-2 Period (2020). *Remote Assistant.* Assisted with digital entrance management, conference link distribution, and attendee support during the event. https://hc32.hotchips.org/

FPL29 **Field-Programmable Logic Conference 29th**, Barcelona, Spain (2019). *Reception and Entrance Coordinator.* Managed reception desk activities, including badge distribution and providing microphones for speakers during presentations. https://fpl2019.bsc.es/

Academic Summer Schools and Workshops

ACM21 **ACM Europe Summer School on High Performance Computing**, Barcelona, Spain (2021). *Participant.* Attended lectures and hands-on sessions covering exascale architectures, programming models, and numerical numerical methods. https://europe.acm.org/summer-school

YP19 **Yale Patt's Computer Architecture Summer School**, Barcelona, Spain (2019). *Participant.* Attended the special summer edition of Prof. Yale Patt's course on out-of-order execution and advanced microarchitectural design.

XIL19 **Xilinx Machine Learning and Artificial Intelligence Seminar**, Paris, France (2019). *Participant.* Technical seminar focused on machine learning workloads and AI acceleration platforms.

PRACE19 **PRACE Summer School on Heterogeneous Programming with OmpSs@FPGA**, Barcelona, Spain (2019). *Participant.* Training on FPGA-based acceleration and heterogeneous programming using the OmpSs@FPGA model.

Hardware & Software Realizations

Tapeouts
TinyTapeout GF0P2 (Faust→MLIR, tanh saturation), TinyTapeout Sky130 (modified placement flow), and MPW5 Sky130 (Posit/Quire systolic array). MPW1 and MPW4 contributions.

Toolchains
OSFNTC (numerically-tailored GEMM generator with PyTorch/OpenBLAS/OpenCAPI integration), SUF (Python→ASIC design-space exploration), VH2V (VHDL→Verilog for OpenLane/OpenROAD), POF (SystemVerilog Posit operators), gdsiistl (GDSII→STL).

Open-Source Contributions
CIRCT/LLVM (arith dialect + HDL lowering), oc-accel and capi2-bsp (OpenCAPI/CAPI2 support), OpenROAD global placer experiments/visualization, FloPoCo (Virtex UltraScale+ timing model).

Languages

French   Native

Spanish   Native (with an honest French accent)

English   Full Proficiency