

# Louis Ledoux

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🌐 bynaryman.github.io

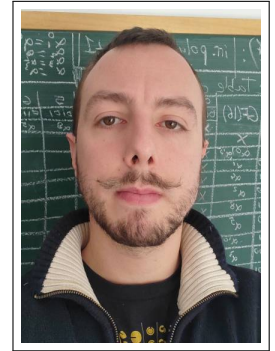
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*“Post Hoc Ergo Propter Hoc”*

## Research Interests

- **Computer Architecture:** Floating-Point Units, Systolic Arrays, Matrix-Matrix Multiply (MMM) Units, GPUs, FPGAs, ASIC Design
- **Computer Arithmetic:** Number Representations, FloPoCo, Posit & IEEE 754 Standards, Fixed-Point Polynomial Approximations, Accuracy–Energy Tradeoffs
- **High Performance Computing:** BLAS, GEMMs, Heterogeneous Workloads, Numerical Analysis, Supercomputing
- **End-to-End Design Philosophy:** From mathematical problem to silicon implementation, integrating MLIR-based compilation and open-source silicon flows for transparent and reproducible design

## Experience

2025 – Now **Postdoctoral Researcher**, INSA/INRIA – *Emeraude*, Lyon

Working on arithmetic compilation and optimization through the integration of *MLIR* and *FloPoCo*. The research focuses on bridging high-level mathematical reasoning with low-level hardware synthesis.

- Developing multi-level arithmetic transformations from real-valued expressions to fixed-point polynomial approximations for ASIC and FPGA targets.
- Extending MLIR with custom dialects to support arithmetic abstraction, reasoning, and approximation (RealArith and FixedPointArith).
- Automating the generation of hardware architectures directly from DSP-oriented code (e.g., Faust), enabling end-to-end lowering from mathematical expressions to silicon.
- Presented results at *DSD 2025* and *EuroLLVM 2025*.

2018 – 2024 **Researcher**, *Barcelona Supercomputing Center (BSC) - RoMoL/CAOS/SONAR*, Barcelona

During the completion of my PhD, I also worked as a researcher, publishing peer-reviewed papers and attending international conferences. The conducted research is summarized as follows:

- Explored co-designed hardware/software acceleration of posit arithmetic for FPGA and ASIC technologies, and Power9 host.
- Developed Kulisch/Quire accumulators for any floating-point representation.
- Conducted accuracy and energy budgeting tailored to workload numerical requirements.
- Designed Systolic Array architecture for HPC workloads with three directions of data flow, infinite number representations, and tailored internal precision.
- Proposed very slow and small division units targeting the SIMD/Vector paradigm at the architecture level, further improving the parallelism/latency/energy ratio.

2017 - 2018 **Hardware Engineer**, *b⟨⟩com*, Rennes

Coop student under a professionalization contract during my final year of study. Engaged in one year of R&D focused on FPGA acceleration in the cloud, aiming to evaluate the feasibility of these novel solutions.

- Successfully integrated an IP (real-time SDR to HDR) to convert video from NVMe to NVMe through cloud FPGA.
- Developed the IP integration using HDLs and tweaked PCI-e drivers (EDMA and XDMA).
- Scheduled user processes asynchronously with OpenCL to overlap reads and writes, successfully saturating PCIe bandwidth ( $\approx 15.8$  GB/s).
- Traveled to Xilinx XDF Frankfurt 2018 to conduct operational monitoring and analysis.

**Keywords:** SDAccel, OpenCL, Xilinx FPGA (Ultrascale VU9P), VHDL, SystemVerilog, AWS F1 instances, Linux driver, Linux kernel, PCIe, C++1x, C, DMA, AaaS (Acceleration as a Service), FaaS (FPGA as a Service), Virtual Machine, Docker, PCI-e virtual functions.

- July 2017 **Back End Developer**, WaryMe, Rennes  
 Summer internship focused on developing the entire back end of a people security application.  
 ○ Designed and implemented backend services and APIs.  
 ○ Ensured secure data transmission using HTTPS and Let's Encrypt.  
 ○ Deployed and managed the application on AWS with PM2 and Nginx.  
 ○ Automated deployment processes with Jenkins.  
 ○ Collaborated with front-end developers using Angular and TypeScript.  
**Keywords:** Node.js, Git, C++, C, Angular, TypeScript, HTTPS, Let's Encrypt, PM2, Nginx, AWS, Jenkins.
- July 2016 **Back End Developer**, ASKIA, Paris 10ème  
 During this summer internship, I developed an automated CLI tool for publishing surveys on popular platforms such as GitHub and Zendesk. **Key Concepts:** Node.js, HTTP(S), REST API, Git, Test-Driven Development (TDD), Event-Driven/Asynchronous Programming, Jasmine Framework, Mocks, Stubs.
- July 2014 **Electronics Technician**, Radio Electronique Rennaise (R.E.R), Rennes  
 As an electronics technician, I was responsible for repairing various electronic devices from customers, with an emphasis on audio equipment. Tasks included soldering, reverse engineering amplifier circuits, welcoming customers, and sorting/ordering electronic parts.

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## Teaching

- 2025 – 2026 **Computer Architecture – Architectures des ordinateurs (AO)**, INSA Lyon, Lyon  
 Lectures and tutorials on processor organization, instruction sets, and memory hierarchy.
- 2025 – 2026 **Digital Design – Architecture des circuits numériques (AC)**, INSA Lyon, Lyon  
 Teaching fundamentals of digital circuits, logic synthesis, and hardware description languages.

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## Education

- 2018 – 2024 **PhD Student**, Universitat Politècnica de Catalunya (UPC), Barcelona  
 Supervisor: Marc Casas Guix. Thesis title: “Floating-Point Arithmetic Paradigms for High-Performance Computing: Software Algorithms and Hardware Designs”. Jury members attributed the **excellent** grade.
- 2015 – 2018 **Engineering School**, ESIR, Université de Rennes  
 Completed a three-year program culminating in an **Engineer diploma** certified by the CTI (Comité des Titres d'Ingénieurs) and a **Master's degree** (Magister) in Computer Science.
- 2013 – 2015 **Classe Préparatoire**, CUPGE ESIR, Université de Rennes  
 Intensive program with a strong emphasis on Mathematics and Computer Sciences.

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## Peer-reviewed Conference Papers

- [Led25] **L. Ledoux** “Design-Space Exploration of Serialized Floating-Point Division for DLP Architectures,” in *28th Euromicro Conference Series on Digital System Design (DSD) 2025*, Salerno, Italy.
- [Led+25b] **L. Ledoux**, Pierre Cochard, and Florent de Dinechin, “Towards Optimized Arithmetic Circuits with MLIR,” in *28th Euromicro Conference Series on Digital System Design (DSD) 2025*, Salerno, Italy.
- [LC23a] **L. Ledoux** and M. Casas, “An Open-Source Framework for Efficient Numerically-Tailored Computations,” in *2023 33rd International Conference on Field-Programmable Logic and Applications (FPL)*, Gothenburg, Sweden. doi: 10.1109/FPL60245.2023.00011, arXiv:2406.02579, HAL:04277512
- [LC22] **L. Ledoux** and M. Casas, “A Generator of Numerically-Tailored and High-Throughput Accelerators for Batched GEMMs,” in *2022 IEEE 30th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2022, pp. 1–10, New York, USA. doi: 10.1109/FCCM53951.2022.9786164, HAL:04103774

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## Poster Presentations

- [Led+25a] **L. Ledoux**, Pierre Cochard, Luc Forget, and Florent de Dinechin, “Towards Multi-Level Arithmetic Optimizations,” in *EuroLLVM2025*, Berlin, Germany. HAL:05063466
- [LC24b] **L. Ledoux** and M. Casas, “LLMMMM: Large Language Models Matrix-Matrix Multiplications Characterization on Open Silicon,” in *2024 11th BSC Symposium*, Barcelona, Spain. HAL:04592229
- [LC24a] **L. Ledoux** and M. Casas, “The Grafted Superset Approach: Bridging Python to Silicon with Asynchronous Compilation and Beyond,” in *2024 4th Workshop on Open-Source Design Automation (OSDA)*, hosted at DATE, Valencia, Spain. HAL:04587458
- [LC23b] **L. Ledoux** and M. Casas, “Open-Source GEMM Hardware Kernels Generator: Toward Numerically-Tailored Computations,” in *2023 10th BSC Symposium*, Barcelona, Spain. arXiv:2305.18328, HAL:04094835

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## Invited Talks & Seminars

- [LC25] **L. Ledoux** and P. Cochard, “FloPoCo and MLIR: A Multi-Level compilation framework for many intents.” Holigrail Seminar at *Sorbonne*, Paris, France, September 18, 2025.
- [Led24] **L. Ledoux**, “The Walls and the Dark Silicon Era: An Arithmetic Perspective,” Seminar at *Team TARAN*, *Inria Rennes*, Rennes, France, December 2, 2024.
- [LC19] **L. Ledoux** and M. Casas, “Accelerating DL Inference with (Open)CAPI and Posit Numbers,” in *OpenPOWER Summit 2019*, Lyon, France. *HAL:04094850*










## Volunteer Experience

- LAC25 **Linux Audio Conference**, Lyon, France (2025). *Technician*. Responsible for sound, YouTube streaming, and microphone management. <https://jimlac25.inria.fr/lac/>
- JIM25 **Journées de l’Informatique Musicale**, Lyon, France (2025). *Technician*. Responsible for sound, YouTube streaming, and microphone management. <https://jimlac25.inria.fr/jim/>
- HC32 **HotChips 32nd**, Remote (Digital), SARS-CoV-2 Period (2020). *Remote Assistant*. Assisted with digital entrance management, conference link distribution, and attendee support during the event. <https://hc32.hotchips.org/>
- FPL29 **Field-Programmable Logic Conference 29th**, Barcelona, Spain (2019). *Reception and Entrance Coordinator*. Managed reception desk activities, including badge distribution and providing microphones for speakers during presentations. <https://fpl2019.bsc.es/>

## Academic Summer Schools & Workshops

- ACM21 **ACM Europe Summer School on High Performance Computing**, Barcelona, Spain (2021). *Participant*. Attended lectures and hands-on sessions on exascale architectures, programming models, and numerical methods. <https://europe.acm.org/summer-school>
- YP19 **Yale Patt’s Computer Architecture Class**, Barcelona, Spain (2019). *Participant*. Attended the special summer edition of Prof. Yale Patt’s class on out-of-order execution and microarchitectural design.

## Projects & Hobbies

- MPW 5 Taped out a Systolic Array for Matrix Multiplication with *Posit* numbers and *Quires* accumulators . I have been interviewed on YouTube .
- Artistic OpenROAD Modified the *replace* tool in the OpenROAD ASIC flow (GitHub ) to visualize electrostatic fields and explore chip sonification as an artistic interpretation of circuit behavior. The project aims to “see” and “hear” chip births, merging aesthetics with silicon design. Taught these concepts in Matt Venn’s Zero to ASIC course (*presentation link*).
- MPW 1 & 4 My first taped-out chip on the first-ever open shared Multi-Project Wafer in collaboration with Google, SkyWater, and Efabless. The design was later re-taped in MPW 4 due to a foundry-wide hold violation affecting all submissions. Open contribution to the Open Source Silicon community available on GitHub . Related official projects: MPW-1 and MPW-4.
- SUF Developed a Python-to-ASIC compiler with a focus on arithmetic. Includes novel (and artistic) placement visualization , among other features such as plot-automation, PDK-agnosticism, asynchronous and parallel execution of several designs, etc.
- OSFNTC Developed an Open-Source Framework for Efficient Numerically-Tailored Computation. Modified PyTorch, Numpy, OpenBLAS, OpenCAPI to work with PCI-e/NVLink FPGAs with arbitrarily large Systolic Arrays and infinite float format representations with any intermediate precision. Systematically improved energy efficiency and accuracy for drastically different workloads such as Deep Learning and Sea Surface Height calculation. Project on GitHub .
- POF Designed the Posit Operators Framework, a comprehensive SW/HW co-designed library to facilitate arithmetic computations and neural network operations using the *Posit* numerical format on FPGAs. Manually written modules can be found on GitHub .
- VH2V Designed a VHDL-to-Verilog translation tool tailored to convert FloPoCo outputs to OpenLane/OpenROAD inputs. Project available on GitHub .
- Synthesizers Crafted analog and digital synthesizers for modular synthesis and Eurorack systems. Responsibilities included PCB manufacturing , part ordering, and digital design.

## Languages

- French Native
- Spanish Native (with an honest French accent)
- English Full Proficiency