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Louis Ledoux

Curriculum Vitae

"Post Hoc Ergo Propter Hoc"

Research Interests

Computer Architecture: Floating-Point Units, Systolic Arrays, Matrix-Matrix Multiply (MMM) Units, GPUs, FPGAs
Computer Arithmetic: Number Representations, Application-Specific Circuits, FloPoCo, Posit & IEEE754 Standards, Kulisch Accumulator, Accuracy and Energy Budgeting
High Performance Computing: BLAS, Dense & Sparse GEMMs, Heterogeneous Workloads, Numerical Analysis, Supercomputing

Education

2018 — **PhD Student**, *Universitat Politècnica de Catalunya (UPC)*, Barcelona
Supervisor: Marc Casas Guix. Thesis title: "Floating-Point Arithmetic Paradigms for High-Performance Computing: Software Algorithms and Hardware Designs".

2015 – 2018 — **Engineering School**, *ESIR*, Université de Rennes
Completed a three-year program culminating in an **Engineer diploma** certified by the CTI (Comité des Titres d'Ingénieurs) and a **Master's degree** (Magister) in Computer Science.

2013 – 2015 — **Classe Préparatoire**, *CUPGE ESIR*, Université de Rennes
Intensive program with a strong emphasis on Mathematics and Computer Sciences.

Experience

2018 — **Researcher**, *Barcelona Supercomputing Center (BSC) - RoMoL/CAOS/SONAR*, Barcelona
During The completion of my PhD I also worked as a researcher where I publisged peer-reviewed papers, travel to itnernational conferences.

- Conducted research on hardware acceleration and optimization using FPGA and ASIC technologies.
- Developed and implemented numerical algorithms tailored for FPGA-based computation.
- Collaborated with a multidisciplinary team to enhance the performance of large-scale simulations.
- **Keywords:** FPGA, Arithmetic, ASIC

2017 – 2018

Hardware Engineer, *b⟨⟩com*, Rennes

Coop student under a professionalization contract during my final year of study. Engaged in one year of R&D focused on FPGA acceleration in the cloud, aiming to evaluate the feasibility of these novel solutions.

- Successfully integrated an IP (real-time SDR to HDR) to convert video from NVMe to NVMe through cloud FPGA.
- Developed the IP integration using HDLs and tweaked PCI-e drivers (EDMA and XDMA).
- Scheduled user processes asynchronously with OpenCL to overlap reads and writes, successfully saturating PCIe bandwidth (≈15.8 GB/s).
- Traveled to https://www.xilinx.com/video/events/xdf-frankfurt-2018-keynote.htm https://www.xilinx.com/video/events/xdf-frankfurt-2018-keynote.htmll

Keywords: SDAccel, OpenCL, Xilinx FPGA (Ultrascale VU9P), VHDL, SystemVerilog, AWS F1 instances, Linux driver, Linux kernel, PCIe, C++1x, C, DMA, AaaS (Acceleration as a Service), FaaS (FPGA as a Service), Virtual Machine, Docker, PCI-e virtual functions.

July 2017

Back End Developer, *WaryMe*, Rennes

Summer internship focused on developing the entire back end of a people security application.

- Designed and implemented backend services and APIs.
- Ensured secure data transmission using HTTPS and Let's Encrypt.
- Deployed and managed the application on AWS with PM2 and Nginx.
- Automated deployment processes with Jenkins.
- Collaborated with front-end developers using Angular and TypeScript.

Keywords: Node.js, SQLite3, Git, C++, C, Angular, TypeScript, HTTPS, Let's Encrypt, PM2, Nginx, AWS, Jenkins.

July 2016

Back End Developer, *ASKIA*, Paris 10ème

During this summer internship, I developed an automated CLI tool for publishing surveys on popular platforms like GitHub and Zendesk. **Key Concepts:** Node.js, HTTP(S), REST API, Git, Test-Driven Development (TDD), Event/Asynchronous Programming, Jasmine Framework, Mocks, Stubs.

July 2014

Electronics Technician, *Radio Electronique Rennaise (R.E.R)*, Rennes

Summer Internship...

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- **Keywords:**

Peer-reviewed Conference Papers

[LC23a] **L. Ledoux** and M. Casas, "An Open-Source Framework for Efficient Numerically-Tailored Computations," in *2023 33rd International Conference on Field-Programmable Logic and Applications (FPL)*, Sep. 2023, pp. 19–26, Gothenburg, Sweden. *Available: doi: 10.1109/FPL60245.2023.00011, arXiv:2406.02579, HAL:04277512*

[LC22] **L. Ledoux** and M. Casas, "A Generator of Numerically-Tailored and High-Throughput Accelerators for Batched GEMMs," in *2022 IEEE 30th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2022, pp. 1–10, New York, USA. *Available: doi: 10.1109/FCCM53951.2022.9786164, HAL:04103774*

Poster Presentations

[LC24b] **L. Ledoux** and M. Casas, "LLMMMM: Large Language Models Matrix-Matrix Multiplications Characterization on Open Silicon" in *2024 11th BSCSymposium*, May 2024, Barcelona, Spain. *Available: HAL:04592229*

[LC24a] **L. Ledoux** and M. Casas, "The Grafted Superset Approach: Bridging Python to Silicon with Asynchronous Compilation and Beyond" in *2024 4th Workshop on Open-Source Design Automation (OSDA)*, hosted at the International Conference on Design, Automation and Test in Europe Conference (DATE), March 25, 2024, at Palacio De Congresos Valencia (Valencia Conference Centre - VCC), Valencia, Spain. *Available: HAL:04587458*

[LC23b] **L. Ledoux** and M. Casas, "Open-Source GEMM Hardware Kernels Generator: Toward Numerically-Tailored Computations" in *2023 10th BSCSymposium*, May 2023, Barcelona, Spain. *Available: arXiv:2305.18328, HAL:04094835*

Invited Talks

[LC19] **L. Ledoux** and M. Casas, "Accelerating DL inference with (Open)CAPI and posit numbers," in *OpenPOWER Summit 2019*, Lyon, France: Linux Foundation, Oct. 2019. *Available: HAL:04094850*

Miscelaneous

ACM Summerschool	attended
Yale Patt	attended anniversayr + yearly class
Xilinx AI PAris	

Languages

French	Native	
Spanish	Native	*(with an honest french accent)*
English	Full Proficiency	

Skills

Scripting	Python, bash, sh, Linux	Dissemination	LaTeX, Matplotlib, Inkscape
FPGA	AMD, ALtera, VHDL, Verilog, SystemVerilog, FloPoCo, SDAccel, AWS f1, PCI-e	GPU	CUDA 8,9, OpenCL
Programming	C, C++, Java, Scala	Versioning	git, github,gitlab, svn, recurrent pull requests