CA HW3 B05901011 電機四 許秉倫

rtl_tb1

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

============================================

 Congratulations!!! Your answer is correct!
```

rtl_tb2

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

============================================

 Congratulations!!! Your answer is correct!
```

gatelevel_tb1

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

SDF File ./matvecmult_syn.sdf were used for this simulation.
============================================

 Congratulations!!! Your answer is correct!
```

gatelevel_tb2

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

SDF File ./matvecmult_syn.sdf were used for this simulation.
============================================

 Congratulations!!! Your answer is correct!
```

no latch

```
 Inferred memory devices in process
        in routine matvecmult line 89 in file
                '/home/raid7_2/userb05/b05011/CA/hw3/matvecmult.v'.
 ===============================================================================
 |    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
 ===============================================================================
 |    counter_r_reg    | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
 |       y_r_reg       | Flip-flop |  128  |  Y  | N  | Y  | N  | N  | N  | N  |
 ===============================================================================
```

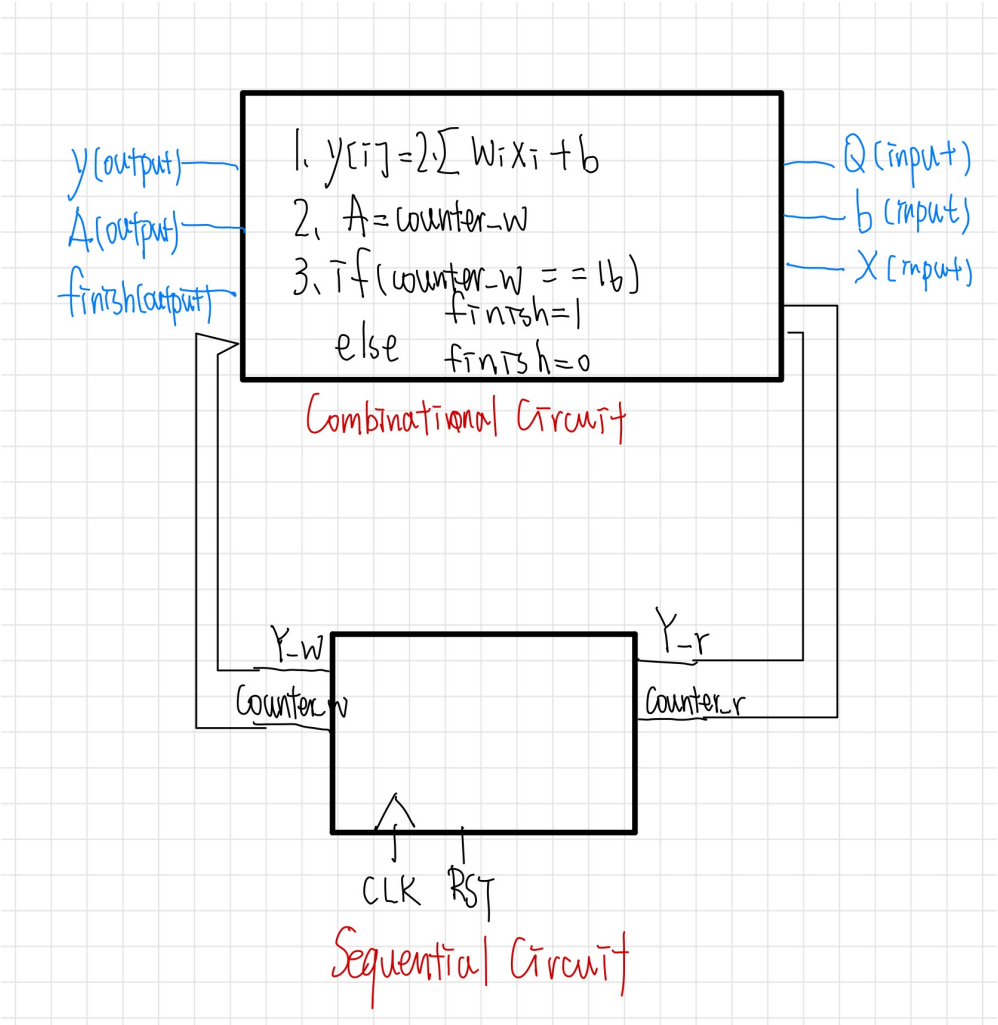
timing report

```
add_0_root_add_1_root_add_48_15/U1_2/CO (ADDFXL)        0.86       5.62 r
add_0_root_add_1_root_add_48_15/U1_3/S (ADDFXL)         0.62       6.24 r
add_0_root_add_1_root_add_48_15/SUM[3] (matvecmult_DW01_add_0)
                                                        0.00       6.24 r
add_0_root_add_48_15/B[3] (matvecmult_DW01_add_15)      0.00       6.24 r
add_0_root_add_48_15/U1_3/CO (ADDFXL)                   0.86       7.10 r
add_0_root_add_48_15/U1_4/S (ADDFXL)                    0.61       7.71 r
add_0_root_add_48_15/SUM[4] (matvecmult_DW01_add_15)
                                                        0.00       7.71 r
add_76/A_5_ (matvecmult_DW01_add_14)                    0.00       7.71 r
add_76/U1_5/CO (ADDFXL)                                 0.80       8.51 r
add_76/U1_6/S (ADDFXL)                                  0.68       9.19 r
add_76/SUM_6_ (matvecmult_DW01_add_14)                  0.00       9.19 r
U208/Y (INVX3)                                          0.45       9.64 f
U272/Y (OAI2BB2XL)                                      0.51      10.15 r
y_r_reg_0__6_/D (DFFRX2)                                0.00      10.15 r
data arrival time                                                 10.15

clock CLK (rise edge)                                  10.00      10.00
clock network delay (ideal)                             0.50      10.50
clock uncertainty                                      -0.10      10.40
y_r_reg_0__6_/CK (DFFRX2)                               0.00      10.40 r
library setup time                                     -0.22      10.18
data required time                                                10.18
--------------------------------------------------------------------------
data required time                                                10.18
data arrival time                                                -10.15
--------------------------------------------------------------------------
slack (MET)                                                       0.03
```

area report

```
Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_I

Number of ports:                         1207
Number of nets:                          2972
Number of cells:                         1651
Number of combinational cells:           1465
Number of sequential cells:               153
Number of macros/black boxes:               0
Number of buf/inv:                        209
Number of references:                      54

Combinational area:              18318.341019
Buf/Inv area:                      841.910387
Noncombinational area:            5037.883209
Macro/Black Box area:                0.000000
Net Interconnect area:          186294.270599

Total cell area:                 23356.224228
Total area:                     209650.494828
1
```

design and difficulty



首先，將電路拆成Sequential和combinational的part。 我設定兩個狀態，分別是Y和counter。
Sequential part: 負責在clock來的時候更新Y及counter。
Combinational part: 當一個cylce來的時候，吃入新的值，並把新的值經過運算得到next state，接著輸出output。
因為是第一次寫verilog所以整個概念還有語法都要從頭摸索，導致花了蠻多時間在這個作業上的，但寫完後覺得很有成就感！