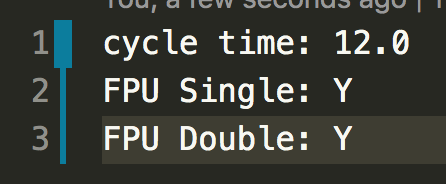
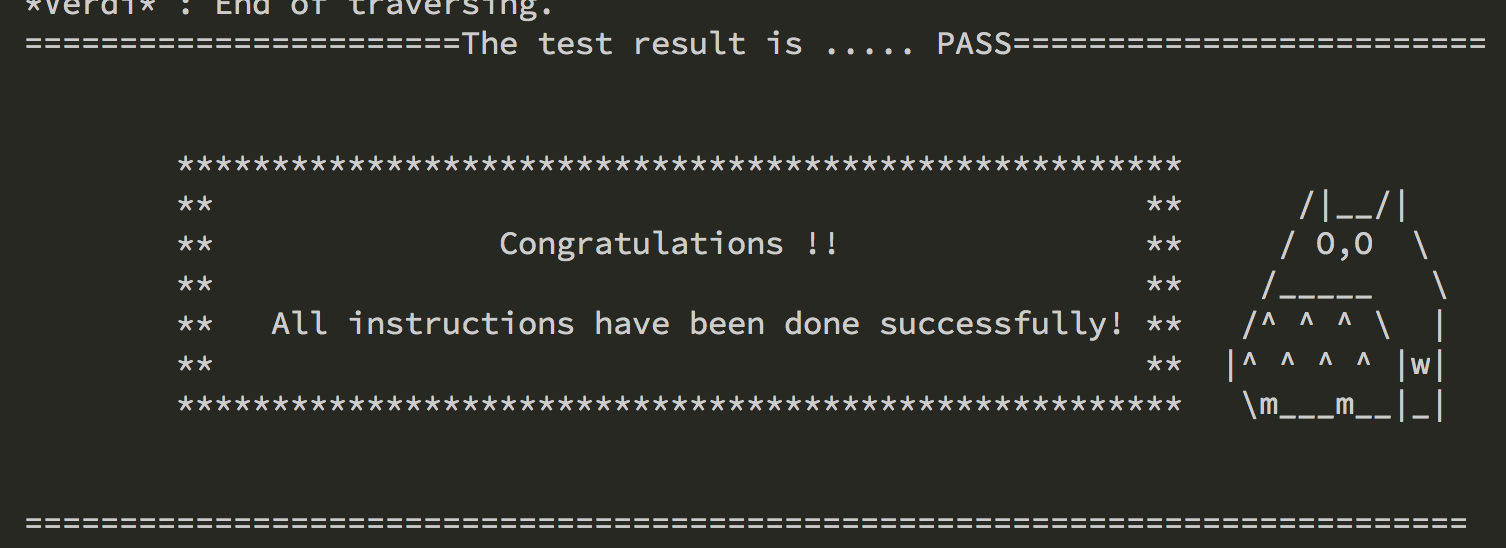
Computer Architecture HW4 report

1. Snapshot
   1. Readme.txt content (see sec. 8)

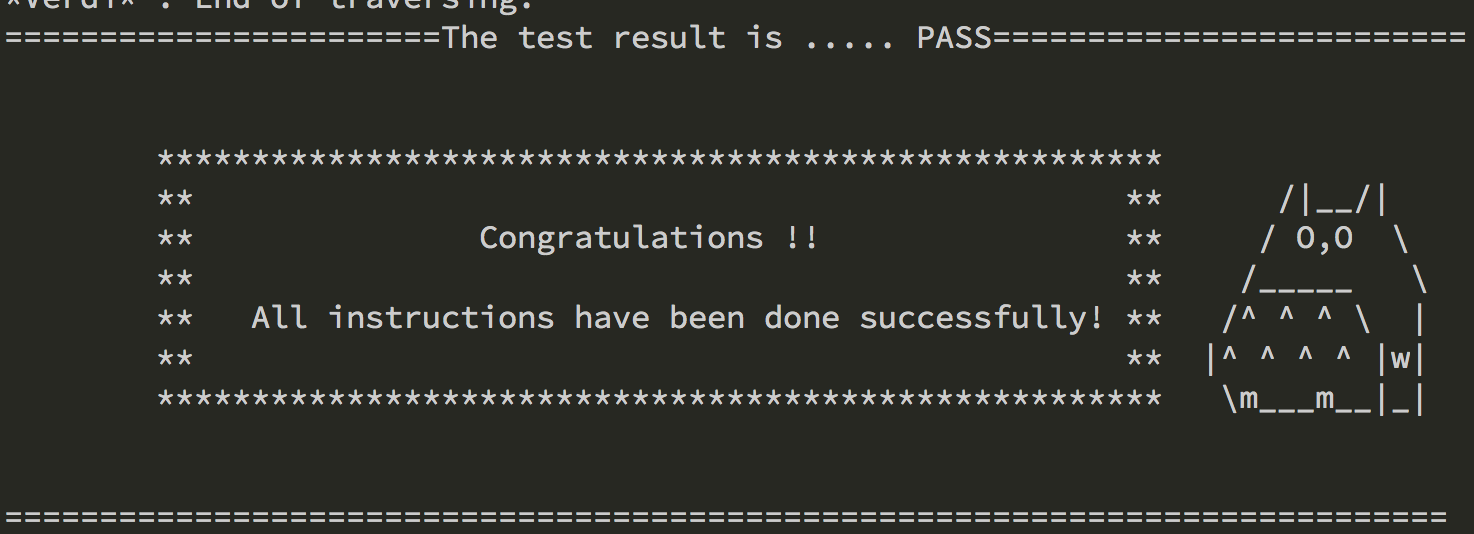


* 1. All RTL Simulation you pass (see Appendix II for example)

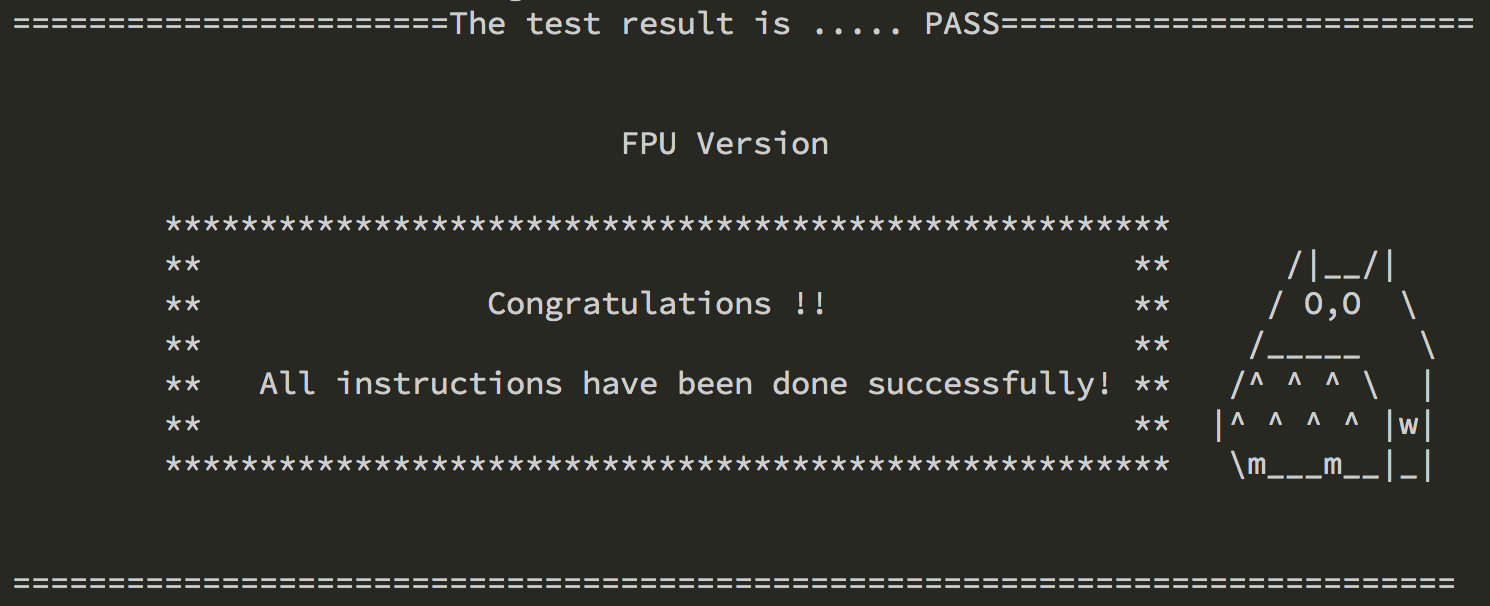
Baseline



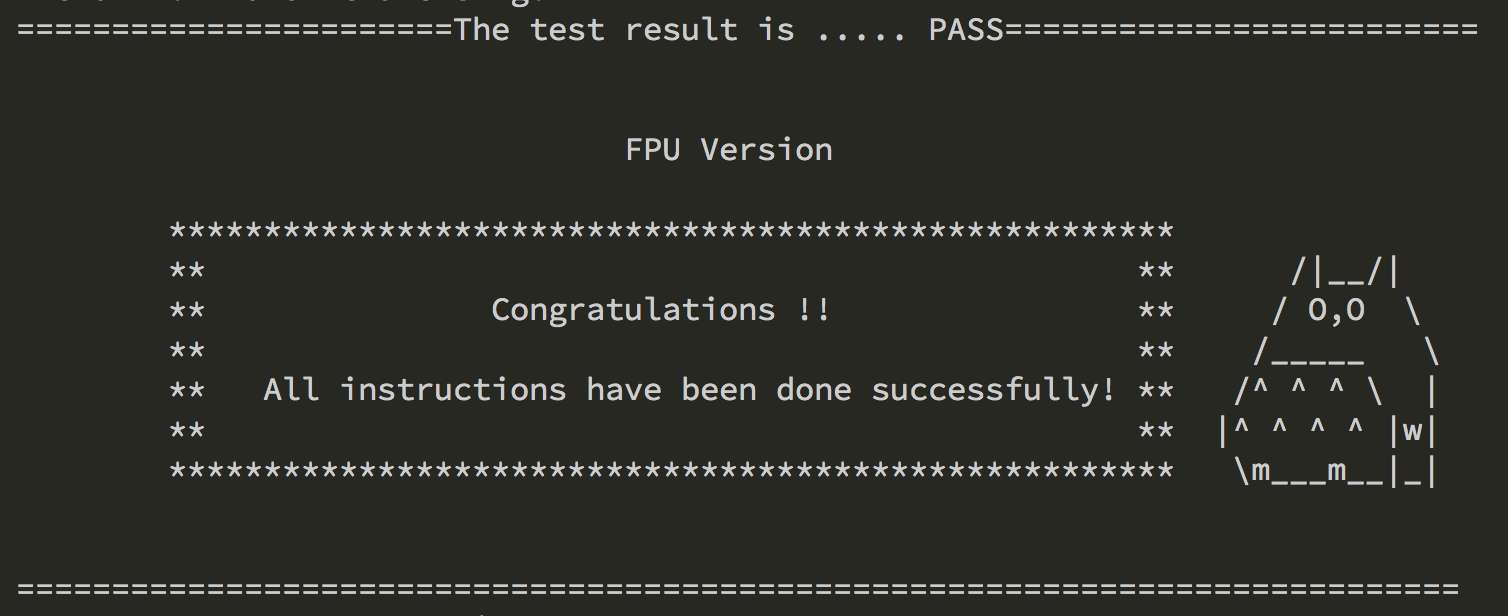
FPU-Baseline



FPU-Single

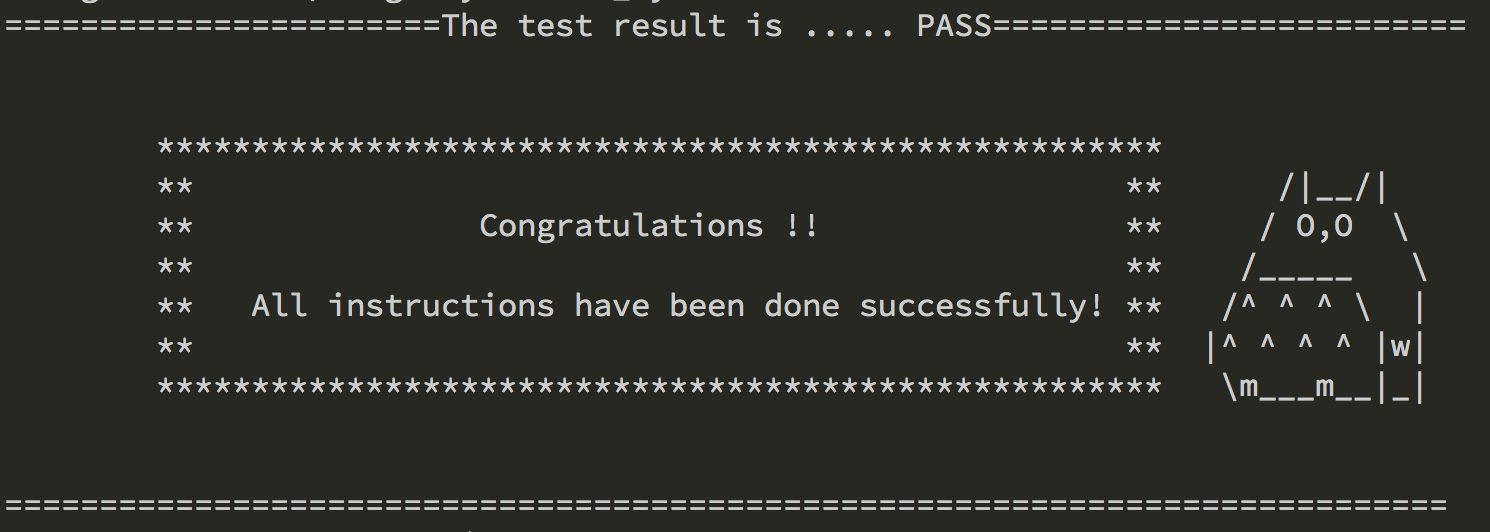


FPU-Double

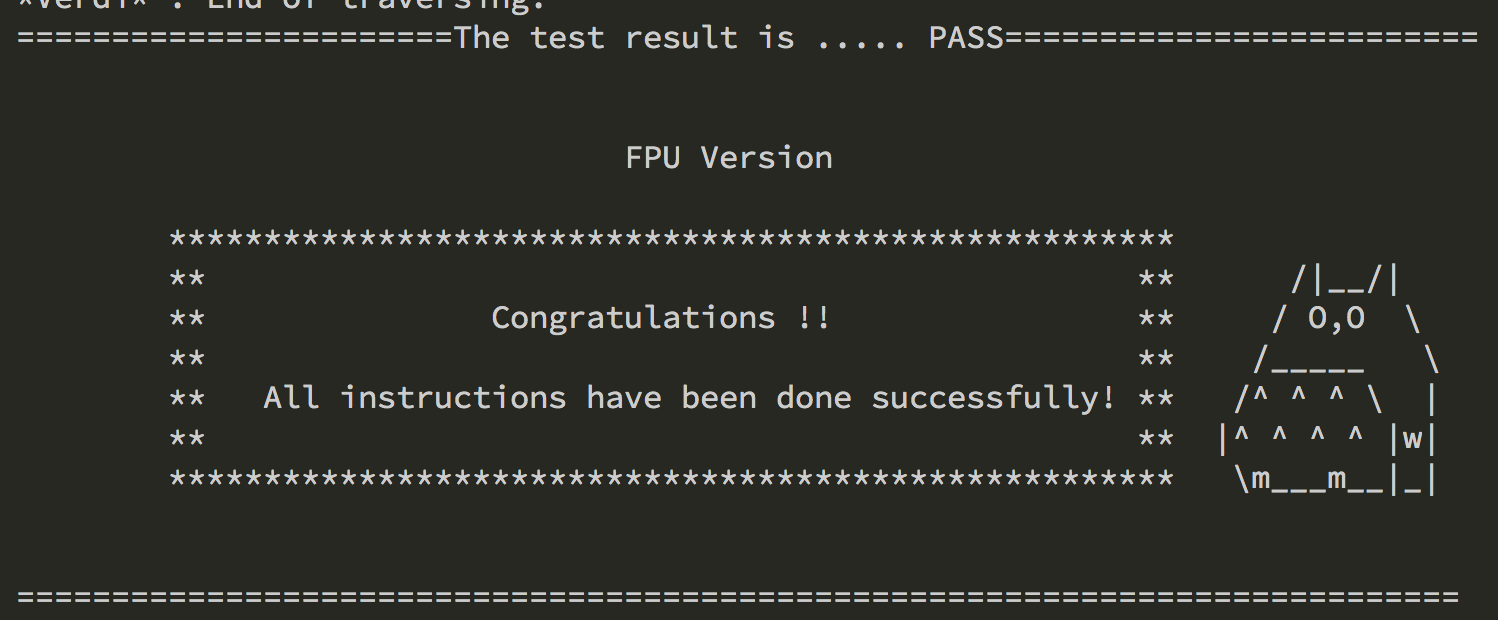


* 1. All Gate-level Simulation you pass

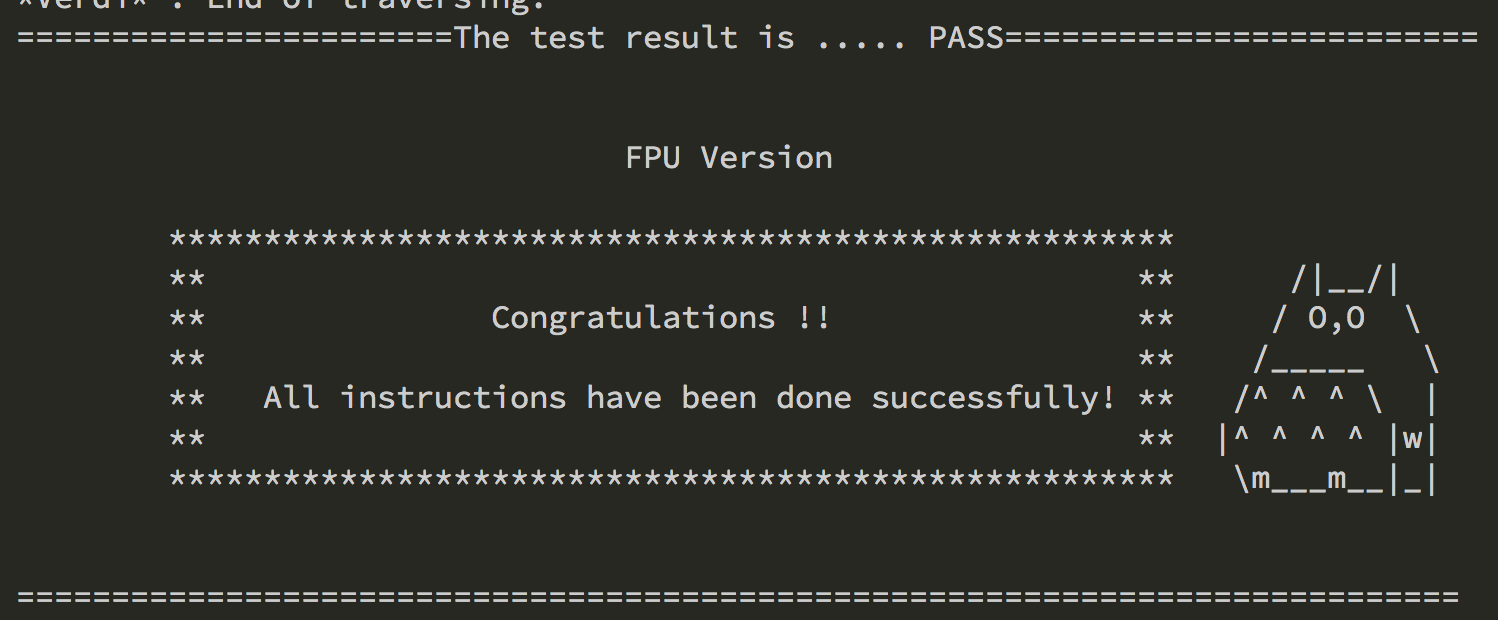
Baseline



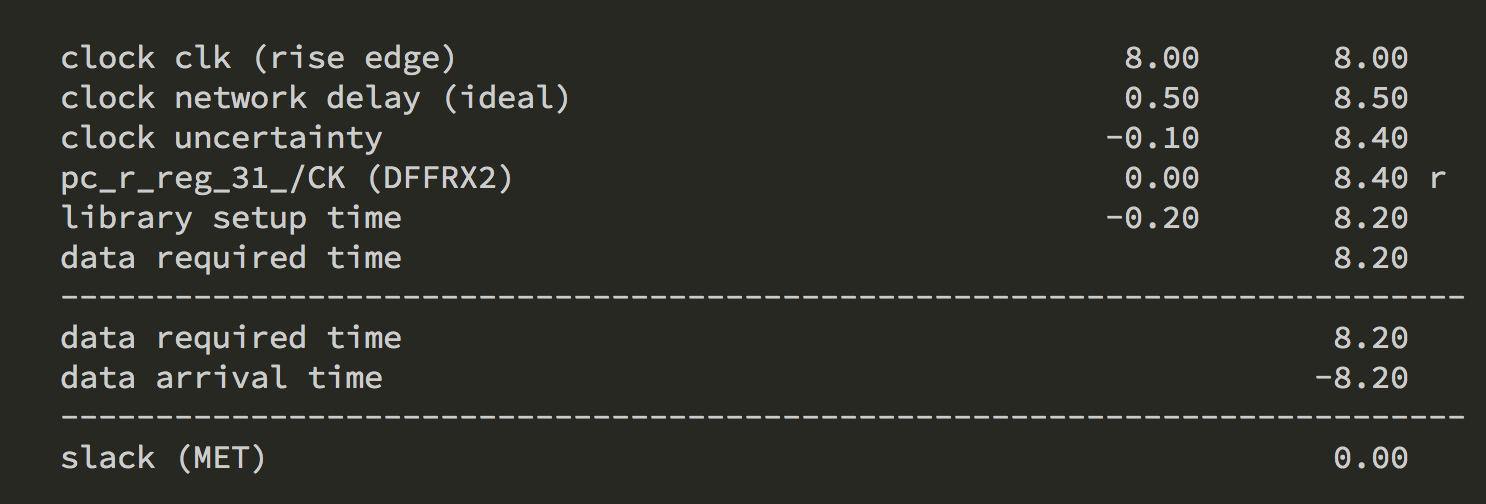
FPU-Single



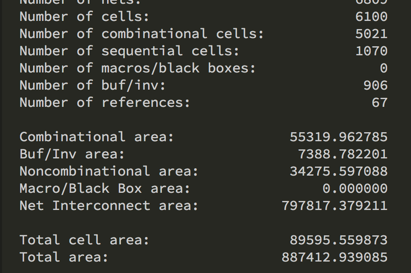
FPU-Double



* 1. Timing report



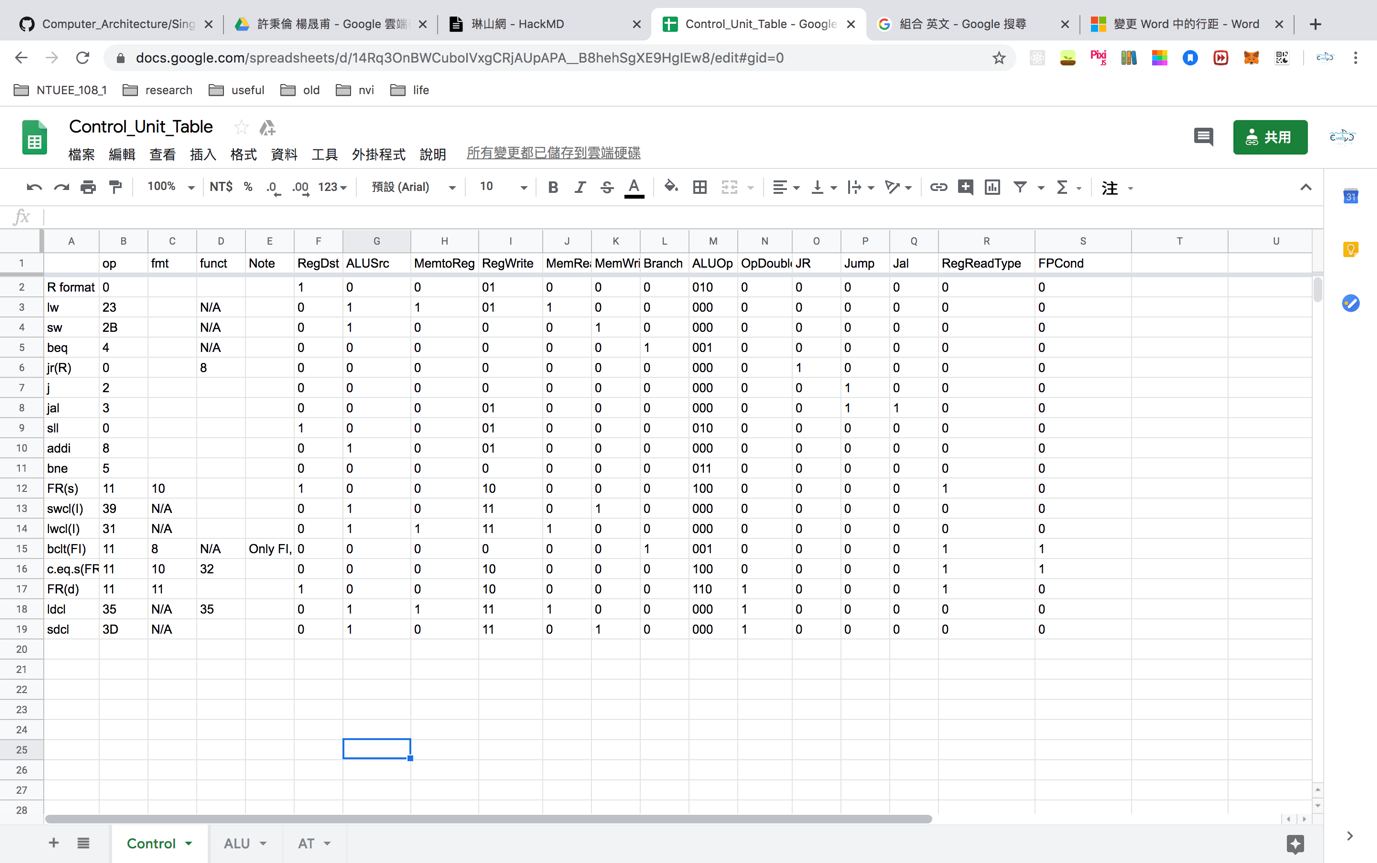
* 1. Area report



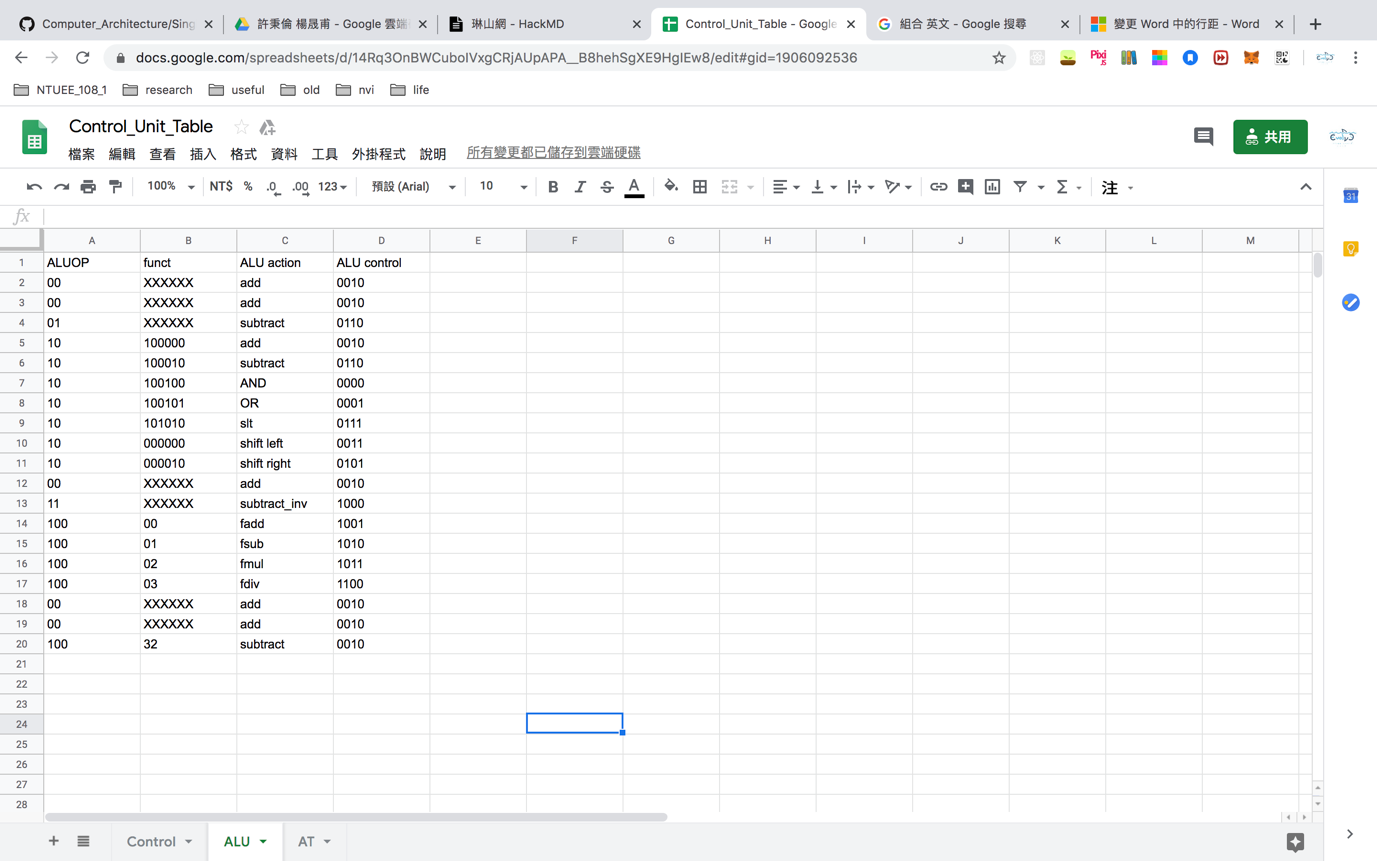
1. Your baseline A\*T value calculated from numbers in the snapshot
2. Please describe how you design this circuit and what difficulties you encountered when working on this exercise.

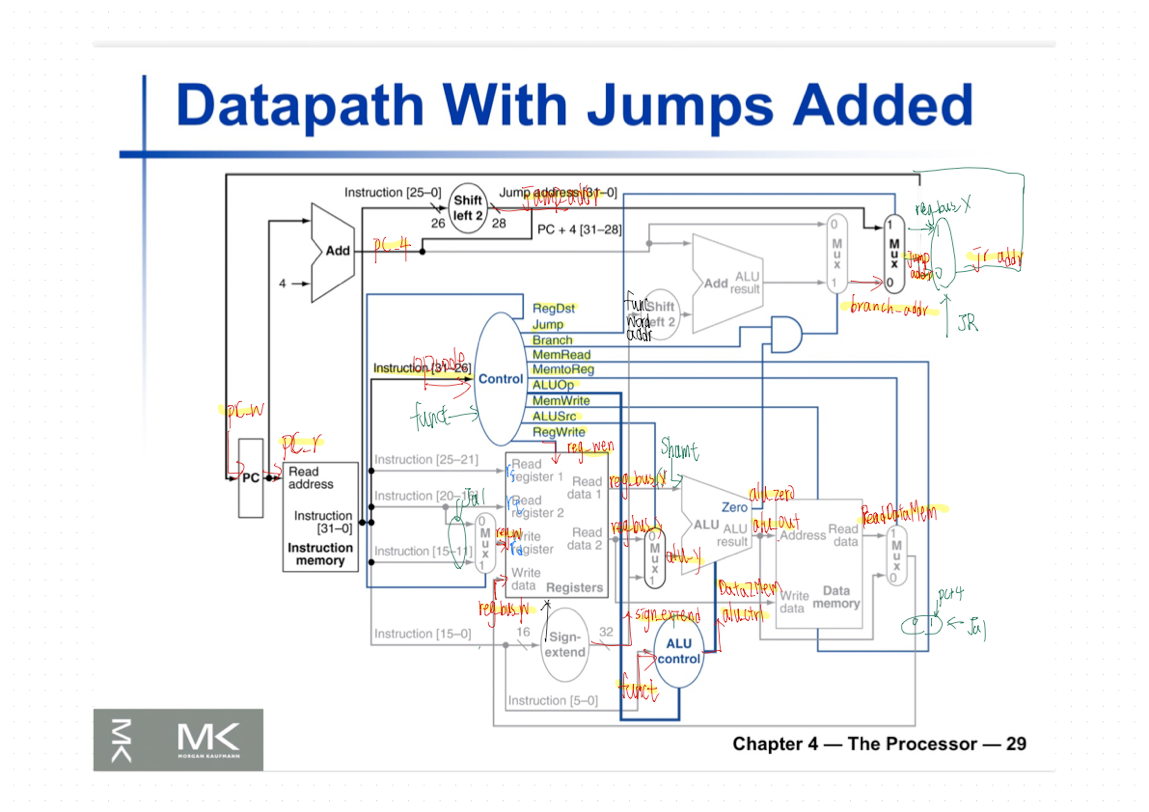
**Design: 我們是照著課本給的電路，把control及alu table擴充，來達成baseline及FPU的功能。**

Control Table:



ALU Control Table:



Baseline: 紅色的字為wrie，綠色的部分是比課本多加的東西  


FPU: TODO

**Difficulties:** 由於我們兩個都對verilog沒有經驗，所以前期花了很多時間上網觀摩別人的code，  
但當大架構出來了之後，就變得比較得心應手

1. Work distribution

許秉倫：Baseline  
楊晟甫：FPU

1. (optional) how you improve your A\*T value

* 將 “control\_table”, “alu\_table”化簡，減少bit用數