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Module name

Peripheral module

Change log

RELEASED

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to the final schematic.

CHECKER - There should be no mistakes. Tell the engineer if you find one.

RELEASER - There should be no mistakes. Tell the engineer if you find

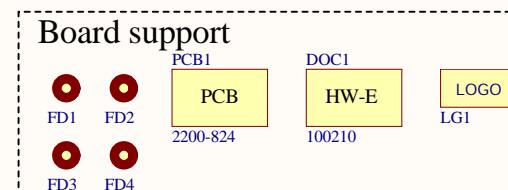
Index	Description
01	COVER
02	CORE
03	PERIPHERAL_I2C
04	PERIPHERAL_SPI
05	INTERFACE
06	FTDI
07	POWER SUPPLY

DESIGN CONSIDERATIONS

SOFTWARE CONFIG NOTE:

- Contains important notes for software development
- Things like: pin configuration, timing requirements, IC configuration etc.

DESIGN NOTE:

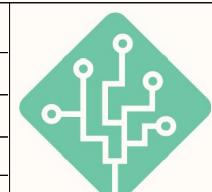


LIST OF AVAILABLE VARIANTS

# VAR	Variant name	Description

REVISION FORMAT EXPLANATION

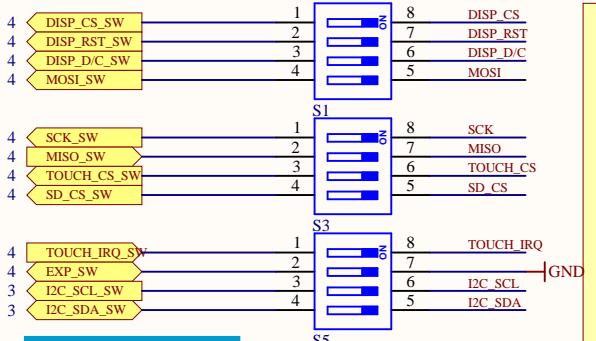
-	-	202y-mm-dd	Development phase, date only	-	
10	-	202y-mm-dd	Prototyping phase, revision numeric	3000-xxx-xxx	
-	A	202y-mm-dd	Production phase, revision alphanumeric	3000-xxx-xxx	



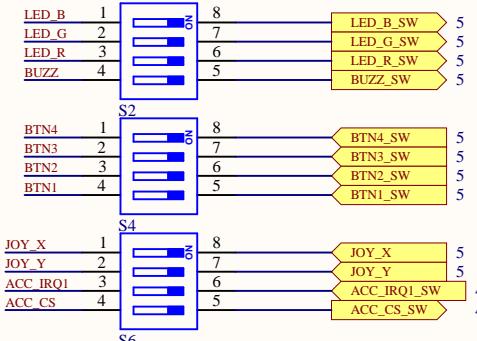
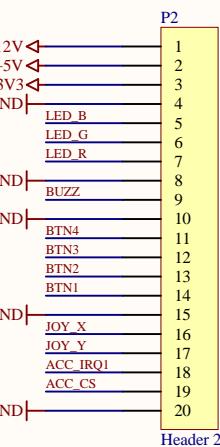
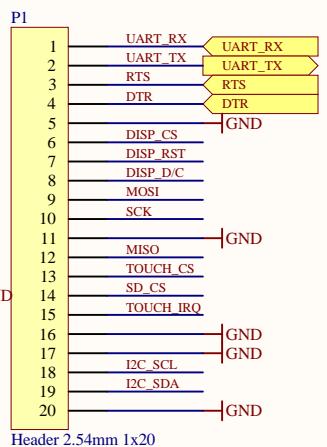
Title: 01_COVER.SchDoc
Project: 100210_BLDK-Peripheral-module.PrjPCB
Company: Byte Lab Grupa d.o.o.
Medarska 69/1, 10000 Zagreb, Croatia www.byte-lab.com
Author: M. Hamin
Acceptor: C. Lusetic
Sheet 1 of 7
Rev: 12
Format: A4

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EXPANSION



SOFTWARE CONFIG NOTE:
EXP_SW is for enabling/disabling expander



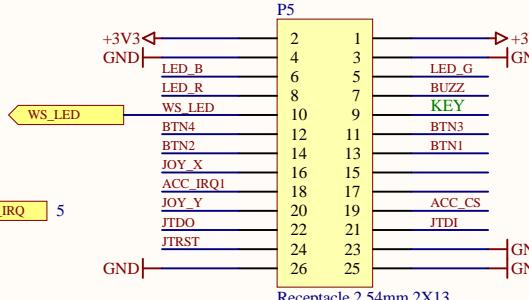
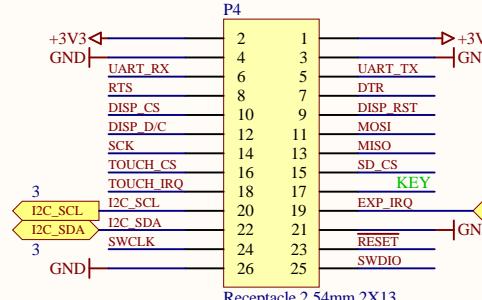
JTAG/SWD

SOFTWARE CONFIG NOTE:
SWD and JTAG pins are shared on MCU

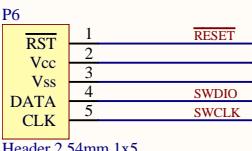


Header 2.54mm 1x8

CORE MODULE CONNECTOR

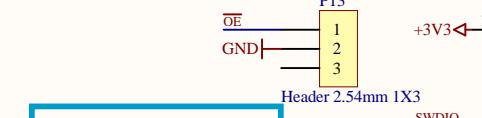


DESIGN NOTE:
- KEY- fill those pins in production as protection for plugging core module in opposite direction



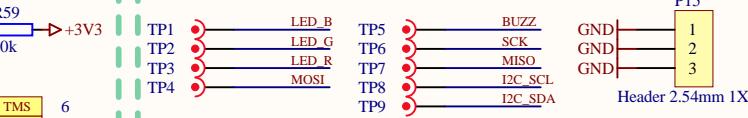
Header 2.54mm 1x5

JTAG CONFIG



SOFTWARE CONFIG NOTE:
Short for internal programmer; left unconnected for ext. JTAG

TESTPOINTS

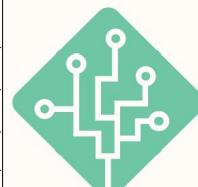


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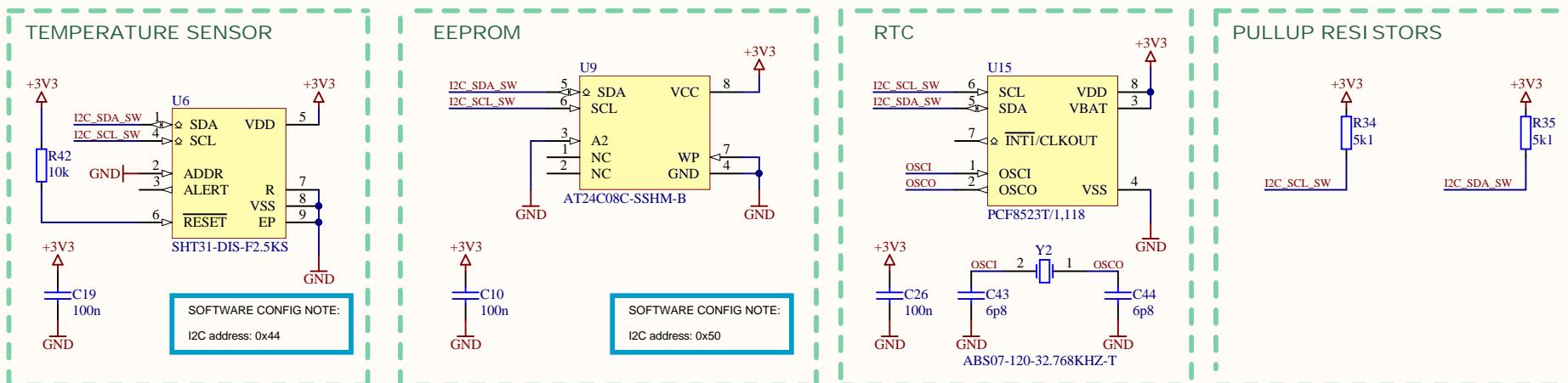
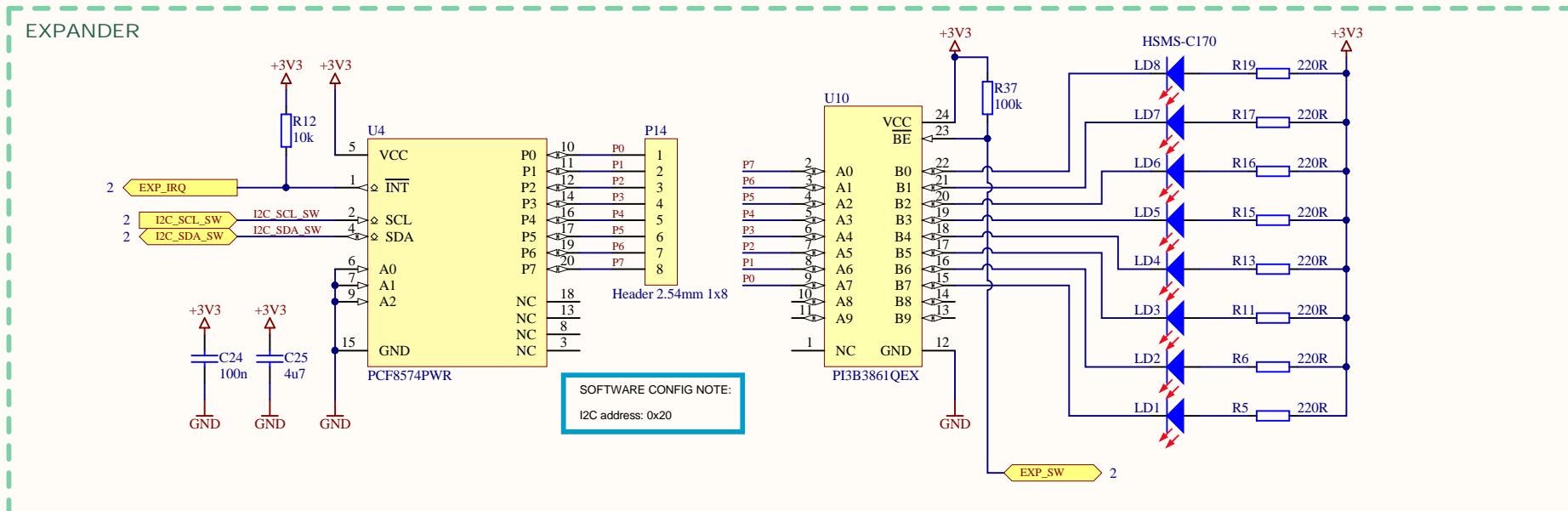
Project:
100210_BLDK-Peripheral-module.PjPCB
Company:
Byte Lab Grupa d.o.o. Medarska 69/1, 10000 Zagreb, Croatia
www.byte-lab.com

Author:
M. Hamin Acceptor:
C. Lusetic

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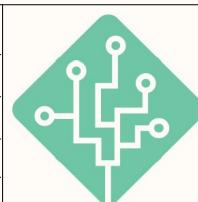
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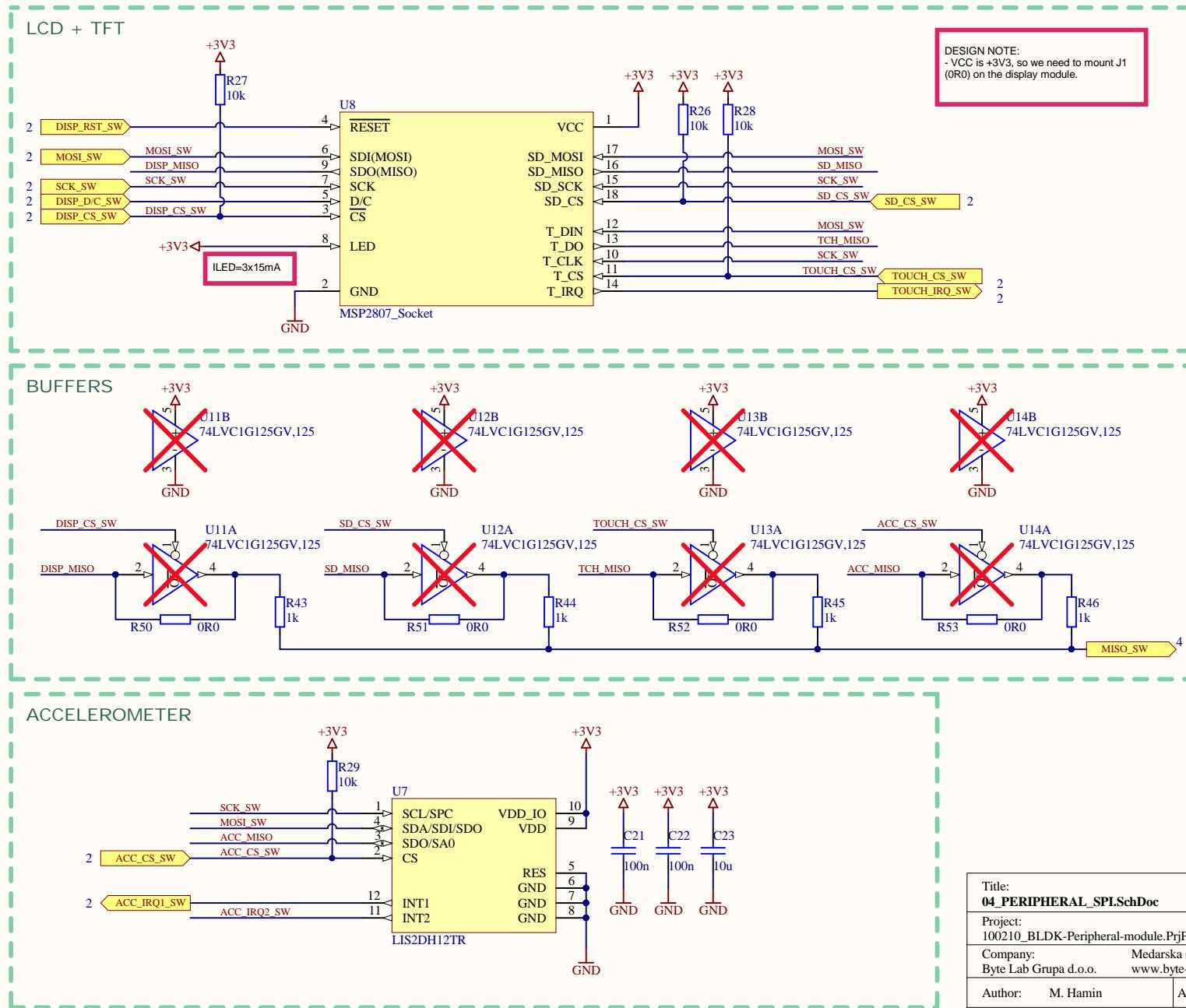
Project:
100210_BLDK-Peripheral-module.PnjPCB

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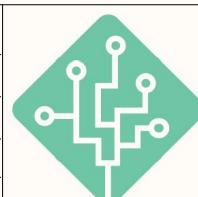
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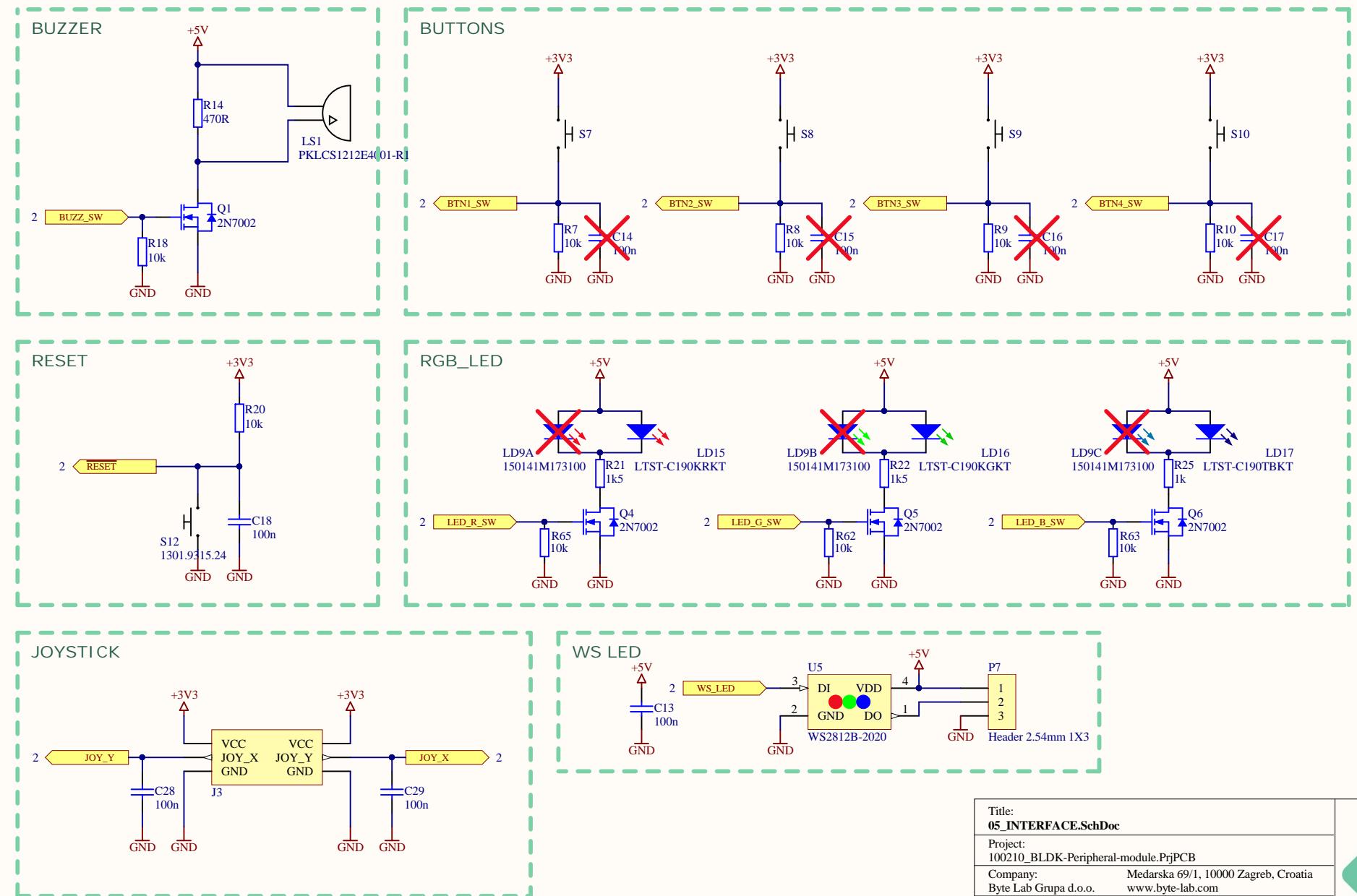
Project:
100210_BLDK-Peripheral-module.PjPCB

Company:
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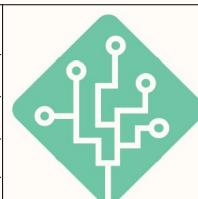


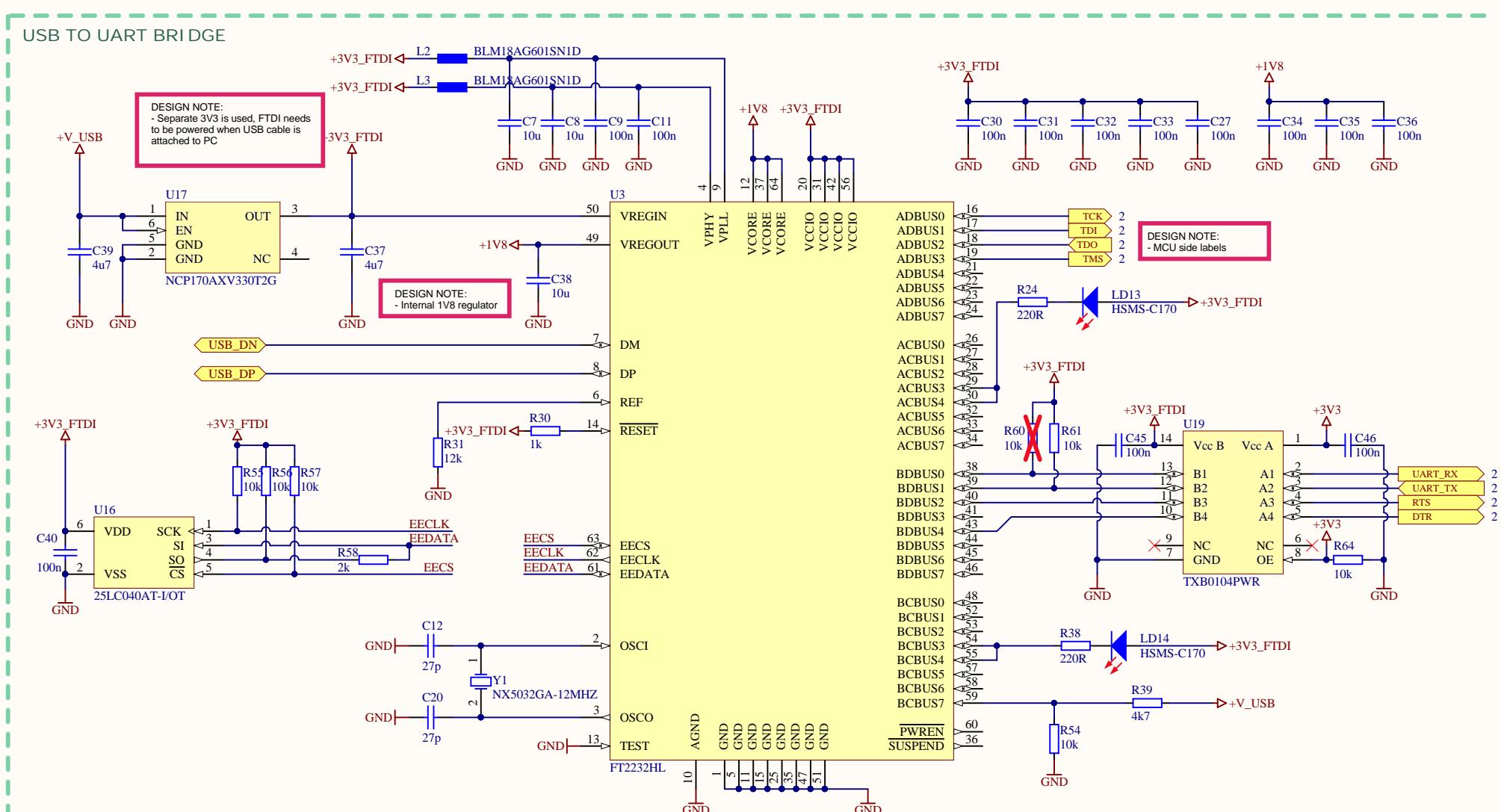
Title:
05_INTERFACE.SchDoc

Project:
100210_BLDK-Peripheral-module.PrdPCB
Company:
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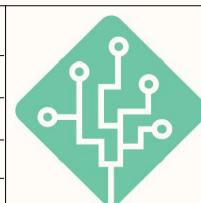
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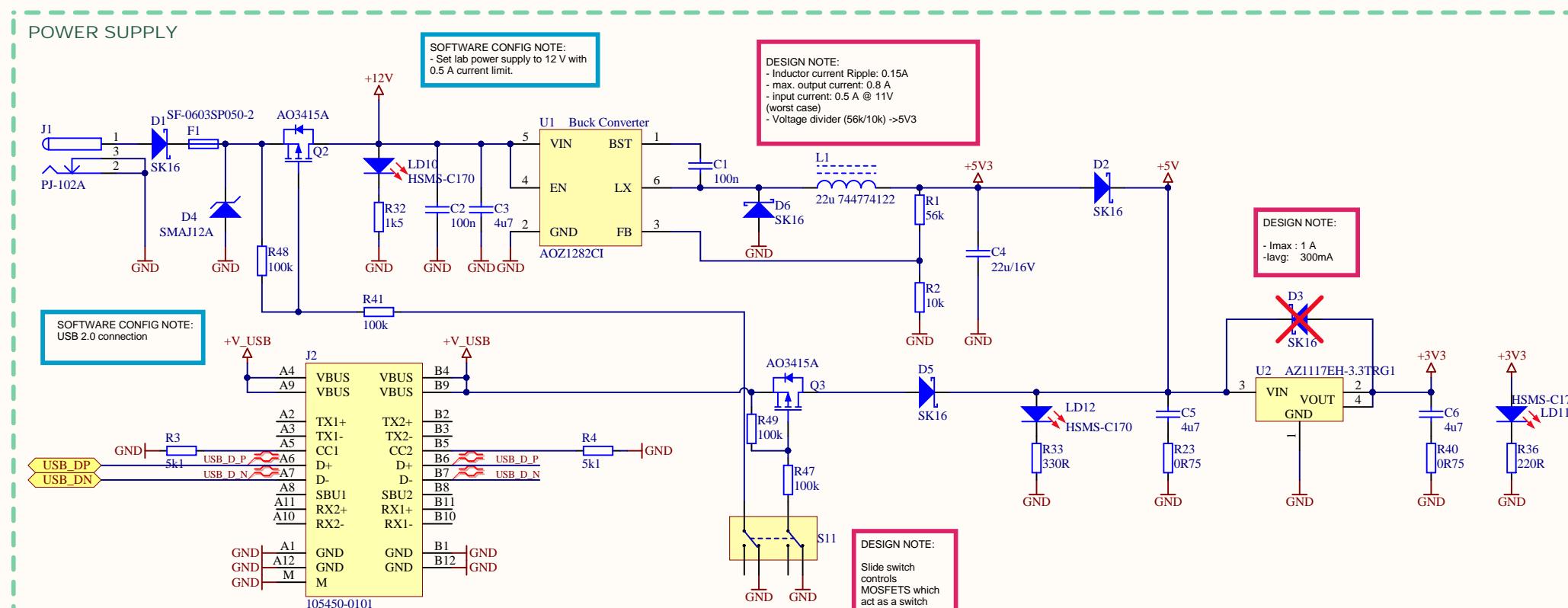
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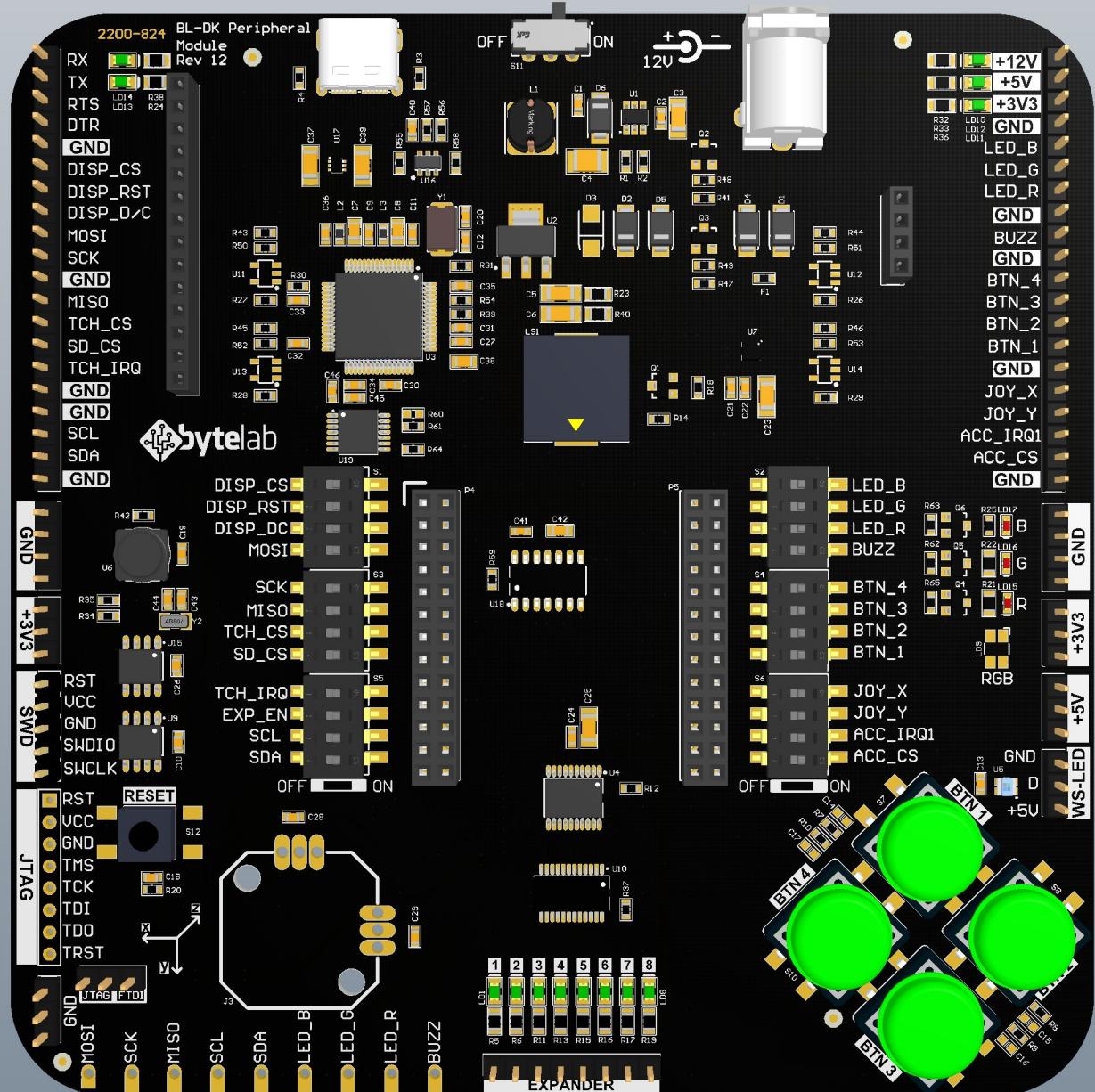
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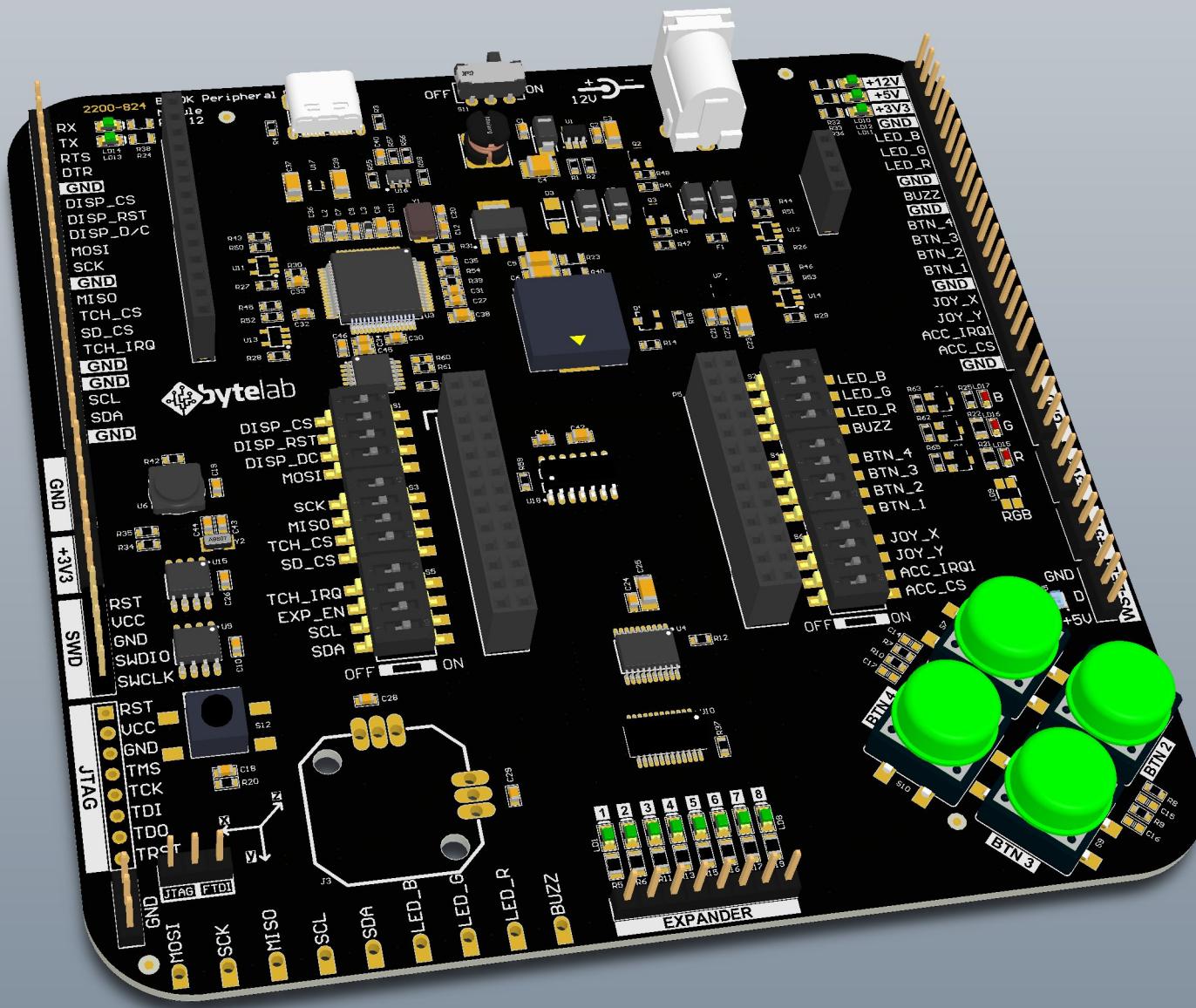
Author:
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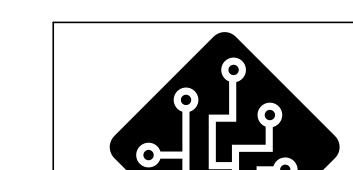
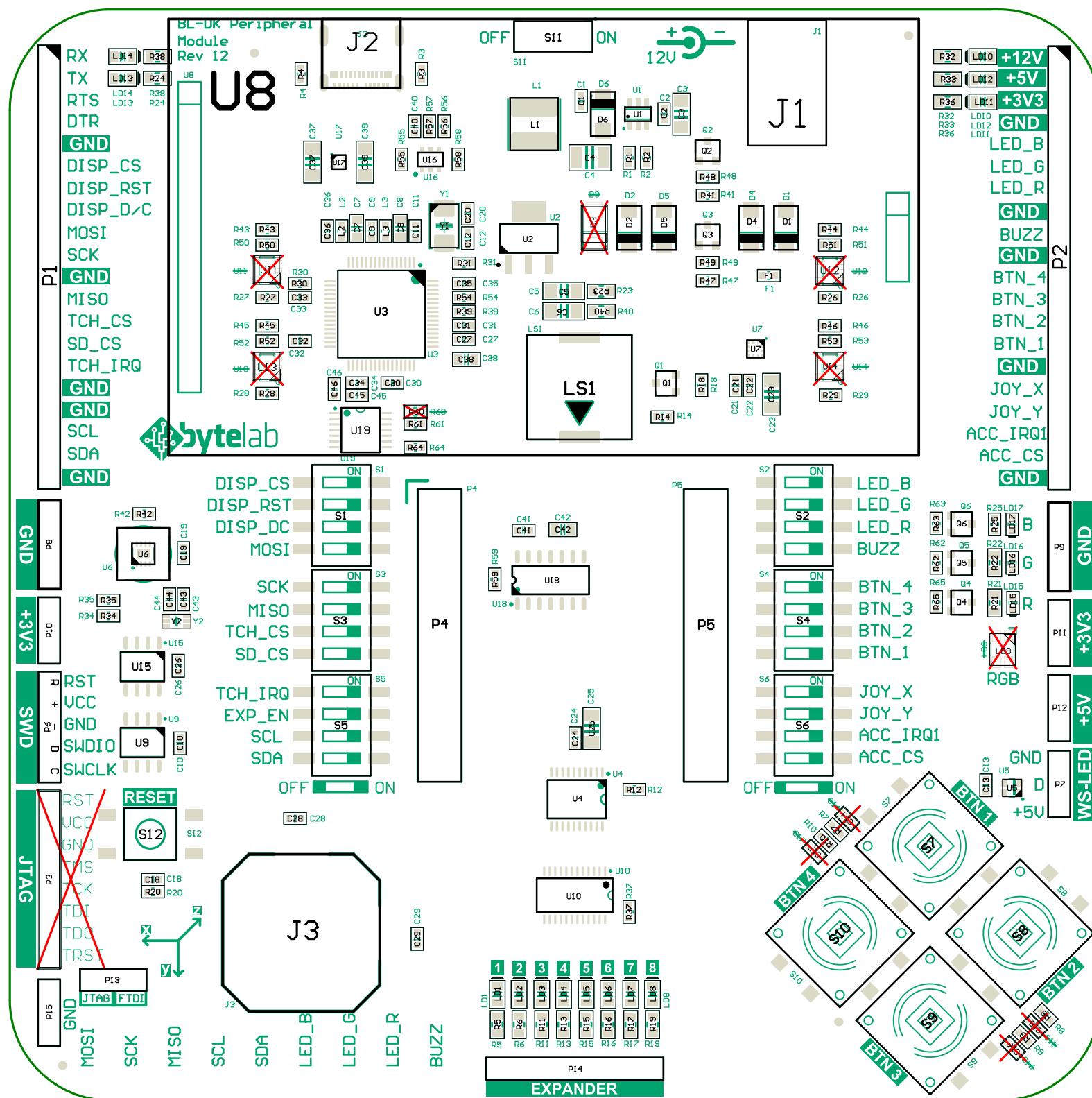








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AUTHOR:	M. Hamin	
ACCEPTOR:	J. Puskar	
BOM NO.:		3000-664-001
DESIGN DOCUMENT NAME: 100210 BLDK Peripheral module Rev. 12		FORMAT: A4