5.5)

```
ENTITY or8g IS
      PORT(i_A:   IN    STD_LOGIC_VECTOR(7 DOWNTO 0);
            o_F  :     OUT   STD_LOGIC);
END or8g;

ARCHITECTURE behavior OF org8 IS
BEGIN
      logic_process:    PROCESS(i_A)
      BEGIN
            IF ( i_A = "00000000" ) THEN
                  o_F   <=    '0';
            ELSE
                  o_F   <=    '1';
            END IF;
      END PROCESS logic_process;
END behavior;
```

7.2)

```
ENTITY dff IS
      PORT(
            S,D,CLK,R   :     IN    STD_LOGIC;
            Q,Inv_Q           :     OUT   STD_LOGIC);
END dff;

ARCHITECTURE behavior OF dff IS
      SIGNAL s_Q  :     STD_LOGIC;
BEGIN
      dff_process: PROCESS(CLK,S,R) IS
      BEGIN
            IF (S = '0') THEN
                  s_Q <= '1';
            ELSIF (R = '0') THEN
                  s_Q <= '0';
            ELSIF (RISING_EDGE(CLK)) THEN
                  s_Q <= D;
            END IF;
      END PROCESS dff_process;

      Q <= s_Q;
      Inv_Q <= NOT s_Q;
END behavior;
```