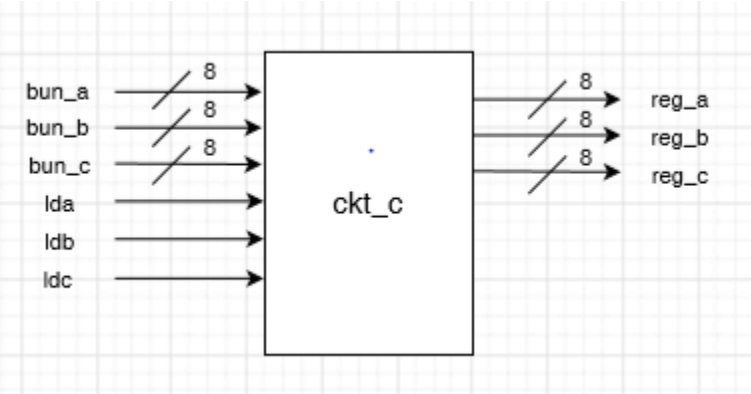
Colby McKinley

PreLab-02

4B)

```
entity sys2 is
      port(input_w : in std_logic;
            a_data : in std_logic_vector(7 downto 0);
            b_data : in std_logic_vector(7 downto 0);
            clk : : in std_logic;
            dat_4 : out std_logic_vector(7 downto 0);
            dat_5 : out std_logic_vector(3 downto 0));
end sys2;
```

5A)



6A)

```
entity ckt_a is
      port(J,K : in std_logic;
            CLK: in std_logic --missing semicolon
            Q : out std_logic;) --semicolon should be on outside parentheses
end ckt_a;
```

6B)

```
entity ckt_b is
      port(mr_fluffy : in std_logic_vector(15 downto 0);
            mux_ctrl : in std_logic_vector(3 downto 0);
            byte_out : out std_logic_vector(3 downto 0); --missing
      parentheses before semicolon
end ckt_b;
```