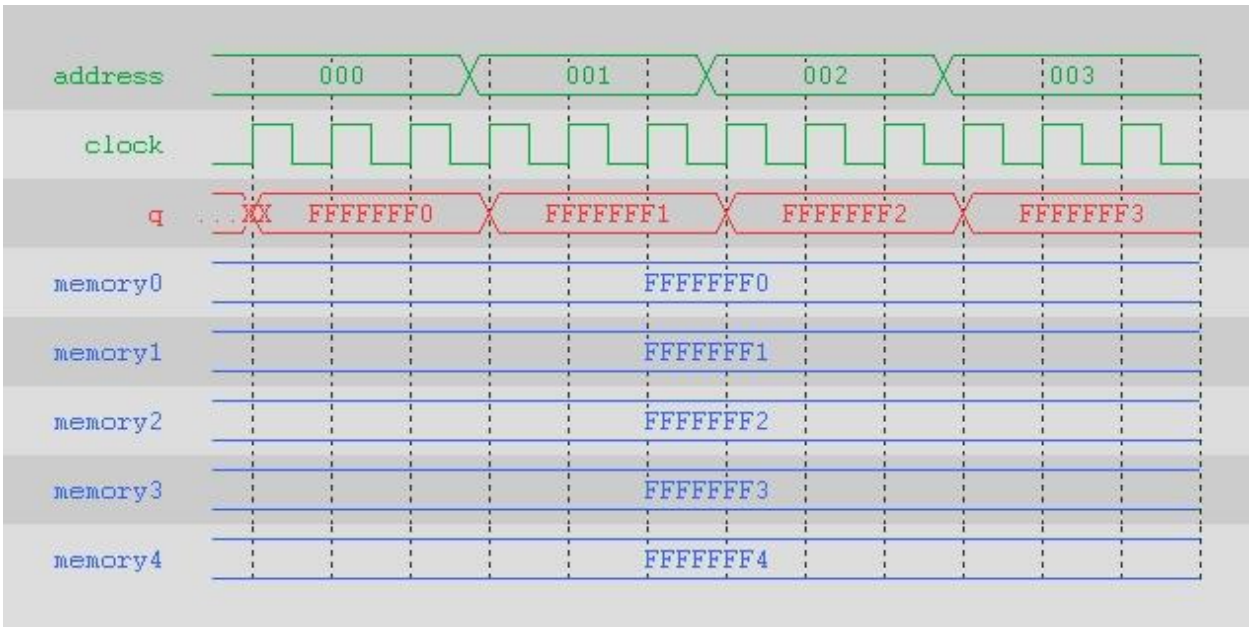
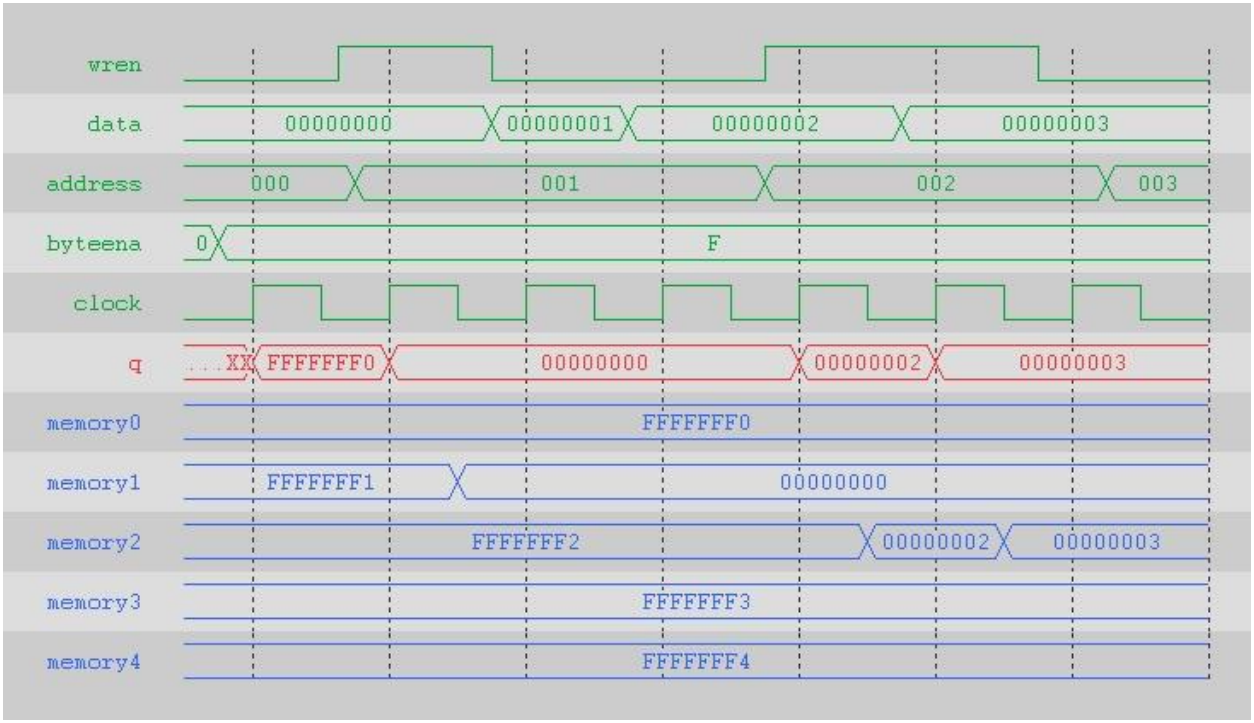
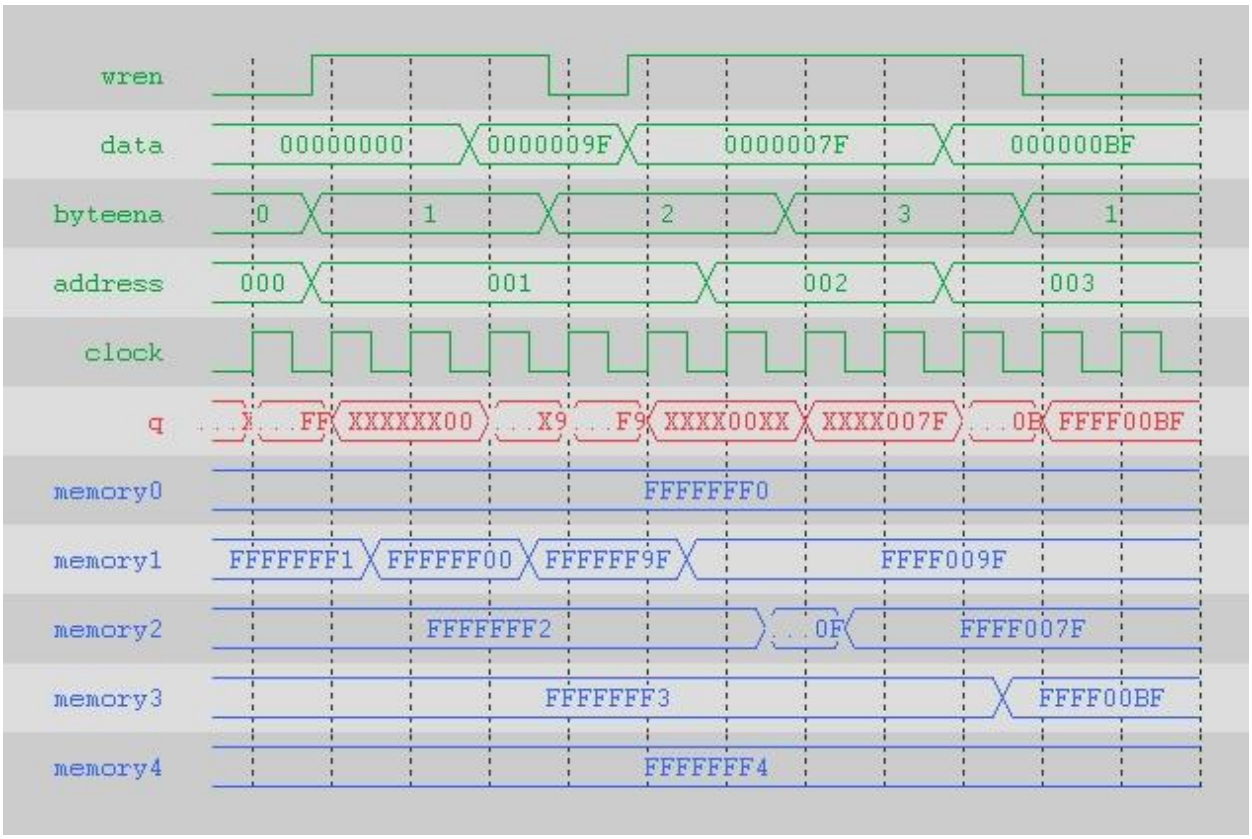


In this first image we observe a module which reads from the from the memory index at the address value into q. Q changes on a rising clock edge.



In this module q is the output of one of the memory addresses which changes on rising clock edge. The memory address which q reads from is the value of address. The wren signal will update the memory location and the value of q to data when it is high. The signal byteena has no obserable effects on any other signal.



In this module we observe the same behavior as the previous one. This time we can see the byteena signal determine how many bits being written to memory or being driven in q. The value in the signal byteena represents a 2 bytes, ie a value of 1 turns on (XXFF), 2 turns on (FFXX), 3 turns on (FFFF), and any previously driven bytes remain unaffected.