CprE 381 – Computer Organization and Assembly-Level Programming

Lab-03 Report

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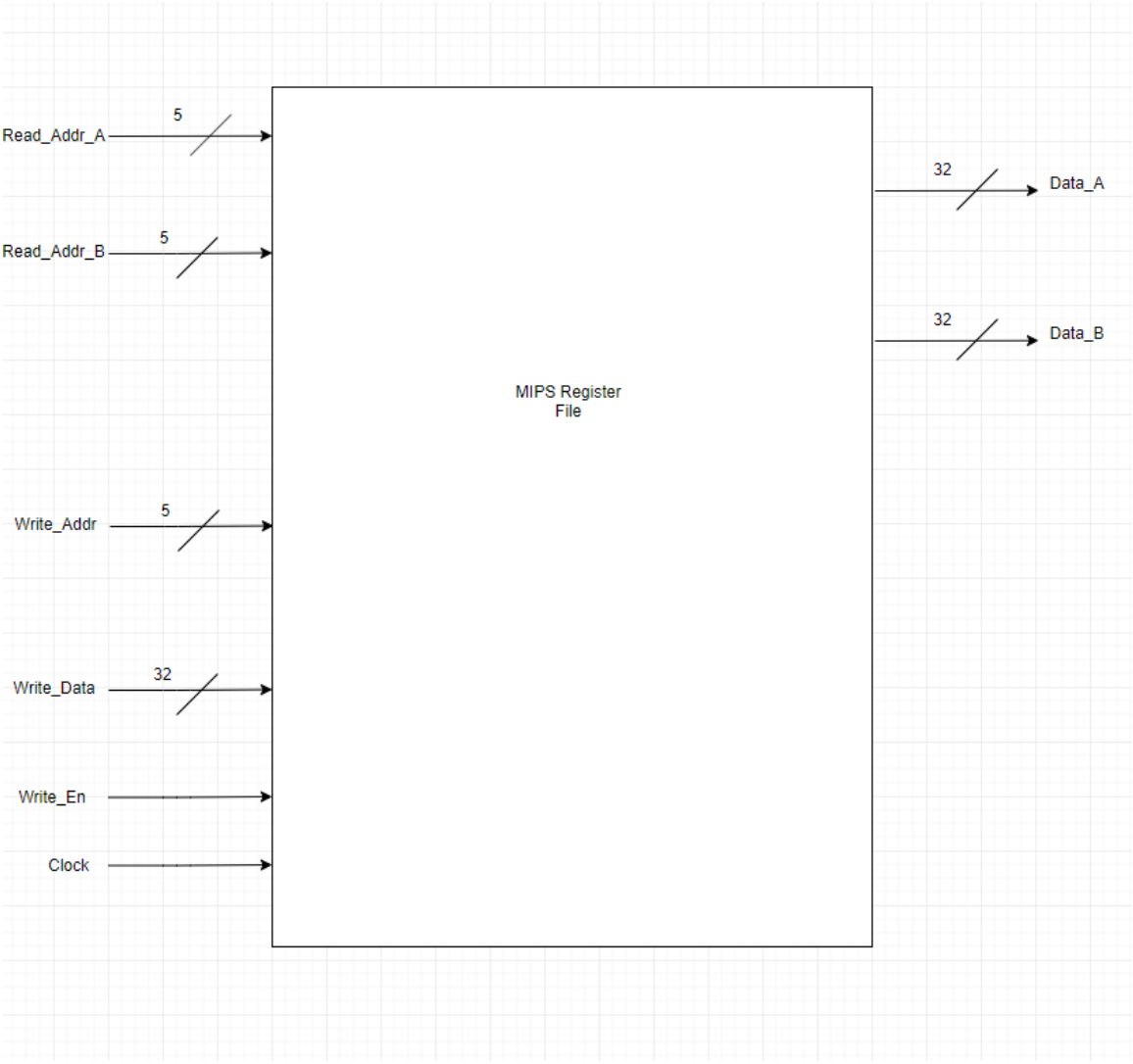
Section / Lab Time Section 5 / W 6:10 – 8:00p

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

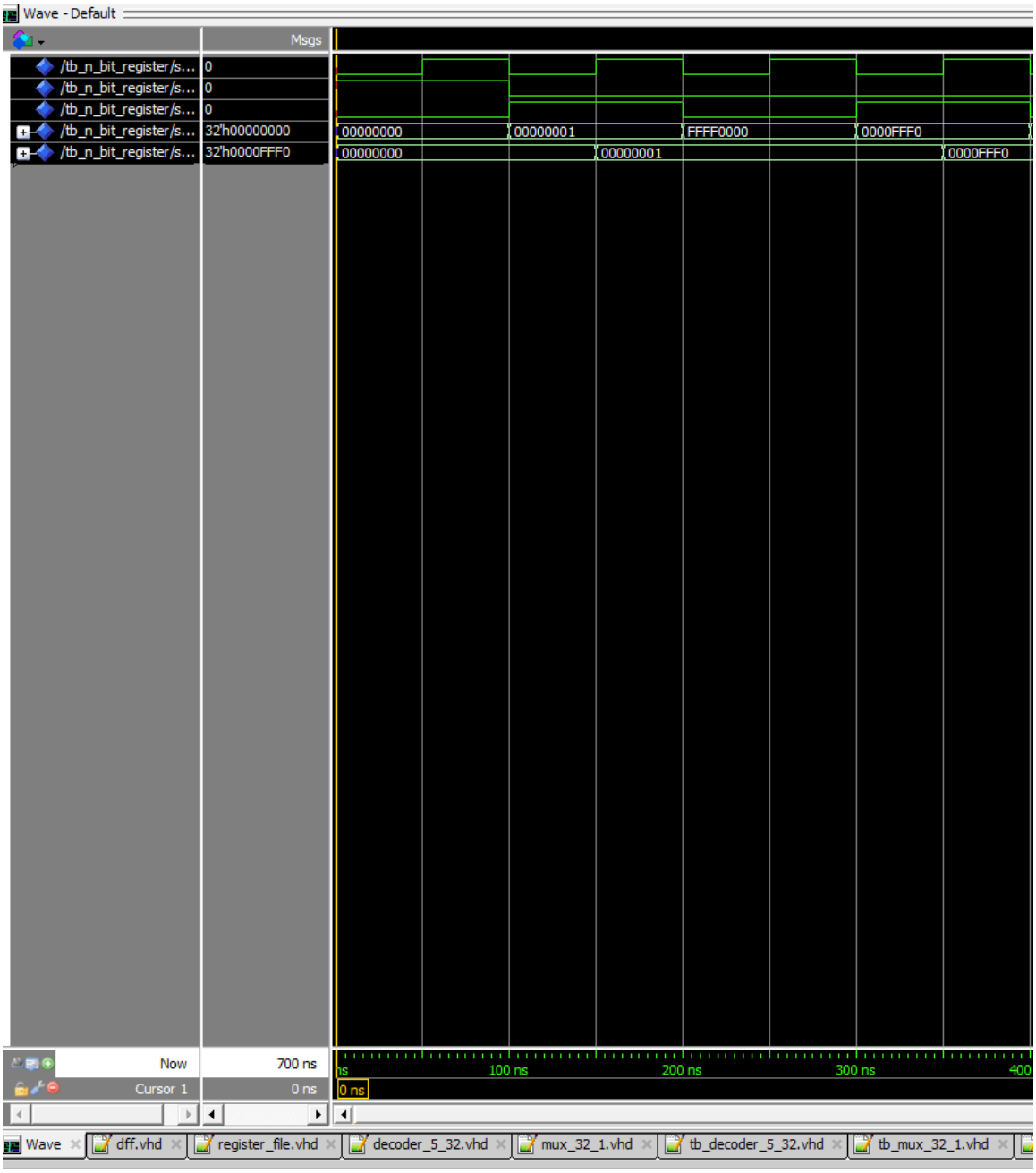
a. [Prelab] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.
   See /Prelab3.pdf
b. [Prelab] In your Lab #3 report PDF, provide the Canvas group name for your project team, and a listing of its members. On a scale of 1-10, how comfortable with VHDL does each team member currently feel?
   Group 4
   Colby – 5
   Tyler – 7

c. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?



d. [Part 1 (b)] Create an N-bit register using this flip-flop as your basis.

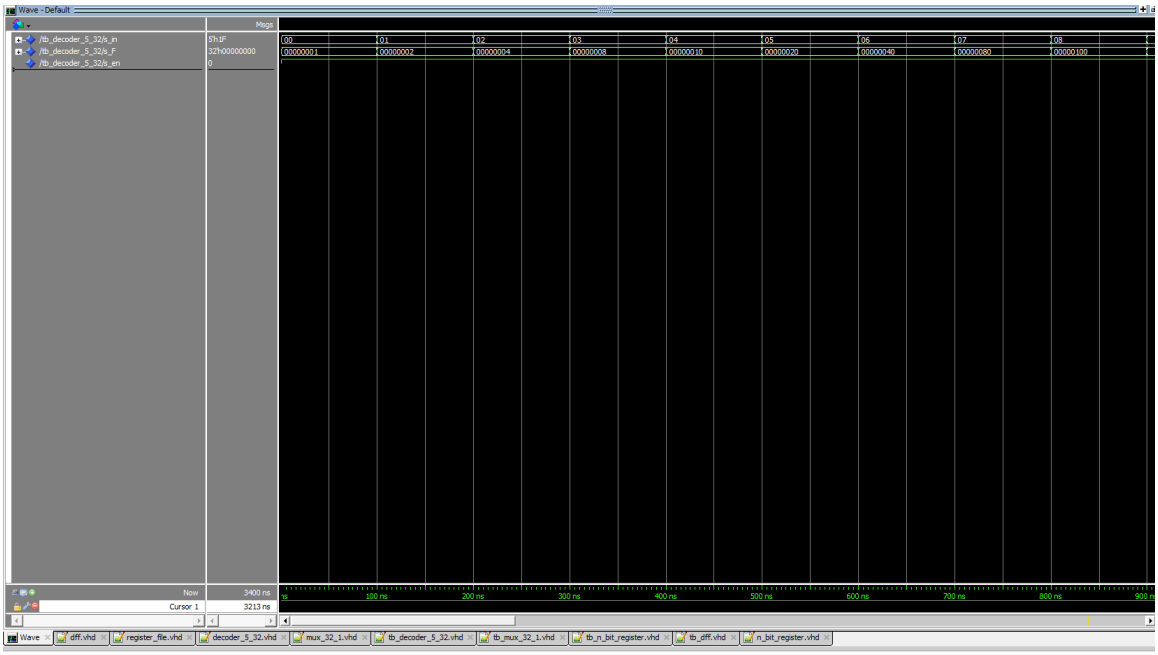
e. [Part 1 (c)] Waveform.



f. [Part 1 (d)] What type of decoder would be required by the MIPS register file and why?

In MIPS since there are 32 available registers, a 5 to 32 decoder is required. I will use each read address to as a select line into a decoder to indexing into one of 32 available registers. By making a 5 to 32 decoder, I can use a single 5 bit address bus easier and cleaner, than using single bit many signals for many single bit decoders.

g. [Part 1 (e)] Waveform.

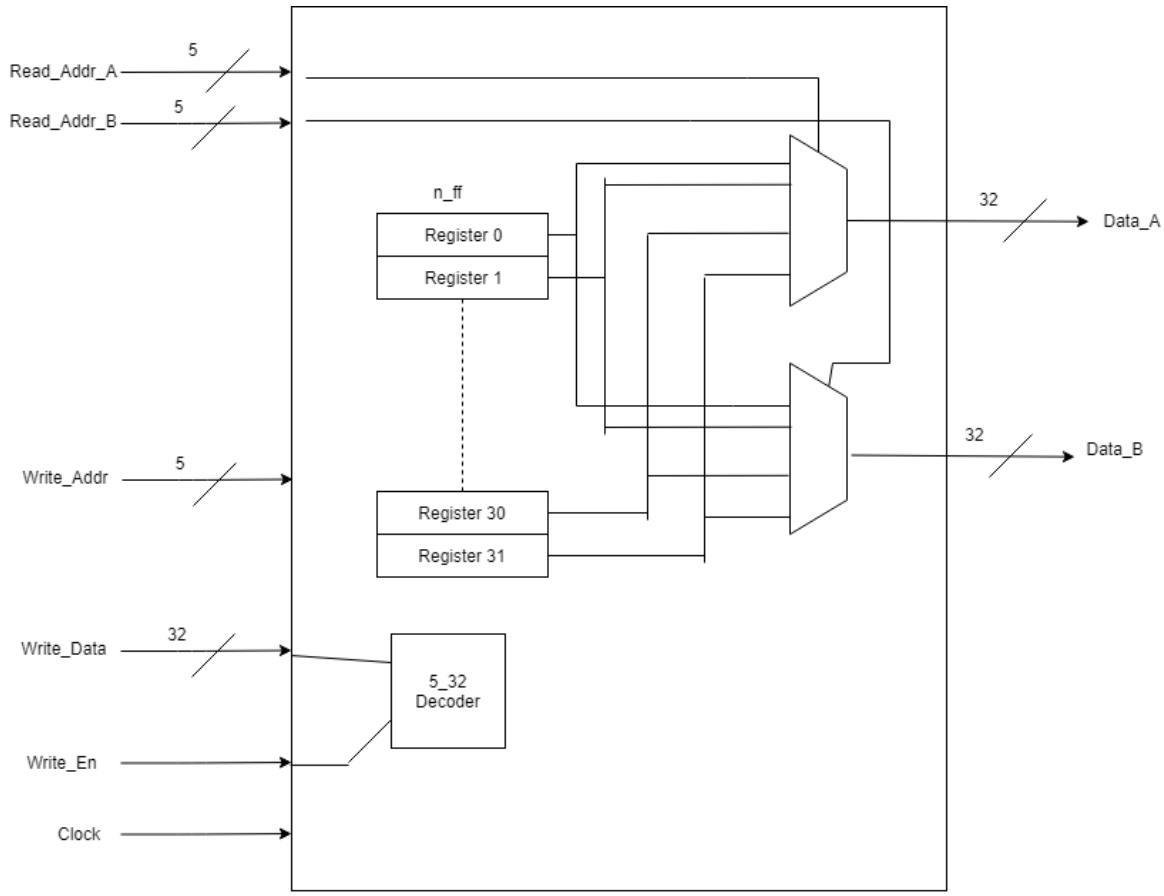


h. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

I plan to thing of the input line as an array of 32 32-bit vectors. This will simplify the code from having 32 32-bit input vectors to a single array. Then using the select line, I can index the bits into the index of the vector in the array.

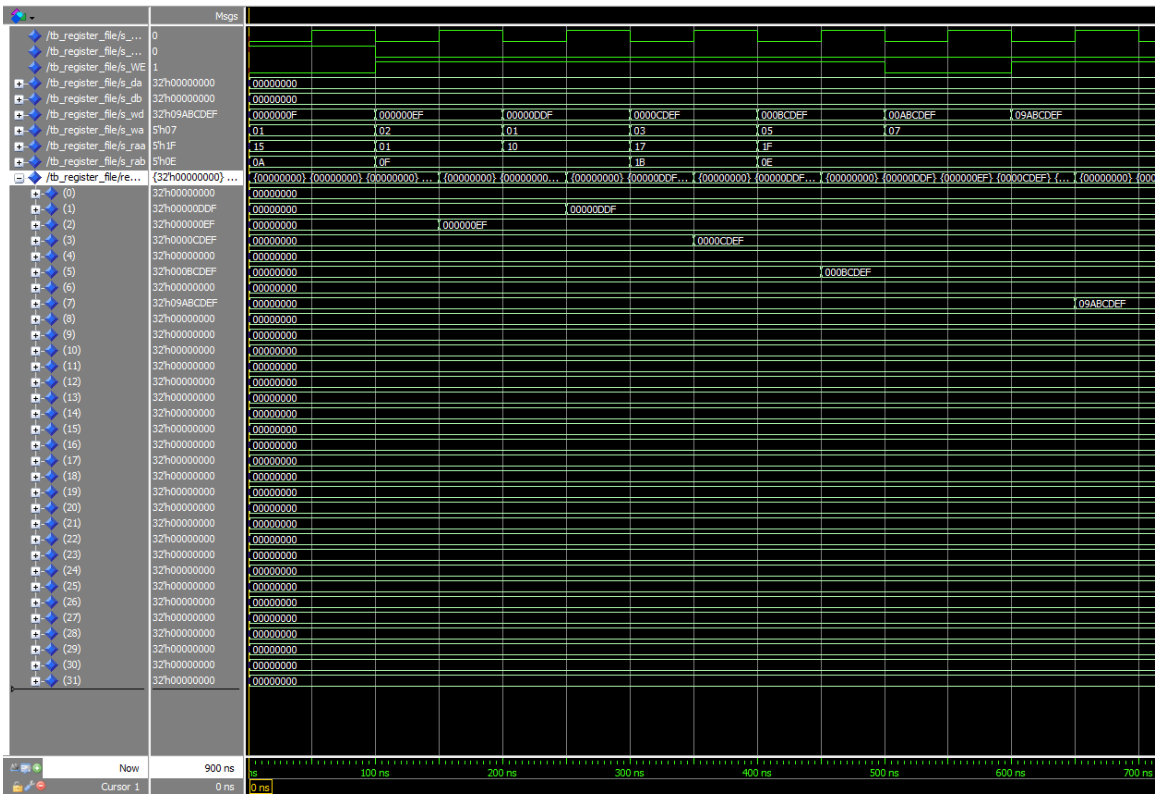
i. [Part 1 (g)] Waveform.

j. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).

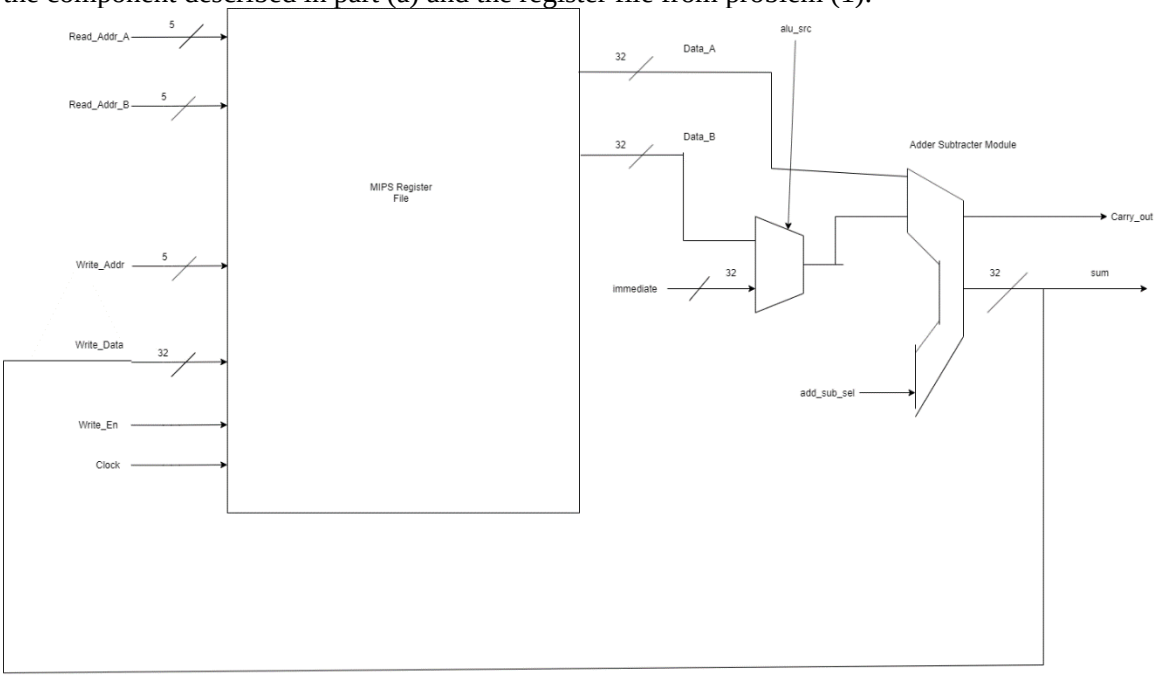


The decoder will be then write enable for each of the registesrs in the n_ff

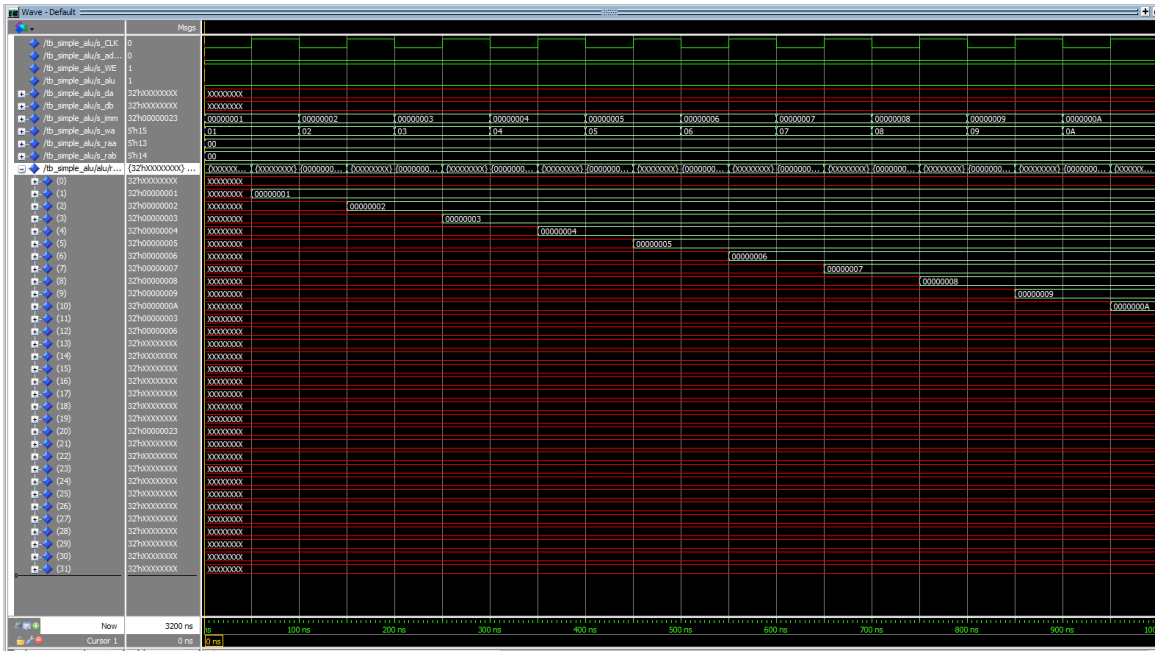
k. [Part 1 (i)] Waveform.



l. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).



m. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.



n. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	10 mintues	
Pencil/paper design		1 hour
VHDL design	2 hours	5 hours
Assembly coding	0 minutes	0 mintues
Simulation	0 minutes	1.5 hours
Debugging	0 minutes	1.5 hours
Report writing	0 minutes	1 hour
Other:		
Total	2 hours 10 minutes	10 hours

ii. If you could change one thing about the lab experience, what would it be? Why?

If there was a power point refresher on dff and register files would have helped lowered the time involved in this lab. It took me a little bit of time to get enough information to design the register file and a lot more time to know how I should be testing my files to make sure they are correct.

iii. What was the most interesting part of the lab?

The register file probably amazed me the most.