# CprE 381 – Computer Organization and

# Assembly-Level Programming

# Lab-01 Report

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## Section / Lab Time Section 5 / W 6:10 – 8:00

***Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-01 instructions for the context of the following questions****.*

1. [Part 1 (b)] Reference the circuit diagram at the end of this document (some parts simplified). There are 33 labeled areas in the diagram. For 15 of these labels, specify where (VHDL file and line number) these values are located – some will be found in more than one place. Also attempt to explain the functionality of each label as it occurs in the code.

(5) is the clock signal, defined on line 24 of Quadratic.vhd. It serves as the driving signal to update the internal components of Quadratic.vhd.

(6) is one of the inputs to the level one multiplier, g\_Mult1 (11) of Quadratic.vhd, defined on line 68. This input takes from the source signal cA (1).

(7) is one of the inputs to the level one multiplier, g\_Mult1 (11) of Quadratic.vhd, defined on line 69. This input takes from the source signal iX (2).

(8) is the multiplication step in the multiplier, which is defined line 41 of Multiplier.vhd. This step will compute the product of the two inputs, which are (6) and (7).

(9) is the conditional statement of the multiplier block, which is defined on line 40 of Multiplier.vhd. It controls if the computation, (8) can be assigned to the internal output signal, (10).

(10) is the output signal for the multiplier, defined on line 31. It is connected to the wire sVALUE\_BxpC, and wired to (21)

(11) is the level one multiplier, g\_Mult1 of Quadratic.vhd, defined on line 66. This block computers the product of the constant value cA (6) by the input value iX (7).

(12) is one of the inputs to the level one multiplier, g\_Mult2 (15) of Quadratic.vhd, defined on line 74. This input takes from the source signal cB (3).

(13) is one of the inputs to the level one multiplier, g\_Mult2 (15) of Quadratic.vhd, defined on line 75. This input takes from the source signal iX (2).

(14) is the product computed by to the level one multiplier, g\_Mult2 (15) of Multiplier.vhd, defined on line 31. This signal result is the product of iA (12) and iB (13) which is assigned by line 41, and is externally labeled as sVALUE\_Bx.

(15) is the level one multiplier, g\_Mult2 of Quadratic.vhd, defined on line 72. This block computers the product of the constant value cA (12) by the input value iX (13).

(16) is the input signal iA to g\_Add1 (30), which is defined on line 29 of Adder.vhd. The source of the signal is (15), the wire labeled sVALUE\_Bx.

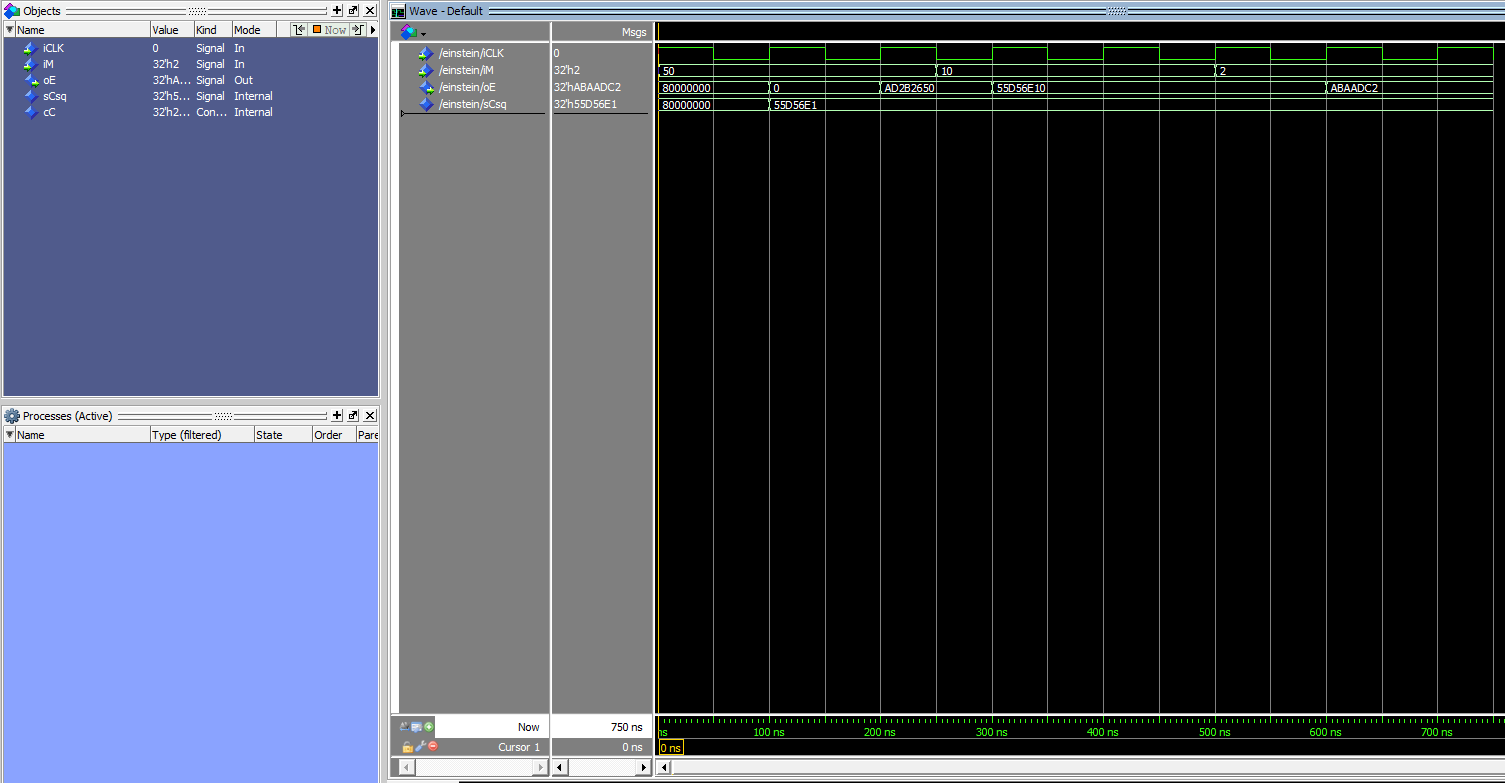
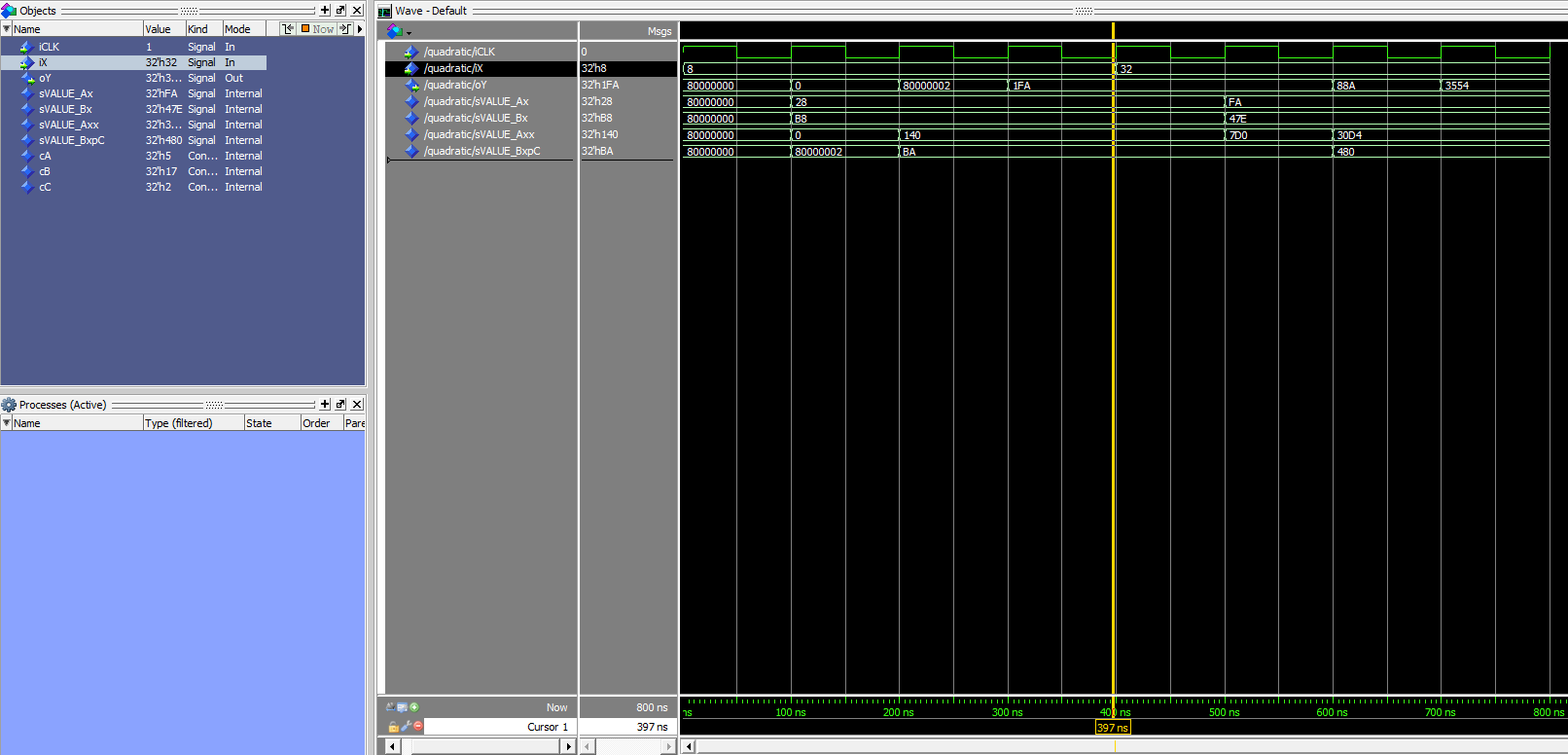
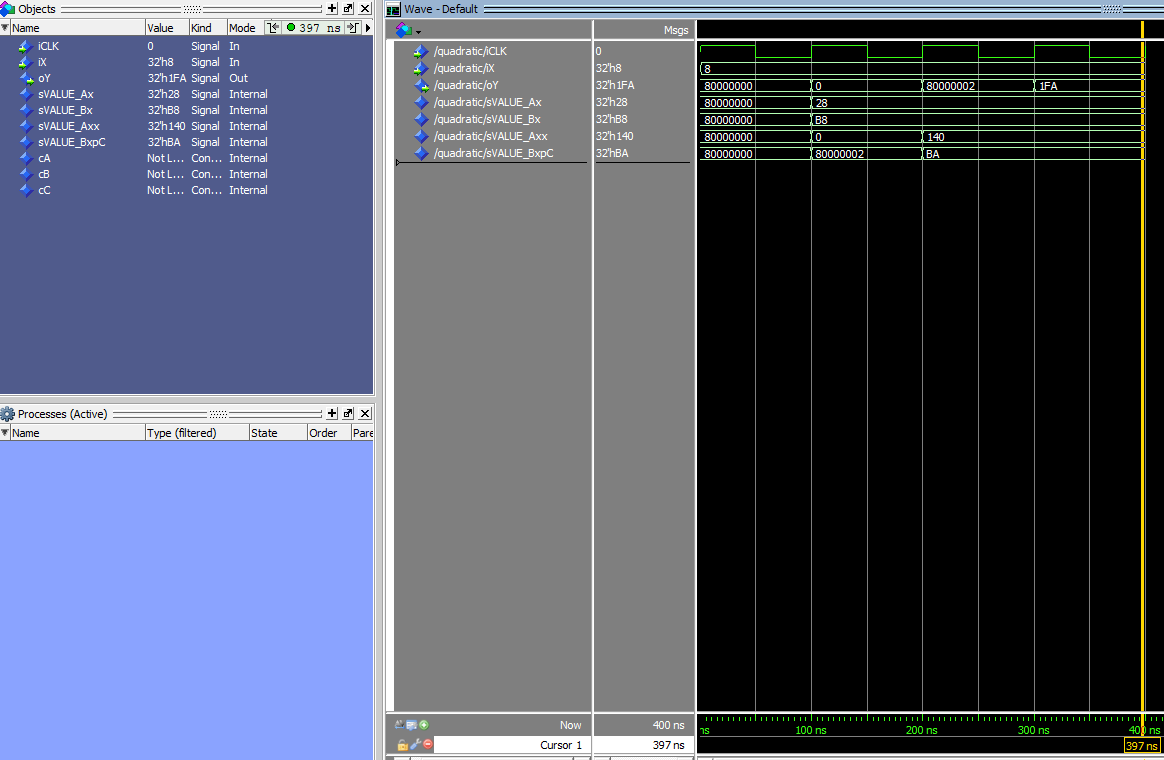
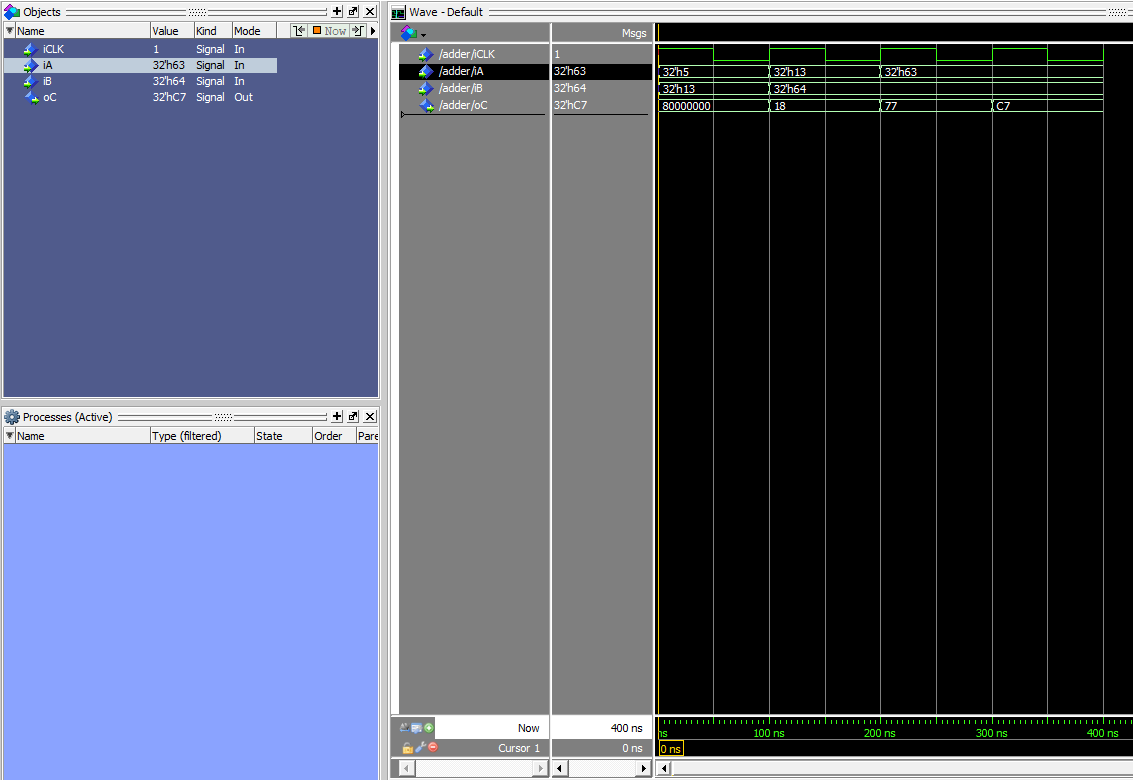
(17) is the input signal iB to g\_Add1 (30), which is defined on line 30 of Adder.vhd. The source is the constant signal cC (4).

(18) is the addition step in the adder, which is defined on line 41. It takes (16) and (17) as inputs to sum.

(19) is the conditional statement of the adder block, which is defined on line 40 of Multiplier.vhd. It controls if the computation, (18) can be assigned to the internal output signal, (20). This is wired, labeled sVALUE\_BxpC, is the input for (26).

1. [Part 1 (h)] In your report, provide a brief explanation of how the timing waveform corresponds to your understanding of the adder design.

The timing waveform to be a collection of signals composed in the VHDL file. There is a clock signal, which drives the outputs of the other signals, depending on how there were set up. Since all of the components were depending on the rising edge of the clock, at each rising edge, the internal signal values were updated. For the designed of Adder.vhd, all the computations were able to be computed in a single clock cycle, so there was never an undriven value for these wires. The number above the line corresponds to that signals output for that period of time.



1. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).
   1. How many hours did you spend on this lab?

|  |  |  |
| --- | --- | --- |
| **Task** | **During lab time** | **Outside of lab time** |
| Reading lab | 10 minutes | 0 minutes |
| Pencil/paper design | 0 minutes | 0 minutes |
| VHDL design | 20 minutes | 0 minutes |
| Assembly coding | 0 minutes | 0 minutes |
| Simulation | 30 minutes | 0 minutes |
| Debugging | 30 minutes | 0 minutes |
| Report writing | 15 minutes | 1 hr |
| Other: |  |  |
| Total | 1 hr 45 minutes | 2 hr 45 minutes |

* 1. If you could change one thing about the lab experience, what would it be? Why?

I would add another section which walks you through designing a testing bench for Quadratic.vhd would have been useful. I found out about hardware test benches at the end of 281 (during the final project), and I think using test benches would have made the labs and final project gone smoother.

* 1. What was the most interesting part of the lab?

I think the most interesting part of the lab was learning ModelSim. The program looks to have a lot more control over hardware designs than Quartus. I also learned that compiling top level designs will not compile the underlying designs.