# CprE 381 – Computer Organization and

# Assembly-Level Programming

# Lab-02 Report

Student Name Colby McKinley

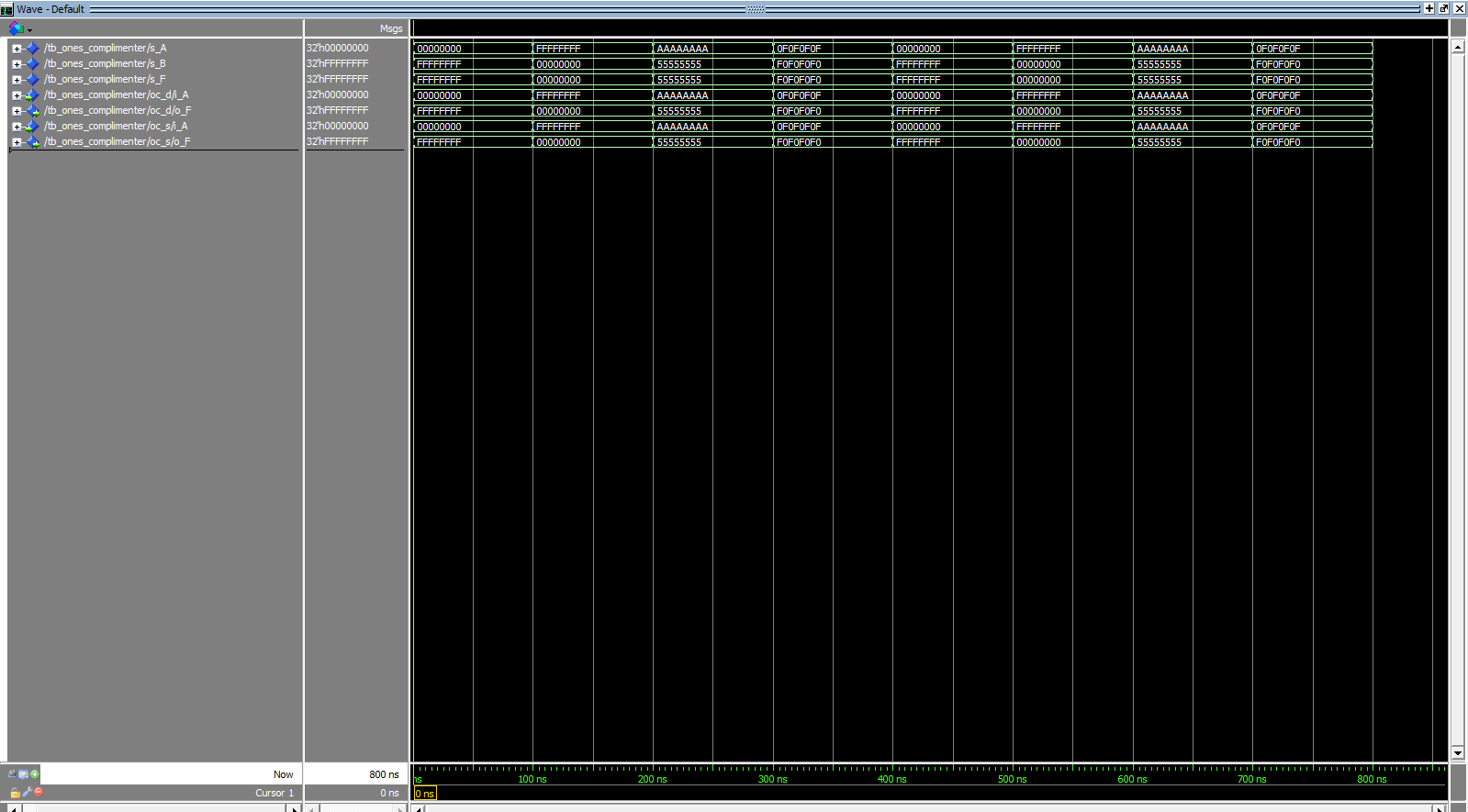
## Section / Lab Time Section 5/ W6:10 – 8:00p

***Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-02 instructions for the context of the following questions****.*

1. [Prelab] At the end of Chapter 3, answer questions 4b), 5a), and 6.

See /Prelab2.pdf

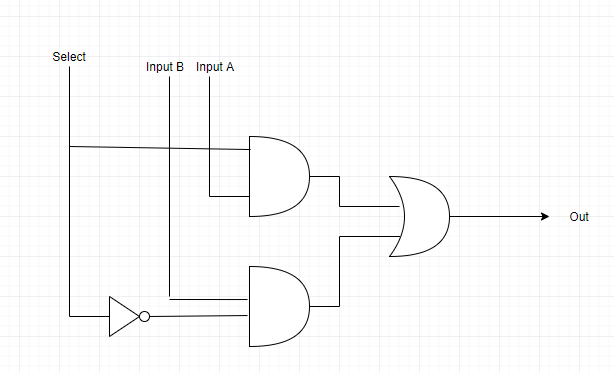
1. [Part 1 (c)] Waveform.



1. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux.

|  |  |  |  |
| --- | --- | --- | --- |
| In A (A) | In B (B) | Select (S) | Out (O) |
| X | X | 0 | In A |
| X | X | 1 | In B |

Boolean Equation:



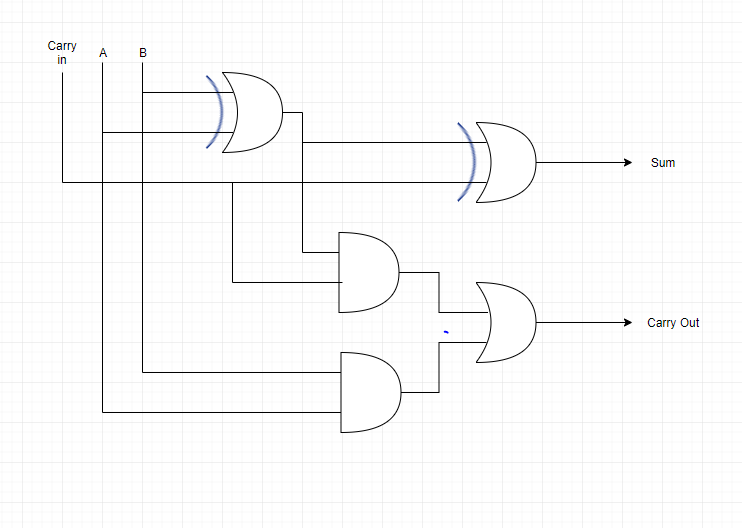
1. [Part 2 (e)] Waveform.



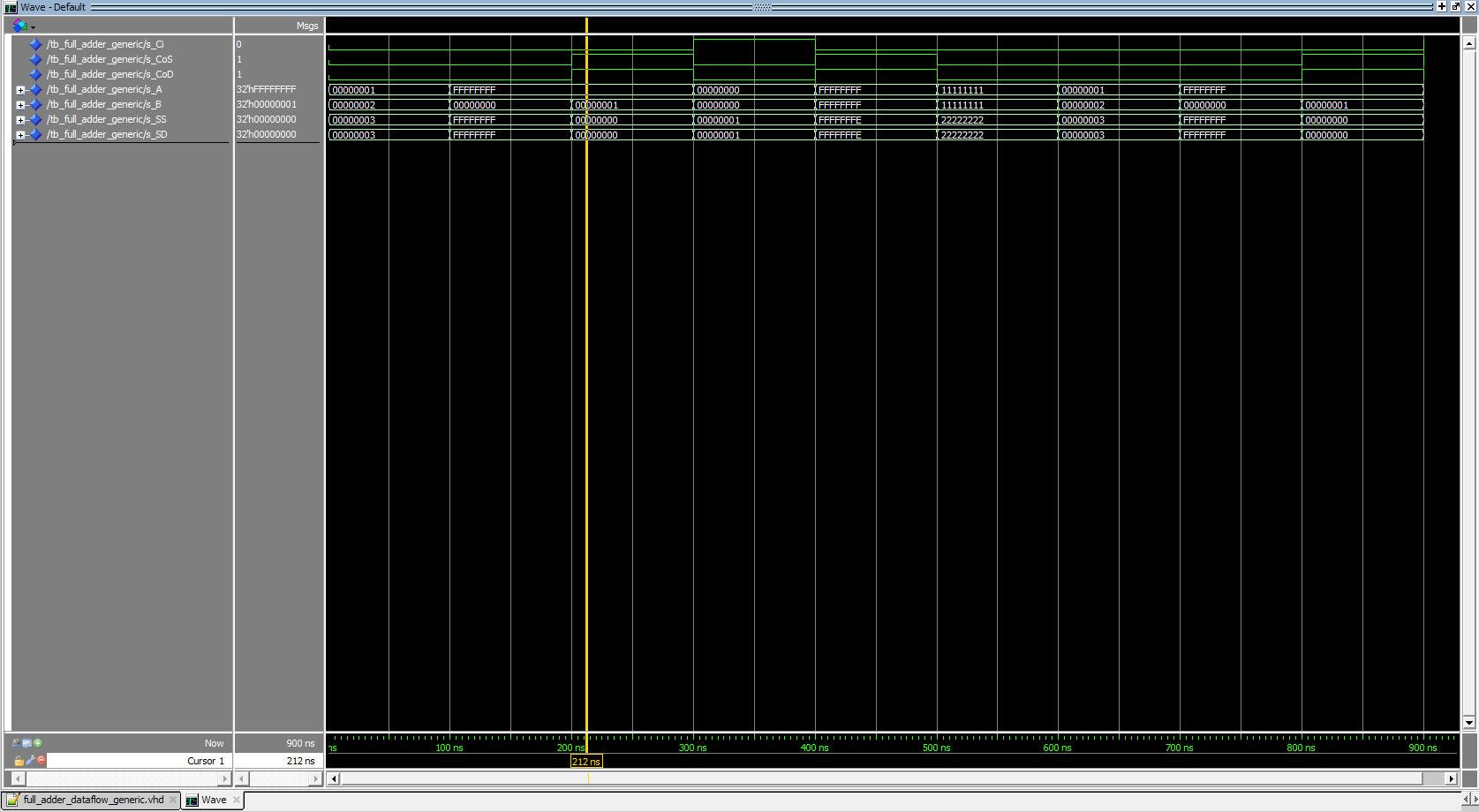
1. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input A (A) | Input B (B) | Carry in (Cin) | Sum (S) | Carry out (Cout) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

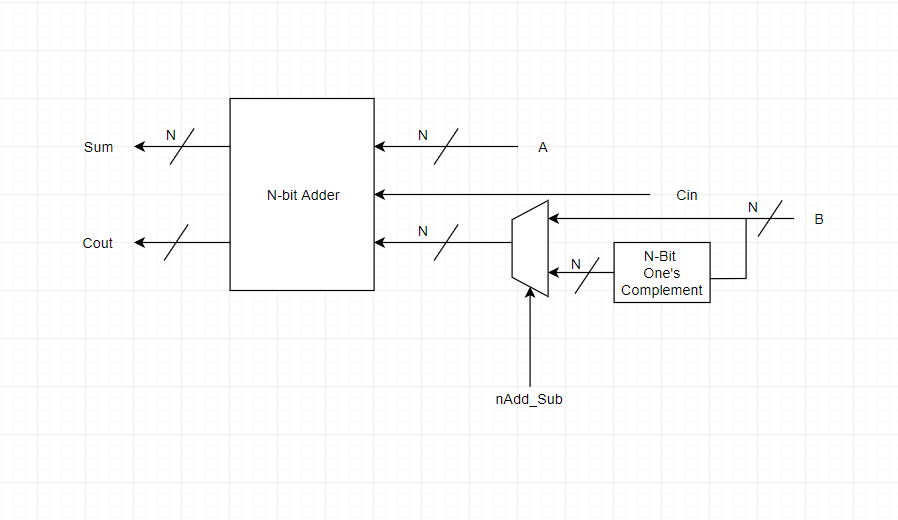
Boolean expression: in



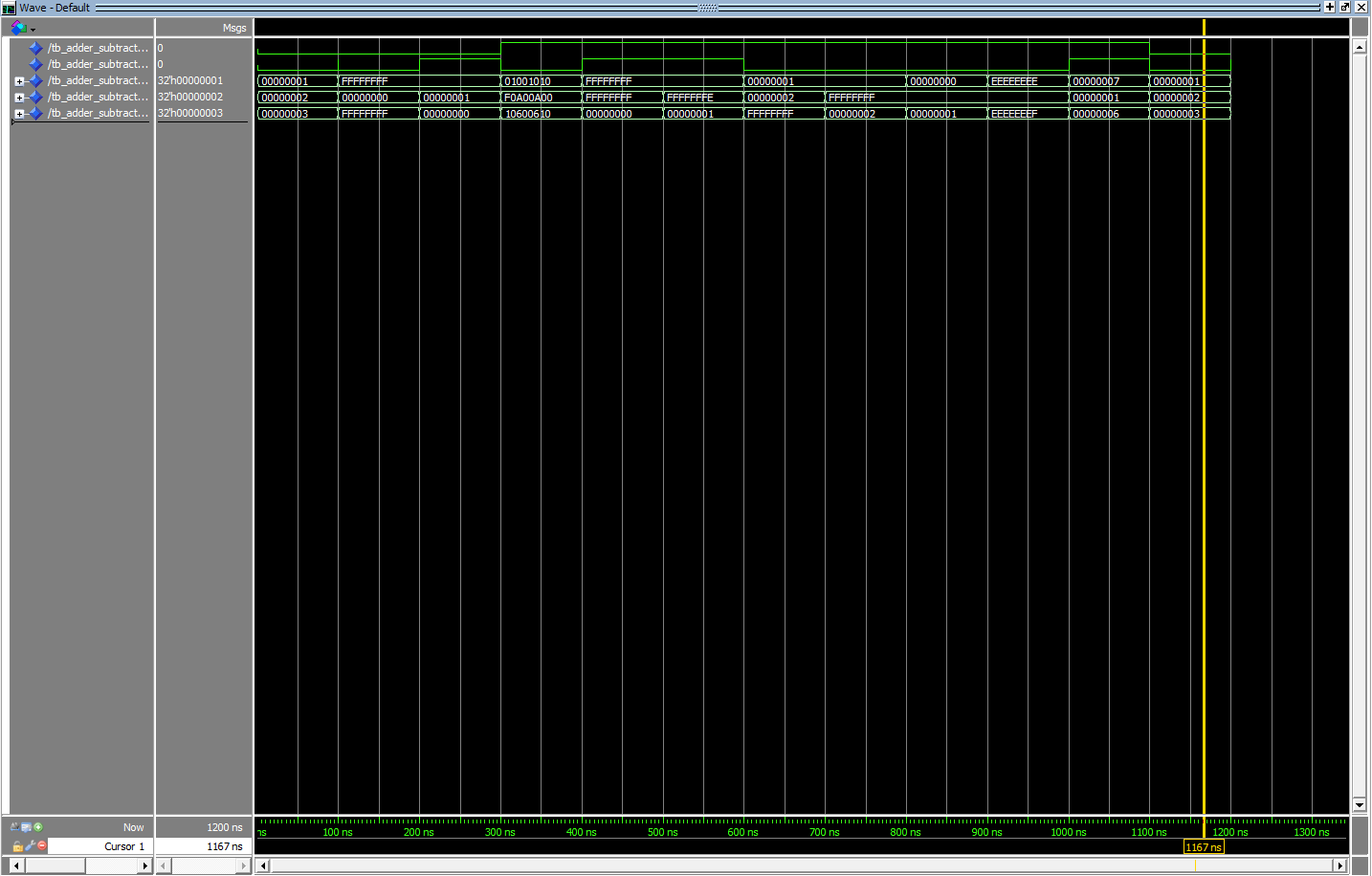
1. [Part 3 (e)] Waveform.



1. [Part 4 (a)] Draw a schematic (don’t use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the ‘nAdd\_Sub’ bit used?



1. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?



I include test cases where overflow or underflow should have occurred, along with a few normal cases. I wanted to test possible paths of the adder/subtractor.

1. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).
   1. How many hours did you spend on this lab?

|  |  |  |
| --- | --- | --- |
| **Task** | **During lab time** | **Outside of lab time** |
| Reading lab | 15 minutes | 0 minutes |
| Pencil/paper design | 20 minutes | 45 minutes |
| VHDL design | 35 minutes | 3 hr |
| Assembly coding | 0 minutes | 0 minutes |
| Simulation | 30 minutes | 1 hr |
| Debugging | 30 minutes | 2 hr |
| Report writing | 0 minutes | 1 hr |
| Other: |  |  |
| Total | 2 hr | 7hr 45 minutes |

* 1. If you could change one thing about the lab experience, what would it be? Why?

Allow drawing the semantics to be done by hand or Quartus. It takes way to long with the drawing tools.

* 1. What was the most interesting part of the lab?

I think the most interesting part of the lab was seeing when dataflow and structural were easiest to implement.