5.5)

**ENTITY** or8g **IS**

**PORT(**i\_A**:** **IN** STD\_LOGIC\_VECTOR**(**7 **DOWNTO** 0**);**

o\_F **:** **OUT** STD\_LOGIC**);**

**END** or8g**;**

**ARCHITECTURE** behavior **OF** org8 **IS**

**BEGIN**

logic\_process**:** **PROCESS(**i\_A**)**

**BEGIN**

**IF** **(** i\_A **=** "00000000" **)** **THEN**

o\_F **<=** '0'**;**

**ELSE**

o\_F **<=** '1'**;**

**END** **IF;**

**END** **PROCESS** logic\_process**;**

**END** behavior**;**

7.2)

**ENTITY** dff **IS**

**PORT(**

S**,**D**,**CLK**,**R **:** **IN** STD\_LOGIC**;**

Q**,**Inv\_Q **:** **OUT** STD\_LOGIC**);**

**END** dff**;**

**ARCHITECTURE** behavior **OF** dff **IS**

**SIGNAL** s\_Q **:** STD\_LOGIC**;**

**BEGIN**

dff\_process**:** **PROCESS(**CLK**,**S**,**R**)** **IS**

**BEGIN**

**IF** **(**S **=** '0'**)** **THEN**

s\_Q **<=** '1'**;**

**ELSIF** **(**R **=** '0'**)** **THEN**

s\_Q **<=** '0'**;**

**ELSIF** **(RISING\_EDGE(**CLK**))** **THEN**

s\_Q **<=** D**;**

**END** **IF;**

**END** **PROCESS** dff\_process**;**

Q **<=** s\_Q**;**

Inv\_Q **<=** NOT s\_Q**;**

**END** behavior**;**