LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY or8g IS

PORT(i\_A: IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

o\_F : OUT STD\_LOGIC);

END or8g;

ARCHITECTURE behavior OF org8 IS

BEGIN

logic\_process: PROCESS(ins)

BEGIN

IF ( ins = "00000000" ) THEN

o\_F <= '0';

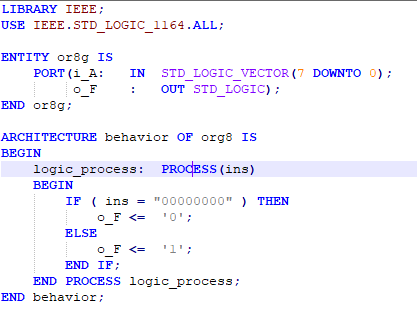
ELSE

o\_F <= '1';

END IF;

END PROCESS logic\_process;

END behavior;



LIBRARY IEEE;

USE ieee.std\_logic\_1164.all;

ENTITY dff\_1 IS

PORT(

S,D,CLK,R : IN STD\_LOGIC;

Q,Inv\_Q : OUT STD\_LOGIC);

END dff\_1;

ARCHITECTURE behavior OF dff IS

SIGNAL q\_temp : STD\_LOGIC;

BEGIN

dff\_process: PROCESS(CLK,S,R) IS

BEGIN

IF (S = '0') THEN

q\_temp <= '1';

ELSIF (R = '0') THEN

q\_temp <= '0';

ELSIF (RISING\_EDGE(CLK)) THEN

q\_temp <= D;

END IF;

END PROCESS dff\_process;

Q <= q\_temp;

Inv\_Q <= NOT q\_temp;

END behavior;

