5-BIT COMPLEX MULTIPLIER - FSM

VERILOG

[2:-2] — Pre-Binary Bit point

[2 1 . 0 -1 -2] — Post Binary bit point

- 2-input Adder
- 2-input Multiplier
- 3-complex numbers
  - $A = (A_r + A_i j)$
  - $B = (B_r + B_i j)$
  - $C = (C_r + C_i j)$

Product

$A \cdot B \cdot C = P_{real} + P_{imaginary} \cdot j$

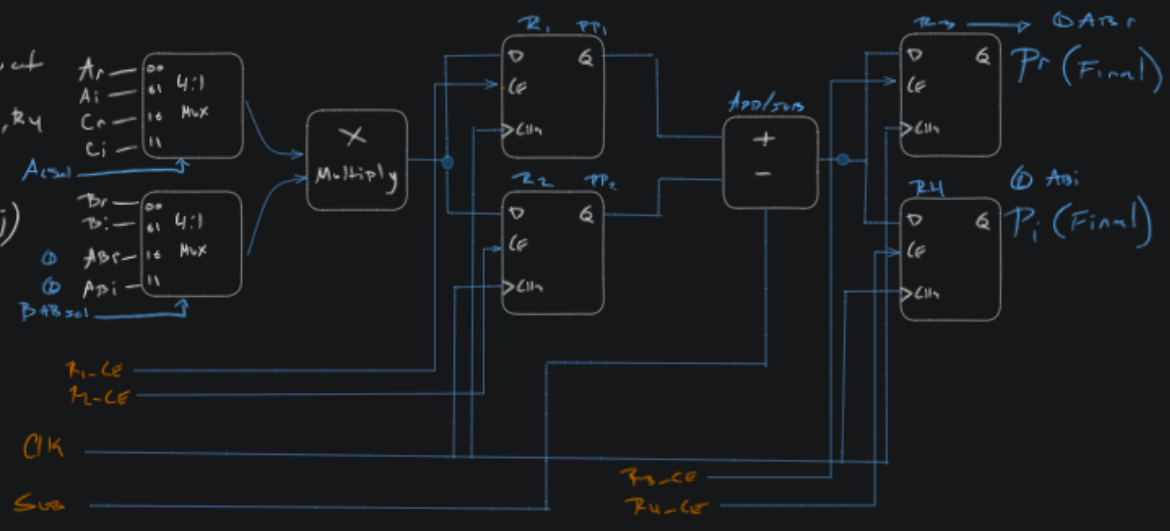
$(A_r \cdot B_r - A_i \cdot B_i) + (A_r \cdot B_i + A_i \cdot B_r) j = AB_r + AB_i j$

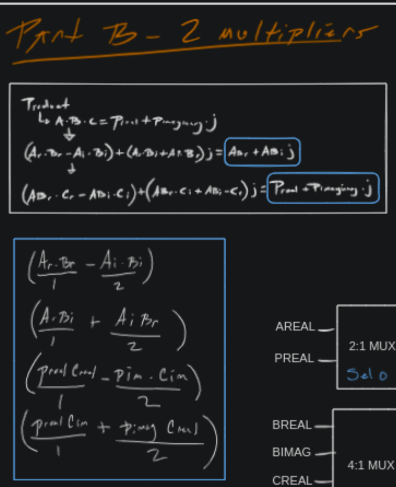
$(AB_r \cdot C_r - AB_i \cdot C_i) + (AB_r \cdot C_i + AB_i \cdot C_r) j = P_{real} + P_{imaginary} \cdot j$

FSM	Step	ac_sel	bab_sel	pp1_e	pp2_e	sub	pr_e	pi_e
0000	1	00	00	1	0	x	0	0
0001	2	01	01	0	1	x	0	0
0010	3	00	01	1	0	1	1	0
0011	4	01	00	0	1	x	0	0
0100	5	10	10	1	0	0	0	1
0101	6	11	11	0	1	x	0	0
0110	7	11	10	1	0	1	1	0
0111	8	10	11	0	1	x	0	0
1000	9	x	x	0	0	0	0	1

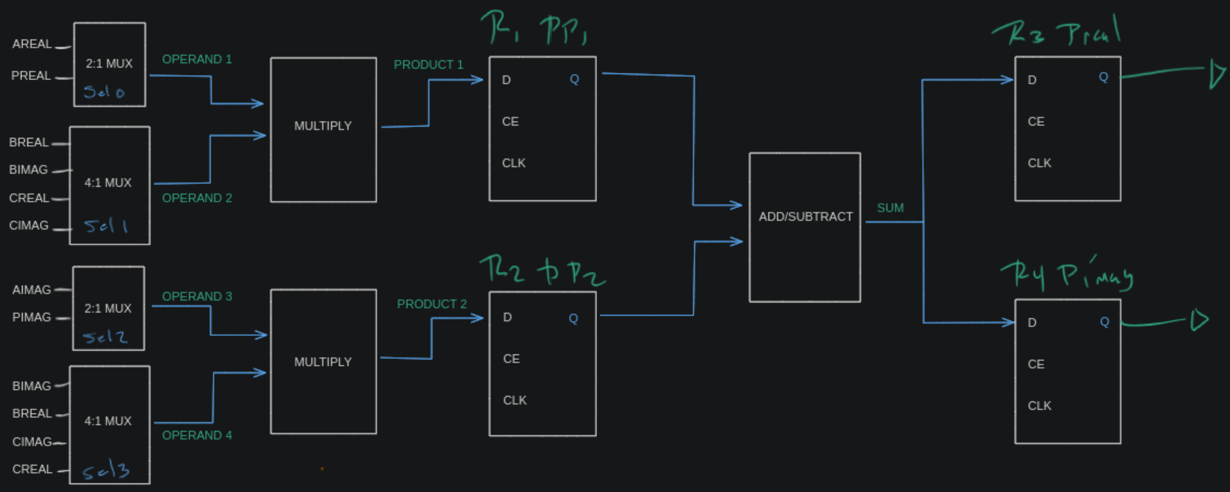
PART A

- Compute 1st product
- Store result in R3, R4
- Route result to MUX
- Multiply by $(C_r + C_i j)$

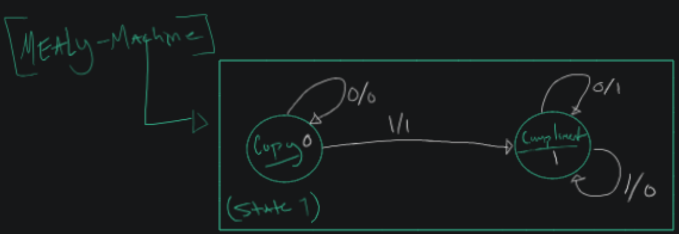




FSM	Step	sel-0	sel-1	sel-2	sel-3	pp1_e	pp2_e	sub	pr_e	pi_e
000	1	0	00	0	00	1	1	x	0	0
001	2	0	01	0	01	1	1	1	1	0
010	3	x	x	x	x	0	0	0	0	1
011	4	1	10	1	10	1	1	x	0	0
100	5	1	11	1	11	1	1	1	1	0
101	6	x	x	x	x	0	0	0	0	1

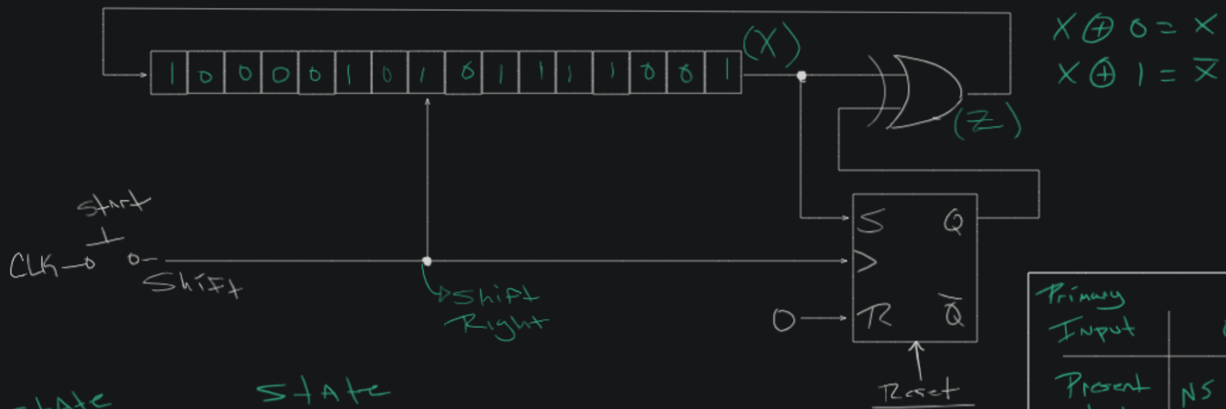


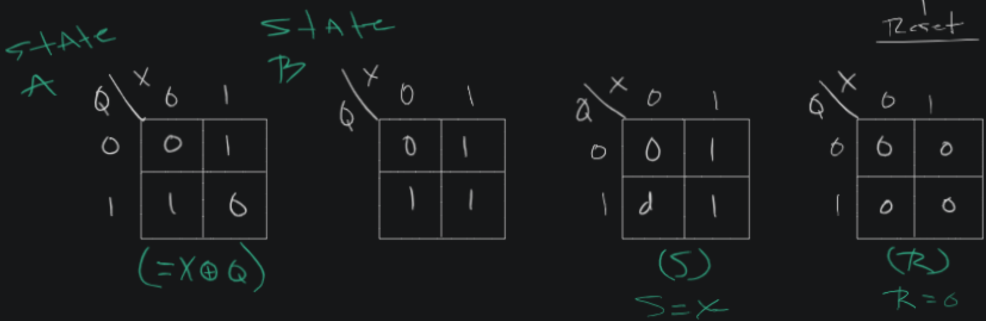
SERIAL 2'S COMPLIMENT (16-BIT)



Q \ Input X	0	1
Copy 0	0/0	1/1
Comp 1	1/1	1/0

Next state/output





Present state	Primary Input 0: NS	Primary output	Primary Input 1: NS	Primary output
A	A	0	B	1
B	B	1	B	0