

Mode: All

Left file: D:\Source\github\CSS422_Hardware\Disassembler\UnitTests\Test_002.X68

Right file: D:\Source\github\CSS422_Hardware\Disassembler\Output.txt

```
*=====
» =====
» =====
* Title      : Test_002
* Written by : CSS 422 Best Group
*
*   The CSS 422 Best Group is:
*   - Howie Catlin
*   - Kyle Dukart
*   - Colton Sellers
*
*
* Date       : 10-Nov-2019
*
* Description:
*   Test input file used to perform software v
» erification
*   and validation (i.e.: validation that the
» disassembler
*   is capable of converting hexadecimal to En
» glish,
*   verification that the the strings being tr
» anslated are
*   in fact correct).
*
*   First parts of this file attempt to prove
» that each
*   operation code is capable of being transla
» ted. The
*   registers D0, D7, A0, & A7 and hex values
» '0', '1', '5',
*   'A', and 'F' as edge cases most likely to
» uncover early
*   programming errors. This method exercises
» all opcodes,
*   but performs less addressing.
*
*   Later in the file, a brute-force matrix of
» every-register
*   to-every-register is employed to verify th
» e Effective
*   Addressing code paths. This method uses fe
» wer op codes,
*   but performs more addressing.
*
*   Refer to the Test Plan and test matrix for
» more
*   information.
*=====
» =====
» =====
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(continued)

TESTIO

* -----

» -----

*** BCLR**

* -----

» -----

```

BCLR      D0,D7
BCLR      D7,(A7)
BCLR      D0,(A0)+
BCLR      D7,-(A7)
BCLR      D0,$FFFF
BCLR      D7,$55555

```

```

111112 BCLR      D0, D7
111114 BCLR      D7, (A7)
111116 BCLR      D0, (A0)+
111118 BCLR      D7, -(A7)
11111A BCLR      D0, $FFFF
111120 BCLR      D7, $55555

```

* -----

» -----

*** ORI**

* -----

» -----

```

ORI.W      #$1111,D0
ORI.W      $AAAA,(A0)+
ORI.W      $0000,-(A0)
ORI.L      $FFFFFF,D0
ORI.L      $55555,(A0)+
ORI.L      $AAAAA,-(A0)

```

```

111126 ORI.W      #$1111, D0
11112A ORI.W      $AAAA, (A0)+
11112E ORI.W      $0, -(A0)
111132 ORI.L      $FFFFFF, D0
111138 ORI.L      $55555, (A0)+
11113E ORI.L      $AAAAA, -(A0)

```

* -----

» -----

*** CMPI**

* -----

» -----

```

CMPI.W      #$1111,D0
CMPI.W      $AAAA,(A0)+
CMPI.W      $0000,-(A0)
CMPI.L      $FFFFFF,D0
CMPI.L      $55555,(A0)+
CMPI.L      $AAAAA,-(A0)

```

```

111144 CMPI.W      #$1111, D0
111148 CMPI.W      $AAAA, (A0)+
11114C CMPI.W      $0, -(A0)
111150 CMPI.L      $FFFFFF, D0
111156 CMPI.L      $55555, (A0)+
11115C CMPI.L      $AAAAA, -(A0)

```

* -----

» -----

*** MOVE.B**

* -----

» -----

```

MOVE.B      $0F,D0
MOVE.B      D7,(A7)
MOVE.B      D7,(A0)+
MOVE.B      D0,-(A7)
MOVE.B      $1000,D0
MOVE.B      $10000,D0

```

```

111162 MOVE.B      #F, D0
111166 MOVE.B      D7, (A7)
111168 MOVE.B      D7, (A0)+
11116A MOVE.B      D0, -(A7)
11116C MOVE.B      $1000, D0
111170 MOVE.B      $10000, D0

```

```

MOVE.W      $AA,D0
MOVE.W      D7,A0
MOVE.W      D7,(A7)
MOVE.W      D0,(A0)+
MOVE.W      D7,-(A7)

```

```

111176 MOVE.W      $AA, D0
11117A MOVE.W      D7, A0
11117C MOVE.W      D7, (A7)
11117E MOVE.W      D0, (A0)+
111180 MOVE.W      D7, -(A7)

```

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```

MOVE.W    $5555,D0
MOVE.W    $AAAAA,D0
MOVE.L    #$AA,D0
MOVE.L    D0,A0
MOVE.L    D0,(A0)
MOVE.L    D0,(A0)+
MOVE.L    D0,-(A0)
MOVE.L    $1000,D0
MOVE.L    $10000,D0

```

```

* -----
» -----
* MOVEA.W
* -----
» -----

```

```

MOVEA.W    D7,A0
MOVEA.W    (A0),A7
MOVEA.W    (A0)+,A7
MOVEA.W    -(A7),A0
MOVEA.W    $AAAA,A0
MOVEA.W    $55555,A0
MOVEA.L    D0,A0
MOVEA.L    D7,A0
MOVEA.L    (A7),A0
MOVEA.L    (A0)+,A7
MOVEA.L    -(A7),A0
MOVEA.L    $FFAA,A7
MOVEA.L    $FFAA5,A0

```

```

* -----
» -----
* NOP, RTS, ILLEGAL
* -----
» -----
NOP

```

```

RTS

ILLEGAL

```

```

* -----
» -----
* LEA
* -----
» -----
LEA        (A7),A0
LEA        $FFAA,A0
LEA        $AA551,A7

```

```

111182 MOVE.W    $5555, D0
111186 MOVE.W    $AAAAA, D0
11118C MOVE.L    #$AA, D0
111192 MOVEA.L    D0, A0
111194 MOVE.L    D0, (A0)
111196 MOVE.L    D0, (A0)+
111198 MOVE.L    D0, -(A0)
11119A MOVE.L    $1000, D0
11119E MOVE.L    $10000, D0

```

```

1111A4 MOVEA.W    D7, A0
1111A6 MOVEA.W    (A0), A7
1111A8 MOVEA.W    (A0)+, A7
1111AA MOVEA.W    -(A7), A0
1111AC MOVEA.W    $AAAA, A0
1111B2 MOVEA.W    $55555, A0
1111B8 MOVEA.L    D0, A0
1111BA MOVEA.L    D7, A0
1111BC MOVEA.L    (A7), A0
1111BE MOVEA.L    (A0)+, A7
1111C0 MOVEA.L    -(A7), A0
1111C2 MOVEA.L    $FFAA, A7
1111C8 MOVEA.L    $FFAA5, A0
1111CE RESET
1111D0 RESET
1111D2 RESET

```

```

1111D4 RESET
1111D6 RESET

1111D8 ORI.B    #$FFAA, D0
1111DC RESET
1111DE ORI.B    #$A551, A2
1111E2 RESET
1111E4 RESET
1111E6 RESET
1111E8 RESET

```

```

1111EA RESET

```

```

1111EC ORI.B    #$AAFF, D0

```

```

1111F0 RESET

```

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```

* -----
» -----
* NEG
* -----
» -----
    NEG      D0
    NEG      (A6)
    NEG      (A0)+
    NEG      -(A1)
    NEG      $AAFF
    NEG      $55FAA

* -----
» -----
* JSR
* -----
» -----
    JSR      (A6)
    JSR      $AAFF
    JSR      $55FAA

* -----
» -----
* MOVEM
* -----
» -----

* -----
» -----
* SUBQ.x
* -----
» -----
    SUBQ.B   #1,D0
    SUBQ.B   #3,(A7)
    SUBQ.B   #4,(A0)+
    SUBQ.B   #5,-(A0)
    SUBQ.B   #6,$AAFF
    SUBQ.B   #7,$AFAF5

    SUBQ.W   #1,D0
    SUBQ.W   #3,(A7)
    SUBQ.W   #4,(A0)+
    SUBQ.W   #5,-(A0)
    SUBQ.W   #6,$AAFF
    SUBQ.W   #7,$AFAF5
    SUBQ.L   #1,D0
    SUBQ.L   #3,(A7)
    SUBQ.L   #4,(A0)+
    SUBQ.L   #5,-(A0)
    SUBQ.L   #6,$AAFF
    SUBQ.L   #7,$AFAF5

```

```

1111F2 ORI.B  #$5FAA, D5
1111F6 RESET
1111F8 RESET

```

```

1111FA ORI.B  #$AAFF, D0

```

```

1111FE RESET
111200 ORI.B  #$5FAA, D5

```

```

111204 SUBQ.B  #1, D0
111206 SUBQ.B  #3, (A7)
111208 SUBQ.B  #4, (A0)+
11120A SUBQ.B  #5, -(A0)
11120C SUBQ.B  #6, $AAFF
111212 SUBQ.B  #7, $AFAF5

```

```

111218 SUBQ.W  #1, D0
11121A SUBQ.W  #3, (A7)
11121C SUBQ.W  #4, (A0)+
11121E SUBQ.W  #5, -(A0)
111220 SUBQ.W  #6, $AAFF
111226 SUBQ.W  #7, $AFAF5
11122C SUBQ.L  #1, D0
11122E SUBQ.L  #3, (A7)
111230 SUBQ.L  #4, (A0)+
111232 SUBQ.L  #5, -(A0)
111234 SUBQ.L  #6, $AAFF
11123A SUBQ.L  #7, $AFAF5

```

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(continued)

```

* -----
» -----
* DIVS
* -----
» -----
    DIVS      D0,D1
    DIVS      (A1)+,D1
    DIVS      -(A2),D2
    DIVS      #01,D1
    DIVS      $AAFF,D1
    DIVS      $FFAA5,D2
* -----
» -----
* OR
* -----
» -----
    OR        D0,D1
    OR        (A0),D0
    OR        (A0)+,D7
    OR        -(A7),D0
    OR        #02,D1
* -----
» -----
* SUB
* -----
» -----
    SUB       D0,D1
    SUB       A0,D0
    SUB       (A0),D0
    SUB       (A0)+,D0
    SUB       -(A7),D1
    SUB       #02,D1
    SUB       $AAFF,D0
    SUB       $AFAF5,D1
* -----
» -----
* CMP
* -----
» -----
    CMP       D0,D1
    CMP       A0,D0
    CMP       (A0),D0
    CMP       (A0)+,D0
    CMP       -(A7),D1
    CMP       #02,D1
    CMP       $AAFF,D0
    CMP       $AFAF5,D1
* -----
» -----
* EOR
* -----

```

```

111240 DIVS      D0, D1
111242 DIVS      (A1)+, D1
111244 DIVS      -(A2), D2
111246 DIVS      #1, D1
11124A DIVS      $AAFF, D1
111250 DIVS      $FFAA5, D2

```

```

111256 OR.W      D0, D1
111258 OR.W      (A0), D0
11125A OR.W      (A0)+, D7
11125C OR.W      -(A7), D0

```

```

11125E OR.W      #2, D1

```

```

111262 SUB.W     D0, D1
111264 SUB.W     A0, D0
111266 SUB.W     (A0), D0
111268 SUB.W     (A0)+, D0
11126A SUB.W     -(A7), D1
11126C SUBQ.W    #2, D1
11126E SUB.W     $AAFF, D0
111274 SUB.W     $AFAF5, D1

```

```

11127A CMP.W     D0, D1
11127C CMP.W     A0, D0
11127E CMP.W     (A0), D0
111280 CMP.W     (A0)+, D0
111282 CMP.W     -(A7), D1
111284 CMP.W     #2, D1
111288 CMP.W     $AAFF, D0
11128E CMP.W     $AFAF5, D1

```

(continued)

Beyond Compare v4.2.10

(continued)

[illegible]

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(continued)

```
* -----
» -----
* ADD
* -----
» -----
    ADD      D0,D1
    ADD      D0,A0
    ADD      (A0),D0
    ADD      (A0)+,D0
    ADD      -(A7),D1
    ADD      #02,D1
    ADD      $AAFF,D0
    ADD      $AFAF5,D1
```

```
* -----
» -----
* ADDA
* -----
» -----
    ADDA     D0,A0
    ADDA     D0,A0
    ADDA     (A0),A0
    ADDA     (A0)+,A0
    ADDA     -(A7),A1
    ADDA     #02,A1
    ADDA     $AAFF,A0
    ADDA     $AFAF5,A7
```

```
* -----
» -----
* ASR
* -----
» -----
    ASR      (A0)
    ASR      (A7)+
    ASR      -(A0)
    ASR      $AFAF
    ASR      $FFAA550
```

```
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyy
```

```
yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyOu
```

```
□MOVE.L D4,D5□ADD.B D0,D1□Output.txt□
```

```
1A001A00□□Config.cfg□0011111200111670Z1112BEÿ
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
» yyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyyy
```


(continued)

[illegible]

ASL	(A0)
ASL	(A7)+
ASL	-(A0)
ASL	\$AFAF
ASL	\$FFAA550

* LSR

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(continued)

```
* -----
» -----
    LSR      (A0)
    LSR      (A7)+
    LSR      -(A0)
    LSR      $AFAF
    LSR      $FFAA550
* -----
» -----
* LSL
* -----
» -----
    LSL      (A0)
    LSL      (A7)+
    LSL      -(A0)
    LSL      $AFAF
    LSL      $FFAA550
* -----
» -----
* ROL
* -----
» -----
    ROL      (A0)
    ROL      (A7)+
    ROL      -(A0)
    ROL      $AFAF
    ROL      $FFAA550
* -----
» -----
* ROR
* -----
» -----
    ROR      (A0)
    ROR      (A7)+
    ROR      -(A0)
    ROR      $AFAF
    ROR      $FFAA550
* -----
» -----
* BRUTE-FORCE VERIFICATION
* -----
» -----
    ; D0 to all other data registers
    ADD      D0,D0
    ADD      D0,D1
    ADD      D0,D2
    ADD      D0,D3
    ADD      D0,D4
    ADD      D0,D5
    ADD      D0,D6
    ADD      D0,D7
    ; D1 to all other data registers
```

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(continued)

```
ADD      D1,D0
ADD      D1,D1
ADD      D1,D2
ADD      D1,D3
ADD      D1,D4
ADD      D1,D5
ADD      D1,D6
ADD      D1,D7
      ; D2 to all other data registers
ADD      D2,D0
ADD      D2,D1
ADD      D2,D2
ADD      D2,D3
ADD      D2,D4
ADD      D2,D5
ADD      D2,D6
ADD      D2,D7
      ; D3 to all other data registers
ADD      D3,D0
ADD      D3,D1
ADD      D3,D2
ADD      D3,D3
ADD      D3,D4
ADD      D3,D5
ADD      D3,D6
ADD      D3,D7
      ; D4 to all other data registers
ADD      D4,D0
ADD      D4,D1
ADD      D4,D2
ADD      D4,D3
ADD      D4,D4
ADD      D4,D5
ADD      D4,D6
ADD      D4,D7
      ; D5 to all other data registers
ADD      D5,D0
ADD      D5,D1
ADD      D5,D2
ADD      D5,D3
ADD      D5,D4
ADD      D5,D5
ADD      D5,D6
ADD      D5,D7
      ; D6 to all other data registers
ADD      D6,D0
ADD      D6,D1
ADD      D6,D2
ADD      D6,D3
ADD      D6,D4
ADD      D6,D5
ADD      D6,D6
```

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```
ADD      D6,D7
; D7 to all other data registers
ADD      D7,D0
ADD      D7,D1
ADD      D7,D2
ADD      D7,D3
ADD      D7,D4
ADD      D7,D5
ADD      D7,D6
ADD      D7,D7
; D0 to all other address registers
ADD      D0,A0
ADD      D0,A1
ADD      D0,A2
ADD      D0,A3
ADD      D0,A4
ADD      D0,A5
ADD      D0,A6
ADD      D0,A7
; D1 to all other address registers
ADD      D1,A0
ADD      D1,A1
ADD      D1,A2
ADD      D1,A3
ADD      D1,A4
ADD      D1,A5
ADD      D1,A6
ADD      D1,A7
; D2 to all other address registers
»
ADD      D2,A0
ADD      D2,A1
ADD      D2,A2
ADD      D2,A3
ADD      D2,A4
ADD      D2,A5
ADD      D2,A6
ADD      D2,A7
; D3 to all other address registers
ADD      D3,A0
ADD      D3,A1
ADD      D3,A2
ADD      D3,A3
ADD      D3,A4
ADD      D3,A5
ADD      D3,A6
ADD      D3,A7
; D4 to all other address registers
ADD      D4,A0
ADD      D4,A1
ADD      D4,A2
```

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(continued)

```
ADD      D4,A3
ADD      D4,A4
ADD      D4,A5
ADD      D4,A6
ADD      D4,A7
      ; D5 to all other address registers
ADD      D5,A0
ADD      D5,A1
ADD      D5,A2
ADD      D5,A3
ADD      D5,A4
ADD      D5,A5
ADD      D5,A6
ADD      D5,A7
      ; D6 to all other address registers
ADD      D6,A0
ADD      D6,A1
ADD      D6,A2
ADD      D6,A3
ADD      D6,A4
ADD      D6,A5
ADD      D6,A6
ADD      D6,A7
      ; D7 to all other address registers
ADD      D7,A0
ADD      D7,A1
ADD      D7,A2
ADD      D7,A3
ADD      D7,A4
ADD      D7,A5
ADD      D7,A6
ADD      D7,A7

      ; values from all address registers to
»  A0
      ADD      (A0),A0
      ADD      (A1),A0
      ADD      (A2),A0
      ADD      (A3),A0
      ADD      (A4),A0
      ADD      (A5),A0
      ADD      (A6),A0
      ADD      (A7),A0
      ; values from all address registers to
»  A1
      ADD      (A0),A1
      ADD      (A1),A1
      ADD      (A2),A1
      ADD      (A3),A1
      ADD      (A4),A1
      ADD      (A5),A1
      ADD      (A6),A1
```

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(continued)

```
ADD      (A7),A1

; values from all address registers to
» A2
ADD      (A0),A2
ADD      (A1),A2
ADD      (A2),A2
ADD      (A3),A2
ADD      (A4),A2
ADD      (A5),A2
ADD      (A6),A2
ADD      (A7),A2

; values from all address registers to
» A3
ADD      (A0),A3
ADD      (A1),A3
ADD      (A2),A3
ADD      (A3),A3
ADD      (A4),A3
ADD      (A5),A3
ADD      (A6),A3
ADD      (A7),A3

; values from all address registers
» to A4
ADD      (A0),A4
ADD      (A1),A4
ADD      (A2),A4
ADD      (A3),A4
ADD      (A4),A4
ADD      (A5),A4
ADD      (A6),A4
ADD      (A7),A4

; values from all address registers to
» A5
ADD      (A0),A5
ADD      (A1),A5
ADD      (A2),A5
ADD      (A3),A5
ADD      (A4),A5
ADD      (A5),A5
ADD      (A6),A5
ADD      (A7),A5

; values from all address registers to
» A6
ADD      (A0),A6
ADD      (A1),A6
ADD      (A2),A6
ADD      (A3),A6
ADD      (A4),A6
```

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(continued)

```
ADD      (A5),A6
ADD      (A6),A6
ADD      (A7),A6
```

```
      ; values from all address registers to
```

```
» A7
```

```
ADD      (A0),A7
ADD      (A1),A7
ADD      (A2),A7
ADD      (A3),A7
ADD      (A4),A7
ADD      (A5),A7
ADD      (A6),A7
ADD      (A7),A7
```

```
      ; post-increment from all address regi
» sters to A0
```

```
ADD      (A0)+,A0
ADD      (A1)+,A0
ADD      (A2)+,A0
ADD      (A3)+,A0
ADD      (A4)+,A0
ADD      (A5)+,A0
ADD      (A6)+,A0
ADD      (A7)+,A0
```

```
      ; post-increment from all address regi
» sters to A1
```

```
ADD      (A0)+,A1
ADD      (A1)+,A1
ADD      (A2)+,A1
ADD      (A3)+,A1
ADD      (A4)+,A1
ADD      (A5)+,A1
ADD      (A6)+,A1
ADD      (A7)+,A1
```

```
      ; post-increment from all address regi
» sters to A2
```

```
ADD      (A0)+,A2
ADD      (A1)+,A2
ADD      (A2)+,A2
ADD      (A3)+,A2
ADD      (A4)+,A2
ADD      (A5)+,A2
ADD      (A6)+,A2
ADD      (A7)+,A2
```

```
      ; post-increment from all address regi
» sters to A3
```

```
ADD      (A0)+,A3
ADD      (A1)+,A3
```


Left file: D:\Source\github\CSS422_Hardware\Disassembler\UnitTests\Test_002.X68

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(continued)

ADD (A2)+,A3

ADD (A3)+,A3

ADD (A4)+,A3

ADD (A5)+,A3

ADD (A6)+,A3

ADD (A7)+,A3

; post-increment from all address regi

» sters to A4

ADD (A0)+,A4

ADD (A1)+,A4

ADD (A2)+,A4

ADD (A3)+,A4

ADD (A4)+,A4

ADD (A5)+,A4

ADD (A6)+,A4

ADD (A7)+,A4

; post-increment from all address regi

» sters to A5

ADD (A0)+,A5

ADD (A1)+,A5

ADD (A2)+,A5

ADD (A3)+,A5

ADD (A4)+,A5

ADD (A5)+,A5

ADD (A6)+,A5

ADD (A7)+,A5

; post-increment from all address regi

» sters to A6

ADD (A0)+,A6

ADD (A1)+,A6

ADD (A2)+,A6

ADD (A3)+,A6

ADD (A4)+,A6

ADD (A5)+,A6

ADD (A6)+,A6

ADD (A7)+,A6

; post-increment from all address reg

» isters to A7

ADD (A0)+,A7

ADD (A1)+,A7

ADD (A2)+,A7

ADD (A3)+,A7

ADD (A4)+,A7

ADD (A5)+,A7

ADD (A6)+,A7

ADD (A7)+,A7

; pre-decrement from all address regis

Left file: D:\Source\github\CSS422_Hardware\Disassembler\UnitTests\Test_002.X68

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(continued)

» ters to A0

```
ADD      -(A0),A0
ADD      -(A1),A0
ADD      -(A2),A0
ADD      -(A3),A0
ADD      -(A4),A0
ADD      -(A5),A0
ADD      -(A6),A0
ADD      -(A7),A0
```

; pre-decrement from all address regis

» ters to A1

```
ADD      -(A0),A1
ADD      -(A1),A1
ADD      -(A2),A1
ADD      -(A3),A1
ADD      -(A4),A1
ADD      -(A5),A1
ADD      -(A6),A1
ADD      -(A7),A1
```

; pre-decrement from all address regis

» ters to A2

```
ADD      -(A0),A2
ADD      -(A1),A2
ADD      -(A2),A2
ADD      -(A3),A2
ADD      -(A4),A2
ADD      -(A5),A2
ADD      -(A6),A2
ADD      -(A7),A2
```

; pre-decrement from all address regis

» ters to A3

```
ADD      -(A0),A3
ADD      -(A1),A3
ADD      -(A2),A3
ADD      -(A3),A3
ADD      -(A4),A3
ADD      -(A5),A3
ADD      -(A6),A3
ADD      -(A7),A3
```

; pre-decrement from all address regis

» ters to A4

```
ADD      -(A0),A4
ADD      -(A1),A4
ADD      -(A2),A4
ADD      -(A3),A4
ADD      -(A4),A4
ADD      -(A5),A4
ADD      -(A6),A4
```

Left file: D:\Source\github\CSS422_Hardware\Disassembler\UnitTests\Test_002.X68

Right file: D:\Source\github\CSS422_Hardware\Disassembler\Output.txt

(continued)

```
ADD      -(A7),A4

; pre-decrement from all address regis
» ters to A5
ADD      -(A0),A5
ADD      -(A1),A5
ADD      -(A2),A5
ADD      -(A3),A5
ADD      -(A4),A5
ADD      -(A5),A5
ADD      -(A6),A5
ADD      -(A7),A5

; pre-decrement from all address regis
» ters to A6
ADD      -(A0),A6
ADD      -(A1),A6
ADD      -(A2),A6
ADD      -(A3),A6
ADD      -(A4),A6
ADD      -(A5),A6
ADD      -(A6),A6
ADD      -(A7),A6

; pre-decrement from all address regis
» ters to A7
ADD      -(A0),A7
ADD      -(A1),A7
ADD      -(A2),A7
ADD      -(A3),A7
ADD      -(A4),A7
ADD      -(A5),A7
ADD      -(A6),A7
ADD      -(A7),A7

; immediate to all data registers
ADD      #01,D0
ADD      #01,D1
ADD      #01,D2
ADD      #01,D3
ADD      #01,D4
ADD      #01,D5
ADD      #01,D6
ADD      #01,D7
; immediate to all address register
ADD      #01,A0
ADD      #01,A1
ADD      #01,A2
ADD      #01,A3
ADD      #01,A4
ADD      #01,A5
ADD      #01,A6
```

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(continued)

```
    ADD        #01,A7
; immediate to all address register va
» lues
    ADD        #01,(A0)
    ADD        #01,(A1)
    ADD        #01,(A2)
    ADD        #01,(A3)
    ADD        #01,(A4)
    ADD        #01,(A5)
    ADD        #01,(A6)
    ADD        #01,(A7)
; immediate to all address register wi
» th post increment
    ADD        #01,(A0)+
    ADD        #01,(A1)+
    ADD        #01,(A2)+
    ADD        #01,(A3)+
    ADD        #01,(A4)+
    ADD        #01,(A5)+
    ADD        #01,(A6)+
    ADD        #01,(A7)+
; immediate to all address register wi
» th pre-decrement
    ADD        #01,-(A0)
    ADD        #01,-(A1)
    ADD        #01,-(A2)
    ADD        #01,-(A3)
    ADD        #01,-(A4)
    ADD        #01,-(A5)
    ADD        #01,-(A6)
    ADD        #01,-(A7)
; absolute short to all data registers
    ADD        $01,D0
    ADD        $01,D1
    ADD        $01,D2
    ADD        $01,D3
    ADD        $01,D4
    ADD        $01,D5
    ADD        $01,D6
    ADD        $01,D7
; absolute long to all data registers
    ADD        $0A05,A0
    ADD        $0A05,A1
    ADD        $0A05,A2
    ADD        $0A05,A3
    ADD        $0A05,A4
    ADD        $0A05,A5
    ADD        $0A05,A6
    ADD        $0A05,A7
*~Font name~Courier New~
*~Font size~10~
*~Tab type~1~
```

Left file: D:\Source\github\CSS422_Hardware\Disassembler\UnitTests\Test_002.X68

Right file: D:\Source\github\CSS422_Hardware\Disassembler\Output.txt

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