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Minor Project Report

on

Implementation Of Logical Built In Self Test(BIST)

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SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled " **FPGA Implementation of reinforced technique for logical BIST** " is a bonafide work carried out by the student team of "**Hema Kongi [01FE19BEC251] , Vaishnavi Chillal [01FE19BEC264] , Daneshwari Hurali [01FE19BEC270] , Prathamesh Rane [01FE19BEC294]** ". The project report has been approved as it satisfies the requirements with respect to the Minor project work prescribed by the university curriculum for BE (VI semester) in School of Electronics and Communication Engineering of KLE Technological University for the academic year 2021-22.

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-The project team 2

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ABSTRACT

The growth of integrated circuit technology has been accelerated by Very Large Scale Integration (VLSI). It has expanded the intricacy of the circuits while reducing their size and cost. In VLSI systems, positive advances have led to significant performance. However,there are possibilities challenges that could prevent the successful usage and development of future Very Large Scale Integration(VLSI) technology one of the issue is as the size of integration develops, circuit testing becomes increasingly complicated. Because of the device's high price,because of the high number of transistors and limited access to input/output that characterise VLSI circuits,the traditional testing methods are frequently used.VLSI circuits are ineffective and insufficient.Primitive polynomials are important in PN sequence design generators. The longest PRPG is generated by the original polynomial-based LFSR. Built-In Self-Test the design technique which allows the circuit to test itself.BIST is popular as the cost-effective circuit testing tool.such as test reuse and test quality Virtually all ICs are tested using two different methodologies: ATPG (Automated Test Pattern Generation) using compression and logic Self-Test Built-In (BIST). Test engineers ensure the accurate manufacture of digital circuitry.

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Chapter 1

Introduction

BIST is the technique of designing hardware and software features into the IC's to allow them to perform self-testing on their own circuits, reducing the reliance on external Automated Test Equipment (ATE)[6].

BIST has following blocks:

- Test pattern Generator (TPG):TPG is a circuit that produces the test patterns/sequence which are given as a inputs to the circuit.
- Circuit under test (CUT):It is the combinational or sequential circuit which is under the test.
- The Response Analyzer:It is a comparator which compares the output from the circuit against the stored response.

1.1 Motivation

Built in self-test(BIST) approaches are the series of techniques that allow for high fault coverage and fast testing.Reduces the dependency on costly external testing tools.As a result, they offer an appealing solution to the VLSI device testing dilemma.Test engineers have been working for decades for the reduction of number of test vectors required for digital circuit testing.So in this project we have designed a logical BIST in which the test patterns are reduced using hamming distance.The aim of this project is to decrease the power with high fault coverage. There are two testing methods namely:Automatic Test Pattern Generator(ATPG) and BIST[1].

1.2 Objectives

In this proposed technique the Fibonacci Linear Feedback Shift Register(LFSR) is used as the test pattern generator.The no.of test sequences are reduced using hamming distance.These reduced test patterns are given as input to Circuit-Under-Test(CUT).The output of CUT is compared with signatures stored in ROM based on this BIST confirms whether the CUT is faulty on not[5].

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	Logic BIST	ATPG
Test Quality	High quality	High quality
Design Impact	High	Low
Test environment	Minimal interface; retest in system and burn-in	Needs a tester
Design type	Design that needs retest in system	Any digital circuit chip
Test application time	Short if design is not pseudorandom resistant	Depends on the number of pattern sets

Figure 1.1: Difference between ATPG and BIST

1.3 Literature survey

- C. Baek, I. Kim, J. Kim, Y. Kim, H. B. Min and J. Lee, "A Dynamic Scan Chain Reordering for Low-Power VLSI Testing"
  This study discusses a technique for reducing power consumption during scan chain testing shift operations by dynamically reordering scan chains[7].

- "Near optimal machine learning based random test generation," 2010 East-West Design Test Symposium (EWDTS), pp. 420-424, doi: 10.1109/EWDTS.2010.5742082.newline, N. Shakeri, N. Nemati, M. N. Ahmadabadi, and Z. Navabi In this paper, a machine learning-based solution for improving random test generation approaches is provided[6].

- "Design for testability—A survey," IEEE Proceedings, vol. 71, no. 1, pp. 98-112, Jan. 1983, doi: 10.1109/PROC.1983.12531. Machine Learning techniques can be used to guide the development of tests for simulation-based verification[8].

- "LFSR-Reseeding Scheme Achieving Low-Power Dissipation During Test," by J. Lee and N. A. Touba, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 2, pp. 396-401, February 2007, doi: 10.1109/TCAD.2006.882509. The proposed method reduces test power and, in most circumstances, compresses test data better than LFSR reseeding alone[4].

- Efficient BIST TPG design and test set compaction for delay testing via input re-," Proceedings International Conference on Computer Design. VLSI in Com- and Processors (Cat. No.98CB36273), 32-39, doi: 10.1109/ICCD.1998.727020. This article covers the fundamentals of testability design[2].

- Charalambos, C-Ioannides, and Kerstin I. Eder. "A review of coverage-directed test generation using machine learning." 17.1 (2012): 1-21 in ACM transactions on the design automation of electronic systems (TODAES).newline BIST TPGs for delay faults have been designed using the input reduction technique described.

1.4 Problem statement

"FPGA implementation of reinforced technique for Logical BIST"

The capacity to test internal circuits with no direct connections to external pins, and thus inaccessible by external automated test equipment, is the primary goal of LBIST. Another benefit is the possibility to activate an integrated circuit's LBIST while performing a built-in or power-on self test on the finished product.

1.5 Organization of the report

- Chapter2: In this section we have given the description of the model which is intended to give overall function of the system through block diagram and other various solutions and their functionalities[7].
- Chapter3: In this section we have explained the process of program through algorithms and flowchart.
- Chapter4: In this section we have understood the how the our model or system works.
- Chapter5: Here we have concluded our project with future scope and its application in social context.

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Chapter 2

System design

2.1 The Functional Block Diagram

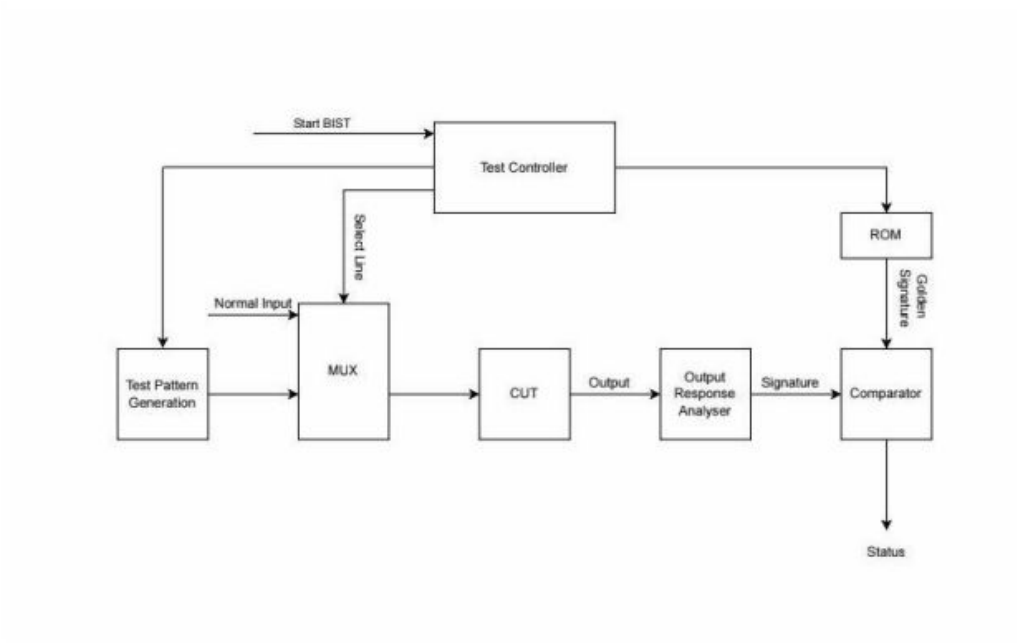

Figure 2.1: The Functional Block diagram

Th vectors from test pattern generator are given as input to the CUT.The output of CUT is compared with golden signature present in ROM if both the values are same then the circuit is not faulty else the circuit is faulty.A linear feedback shift register (LFSR) creates test patterns, while a multiple input shift register (MISR) compacts test replies in BIST. The average and/or peak power dissipation of test vectors applied to a circuit under test at nominal operating frequency may be higher than in normal mode.

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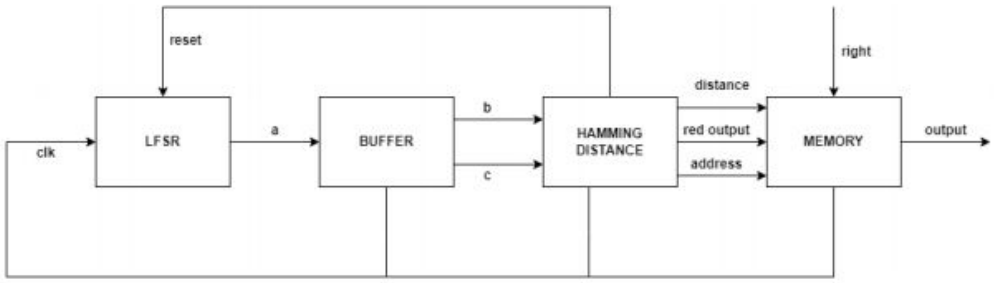

Figure 2.2: The Test Pattern Generator

Test Pattern Generator generates the test patterns.In traditional BIST architecture, test pattern generators (TPGs) with linear feedback shift registers (LFSRs) are used. The main disadvantage of these architecture is that the LFSR generates pseudorandom patterns, which result in excessive switching activities in the CUT.

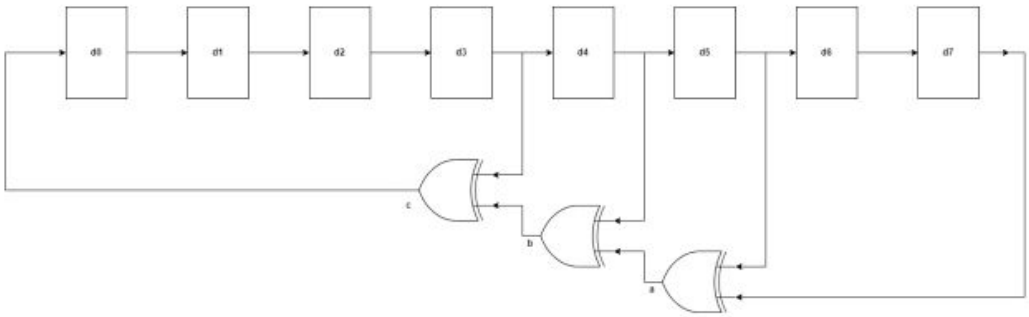

Figure 2.3: LFSR

Linear Feedback Shift Register- It produces the pseudo random test patterns for every positive edge of clock.The Test Pattern Generator (TPG) generates test patterns that are fed into the CUT as inputs. For this purpose, pseudo random number generators (PRNGs) based on the Linear Feedback Shift Register (LFSR) architecture are commonly utilised.

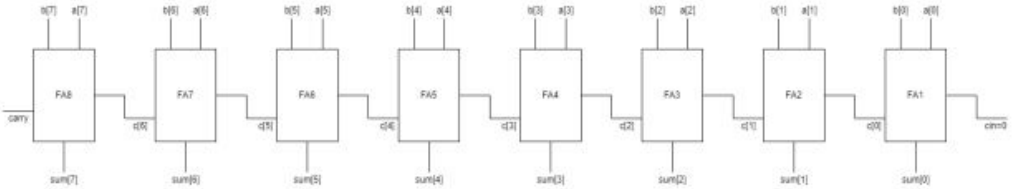

Figure 2.4: Ripple carry adder

The model that will be verified is referred to as the CUT. We have considered Ripple carry adder as our circuit under test.

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Chapter 3

Implementation details

3.1 Specifications and system architecture

- 8-bit Fibonacci LFSR
- Fibonacci LFSR is a shift register whose input bits are the linear function of its previous state.

$$x^7 + x^5 + x^4 + x^3 + 1$$

- Test patterns whose hamming distances are either 0,1 or 2 are used as inputs.
- For binary sequences x and y the hamming distance is equal to the number of ones in

$$x \oplus y$$

3.2 Algorithm

An algorithm is a set of instructions that tells a computer how to turn a set of world facts into useful information.

- Step 1)TPG consists of 4 blocks, LFSR, Buffer, Hamming distance, Memory.
- We have taken clk, reset, wright, address, distance as inputs and regout, output as outputs.
- 1) LFSR- reset and clk are the inputs and a is the output here the test patterns are generated and get stored in a.
- 2) Buffer- The present output of LFSR is the input, which gives previous and the present outputs(b,c respectively) of LFSR as output.
- 3) Hamming distance: Buffer outputs(b,c) are taken as inputs, here the 2 inputs are xor'd and calculated the distance between them(hamming distance), and we have taken 0,1,2 as threshold values. The output of this block is get stored as reduced output
- 4) Memory: output of hamming distance is get stored in the memory location.[4]
- Step 2)Circuit-Under-Test

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- 1) The CUT is the test circuit which is placed for testing.
- 2) It could be sequential, combinatorial, or memory-based. Initially, a fully functional circuit is installed in the chip socket, which is off-chip from the parent chip and houses the LFSR, MISR, Signature register, and BIST controller.
- 3) Once there is a need of testing the required circuitry is connected to the parent chip and is run.
- 4)Here,we are using ripple carry adder as CUT[2].
- Step 3)Multiple Input Shift Register
- 1) A multiple-output digital system requires a multiple-input signature register for testable design.
- 2)This register speeds up the testing process by combining various data streams into a single signature[3].

3.3 Flowchart

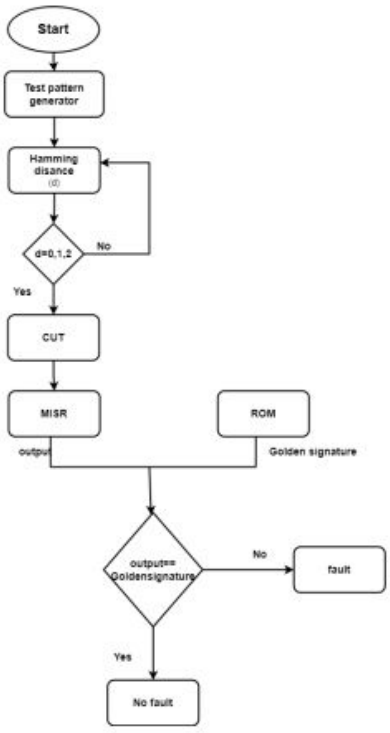

Figure 3.1: Flow chart

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Chapter 4

Results and discussions

4.1 Result Analysis

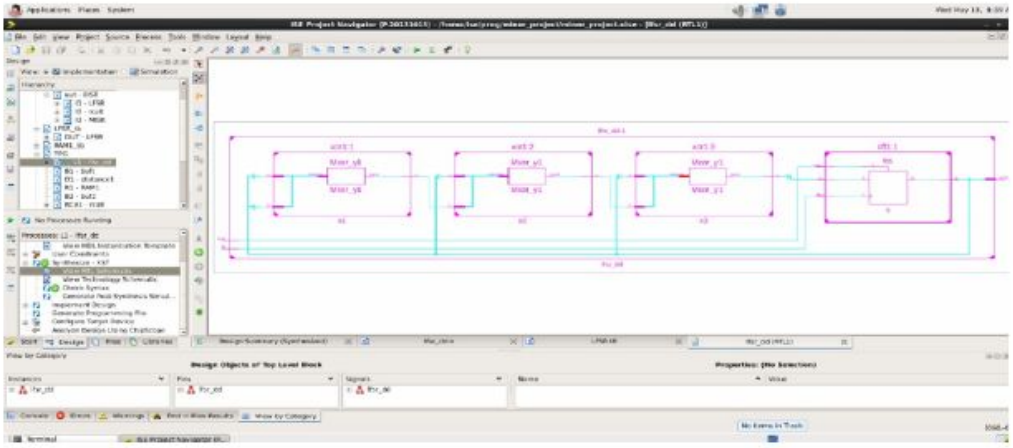

Figure 4.1: LFSR

The figure 4.1 indicates the rtl design of LFSR.Register-transfer level (RTL) is a design abstraction for modelling a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers and the logical operations performed on those signals in digital circuit design.

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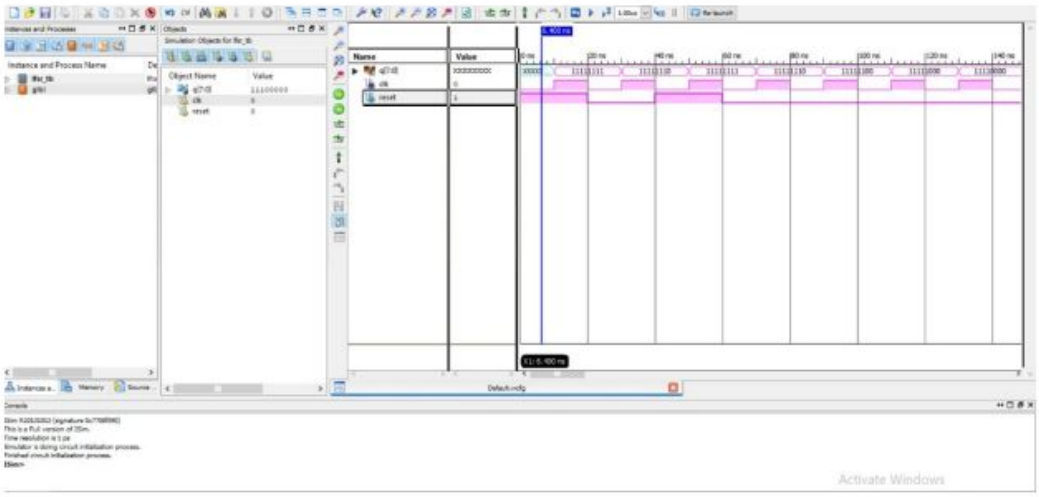
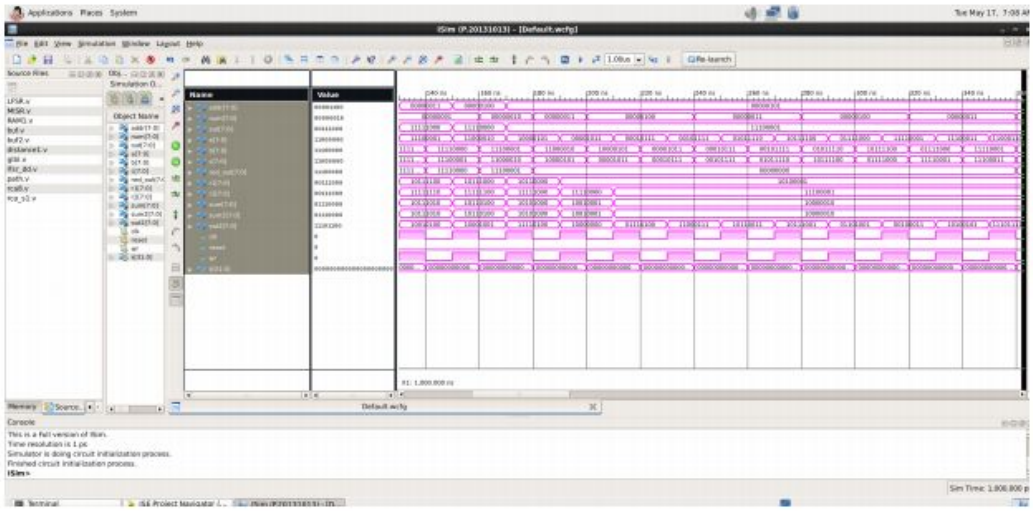


Figure 4.2: Waveform of lfsr

Above figure 4.2 shows the waveform of LFSR.This is used as a pseudo random test pattern generator which generates pseudo random pattern generators.Those patterns are fed as inputs to the circuit under test.



The above 4.3 shows the waveform of Test Pattern Generator before Hamming Distance.

Figure 4.3: TPG

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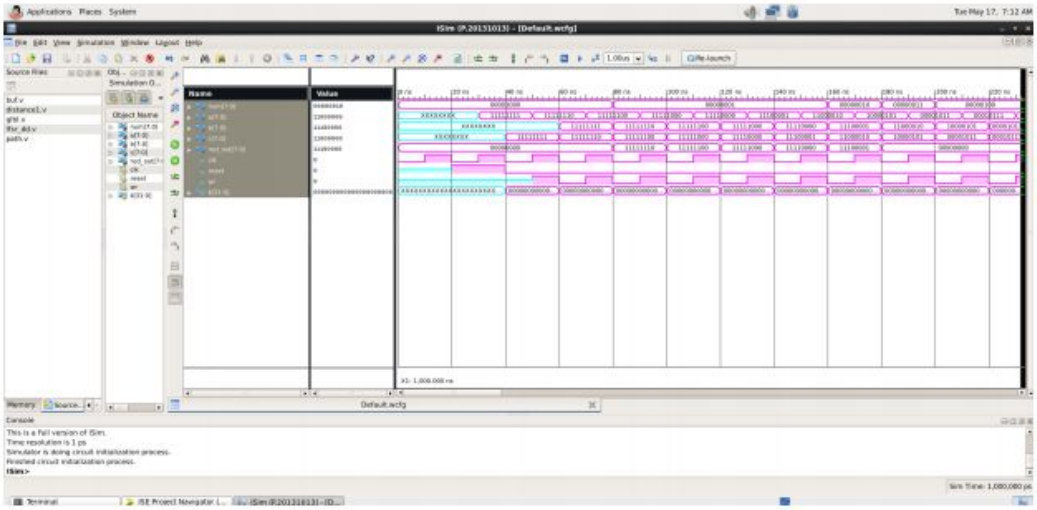

Figure 4.4: Waveform of TPG after Hamming Distance

The above figure 4.4 shows the waveform og TPG.The number of locations at which the matching symbols differ is the Hamming distance between two equal-length strings of symbols. The clock cycle and test patterns are reduced using Hamming distance. The Hamming distance between binary strings a and b is equal to the number of ones in a xor b. Symbols could include letters, bits, or decimal digits, among other things. For instance, consider the Hamming distance between:0000 and 1111 equals 4.

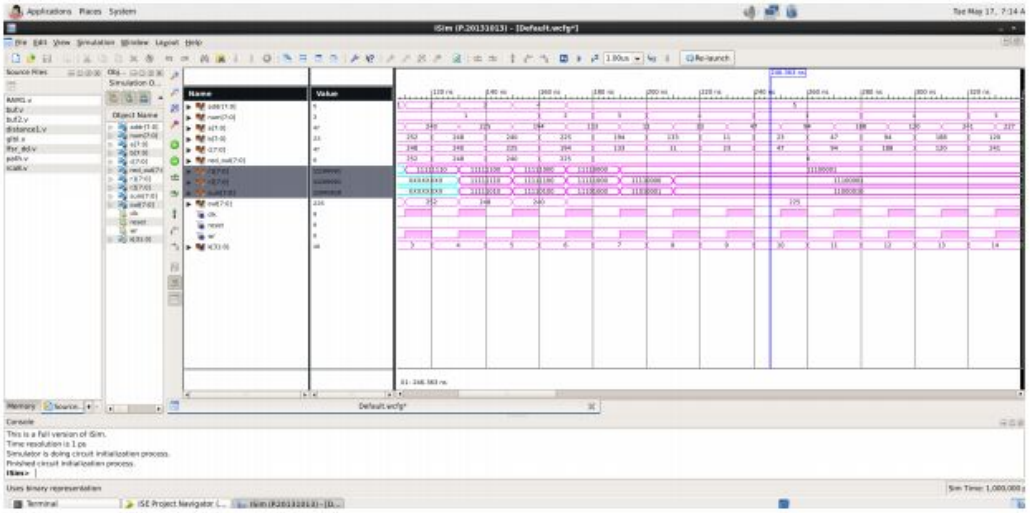

Figure 4.5: Waveform of Ripple Carry Adder

The above figure 4.5 shows the waveform of cut after applying hamming distance to the test pattern generator which are fed as inputs to the MISR.

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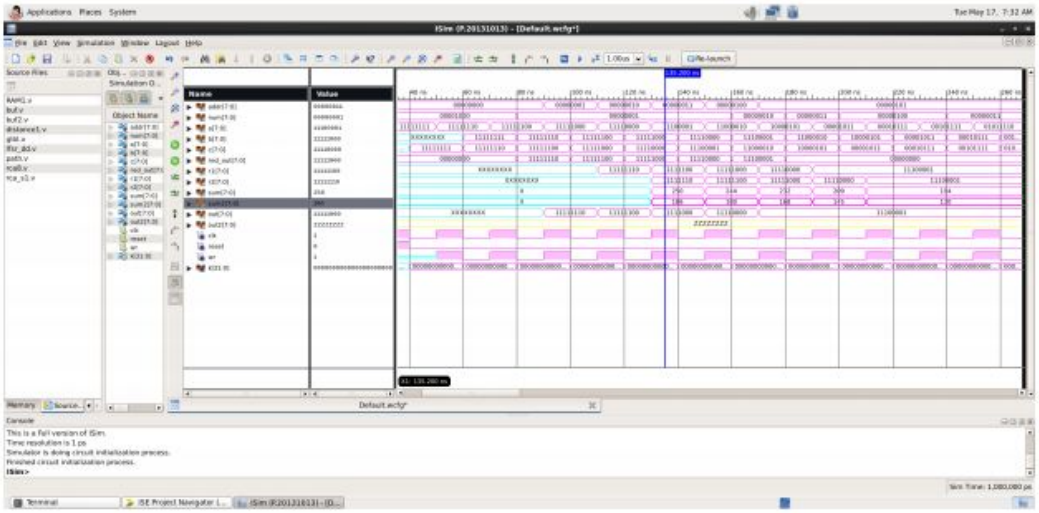

Figure 4.6: Waveform of Stuck at fault

The figure 4.6 shows the waveform of Stuck at fault.When a line is permanently connected to Vdd or ground, it causes a defective output. Any gate can use this line as an input or output. This fault can also be one or more stuck at faults.

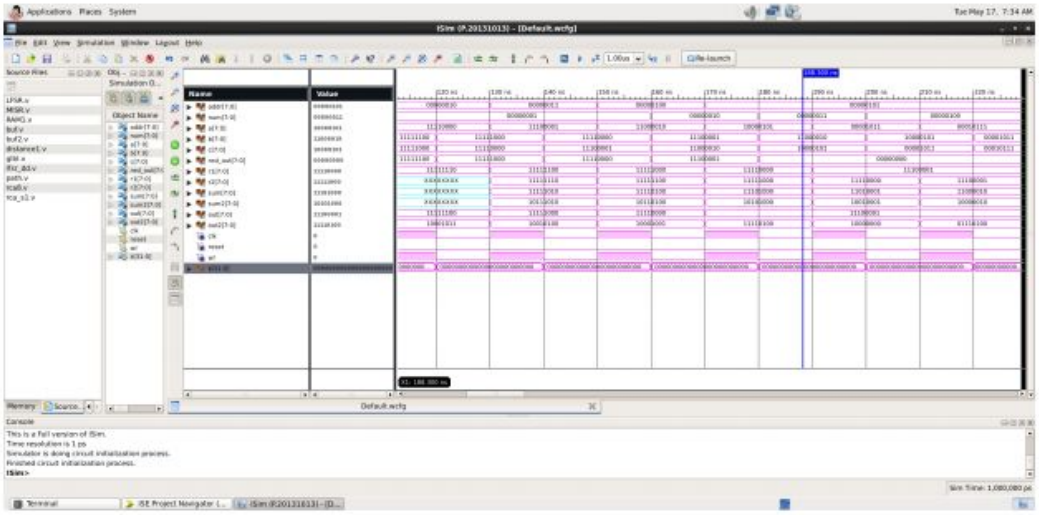

Figure 4.7: Waveform of MISR

The figure 4.7 shows the waveform of MISR.MISR is a popular output response analyzer because it is a cheaper alternative to n-parallel LFSRs. MISRs shorten the testing process by combining many bits streams into a single signature. To increase the fault coverage of IC testing, a Reconfigurable LFSR can be employed as a test pattern generator as well as a response compactor inside Logic BIST.

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Chapter 5

Conclusions and Future Scope

5.1 Conclusion

A novel technique for reducing switching action at the source inputs was designed by replacing the traditional LFSR approach with a combinational circuit, resulting in a final TPG with the smallest hamming distance between test patterns. Using the Xilinx tool, the proposed design was simulated and verified. From proposed technique we are able to test the given circuit by using the logical BIST with maximum fault coverage and minimum power dissipation.

5.2 Future scope

Bit-swapping LFSR provides a random test sequence with minimal switching power by calculating the hamming distance between two consecutive patterns and utilising combinational logic to minimise that distance. Dual threshold voltages are provided to further minimise the average power. This method can be used to reduce total power, particularly leakage power, by identifying the critical and non-critical paths present in BIST.

5.2.1 Application in the societal context

- Because contemporary technologies and packaging are difficult to design and VLSI testing difficulty BIST has emerged as the best solution.
- Most ATE functionalities are implemented on chip by Logic BIST, which reduces test costs by reducing test time, requiring less tester memory, or using a less expensive tester.

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