

Objective

To create a bidirectional level shifter using a MOSFET.

Level Shifting

Take a logic level voltage and convert it to another logic level voltage. Useful to convert UART/I₂C/SPI communications between a device that operates at a 5V logic level and another at 3.3V logic level...

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Logic Level Shifting Basics | DigiKey

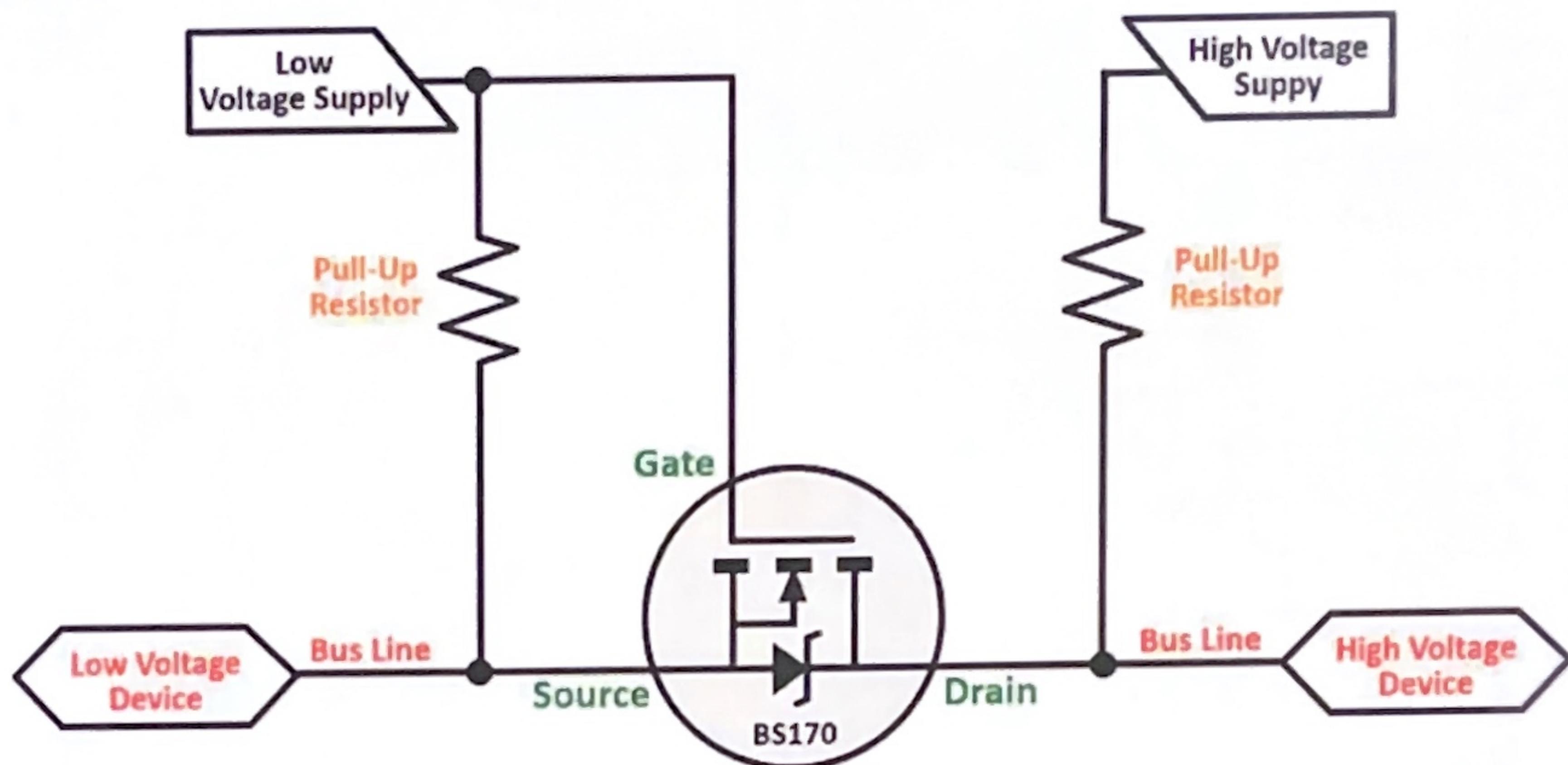


Figure 1: Basic, single bus, level translation MOSFET circuit.

The logic high levels on each side of the MOSFET are achieved by pull-up resistors to their respective supplies providing conversion of fast mode (400 kHz) I²C signals or other similarly fast digital interfaces. The gate of the MOSFET is held at the low voltage supply level. When no device is pulling down the bus line, the bus line at the MOSFET's source is pulled up by the low voltage pull-up resistors. The MOSFET's Gate/Source voltage (VGS) is below the threshold, and the MOSFET is not conducting. This allows the bus line at the MOSFET's drain to be pulled up by the higher-voltage pull-up resistor. The bus lines on each side of the MOSFET are held HIGH but at different voltage levels. See Figure 2.

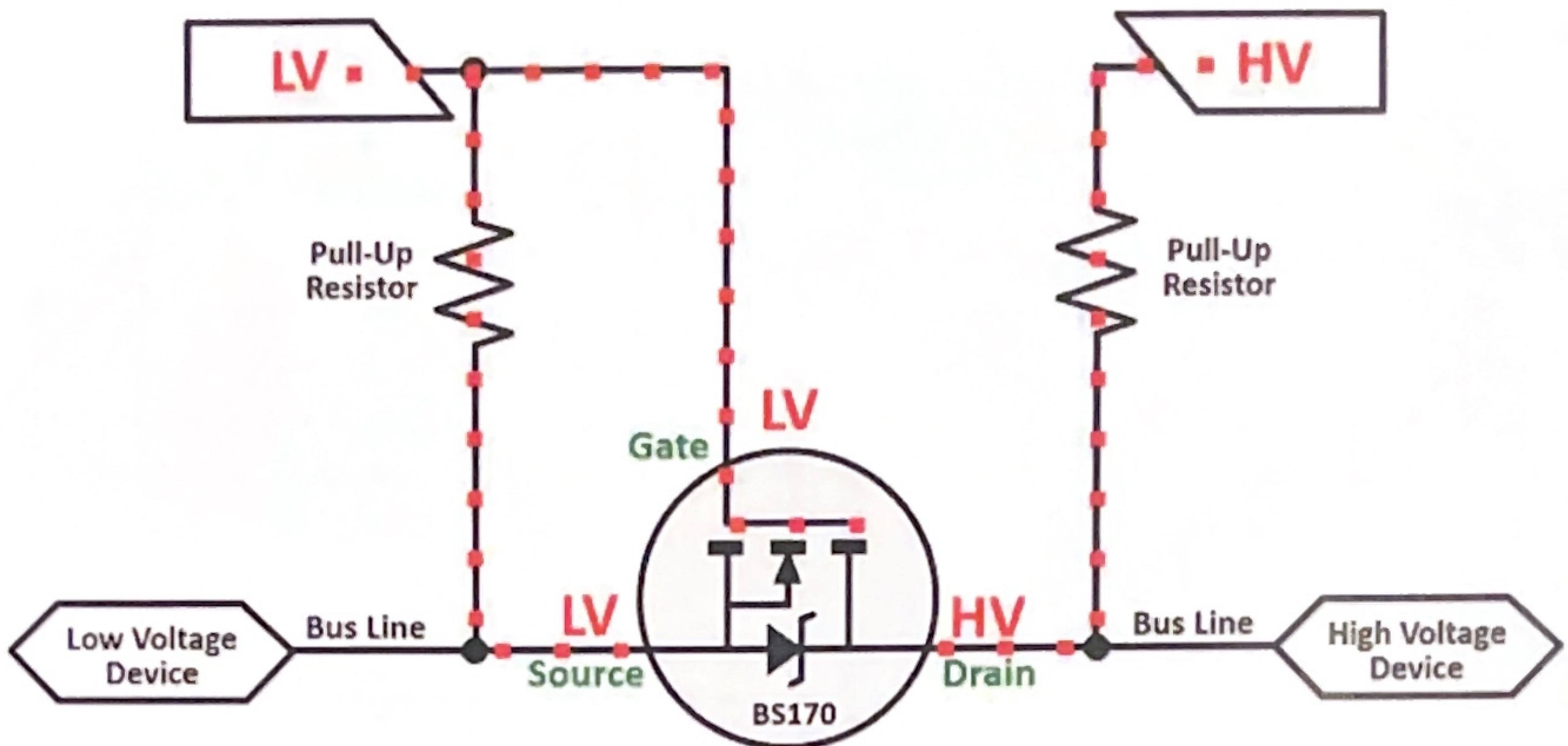


Figure 2: Logical HIGH voltage translation.

If the low voltage device pulls down the bus line at the MOSFET's source and the gate remains at the low voltage supply, VGS rises above the threshold and the MOSFET starts to conduct. The bus line at the MOSFET's drain is now pulled down as well. Refer to Figure 3.

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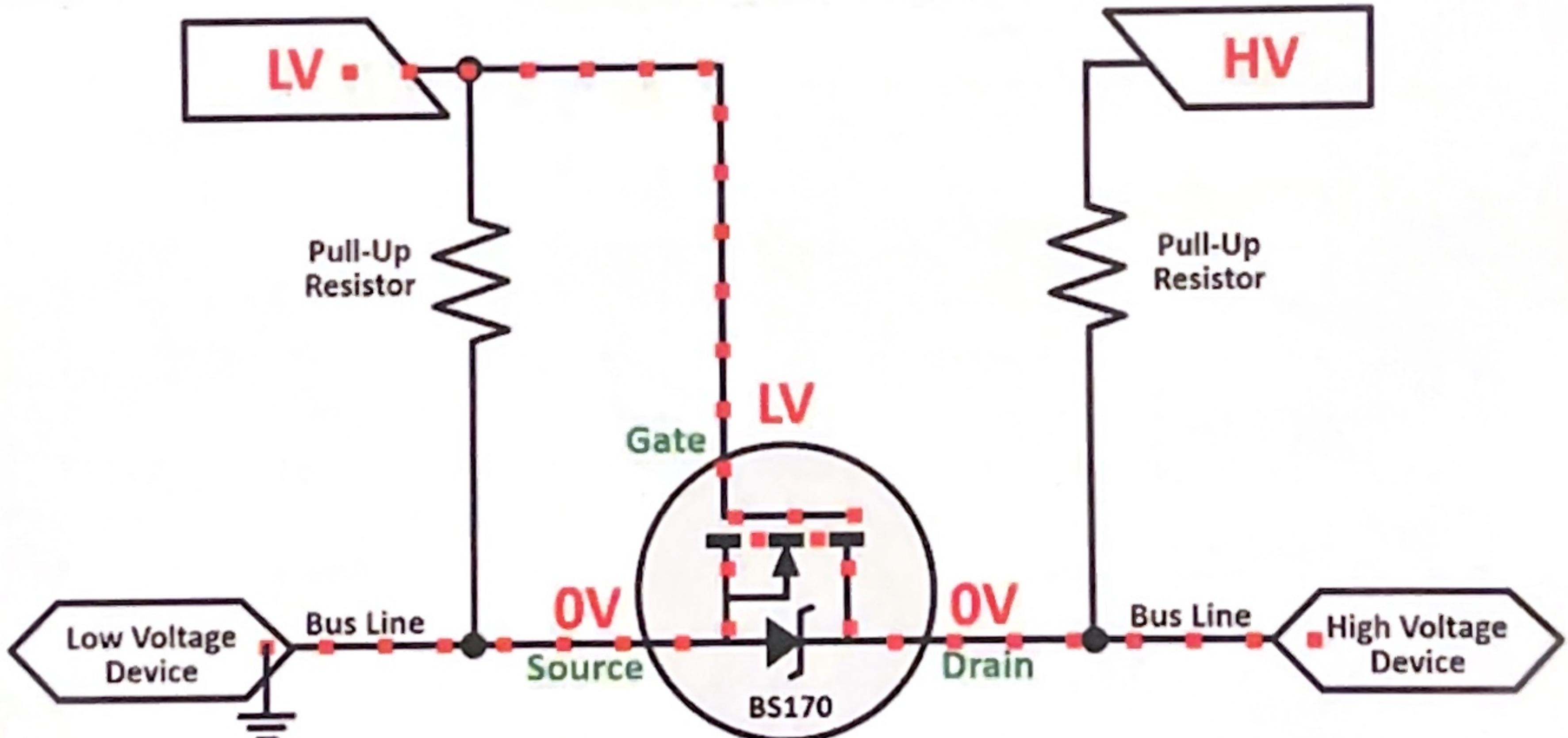


Figure 3: Logical LOW voltage translation initiated by low voltage device.

If the high voltage device pulls down the bus line at the MOSFET's drain, the MOSFET's substrate diode allows the source to also be partially pulled down due to a small amount of voltage dropped across the diode. See Figure 4.

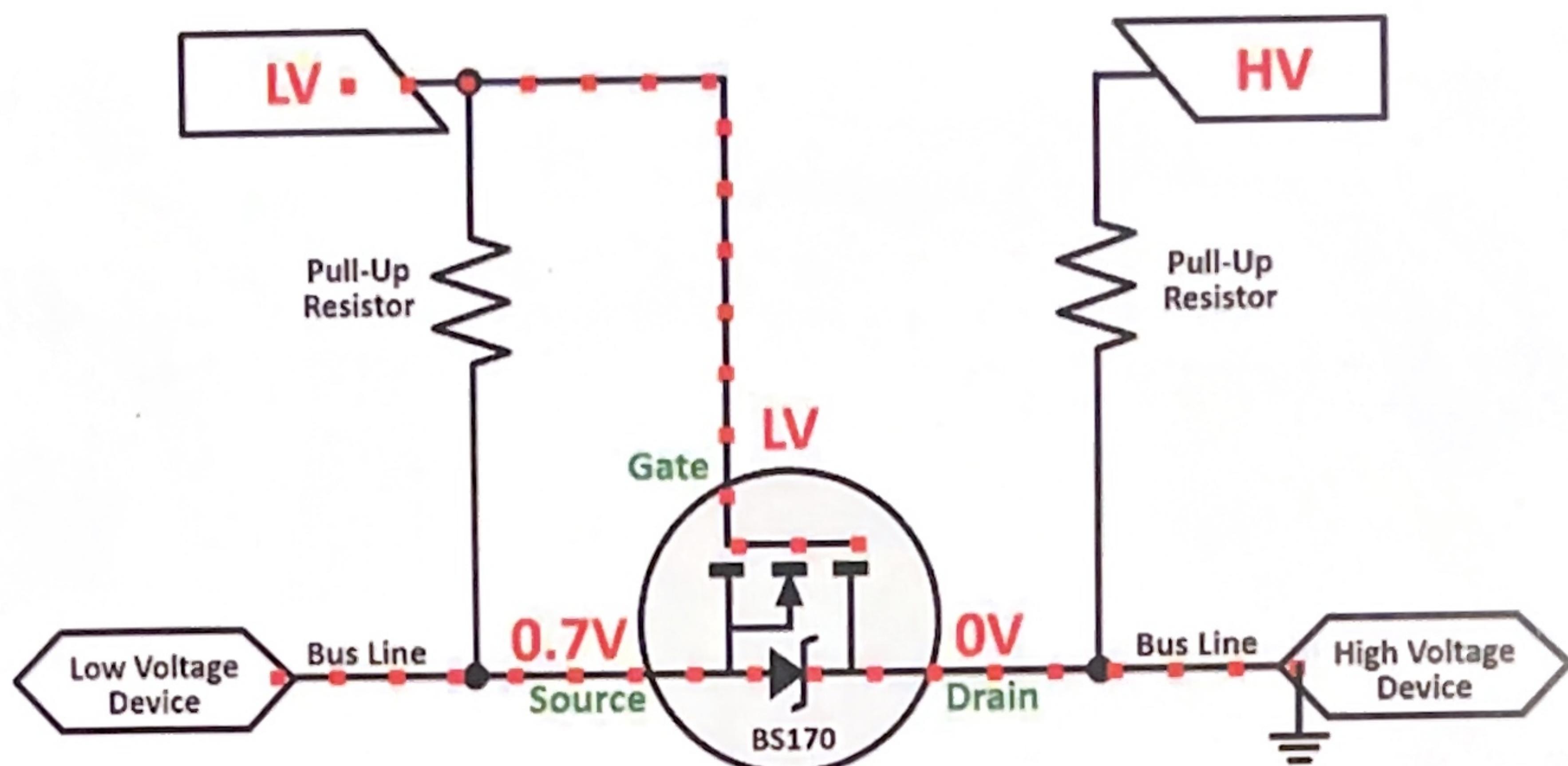


Figure 4: Near logical LOW voltage translation initiated by a high voltage device.

When the MOSFET's source is partially pulled down, the VGS rises above the threshold and the MOSFET starts to conduct effectively bypassing the substrate diode. See Figures 5.

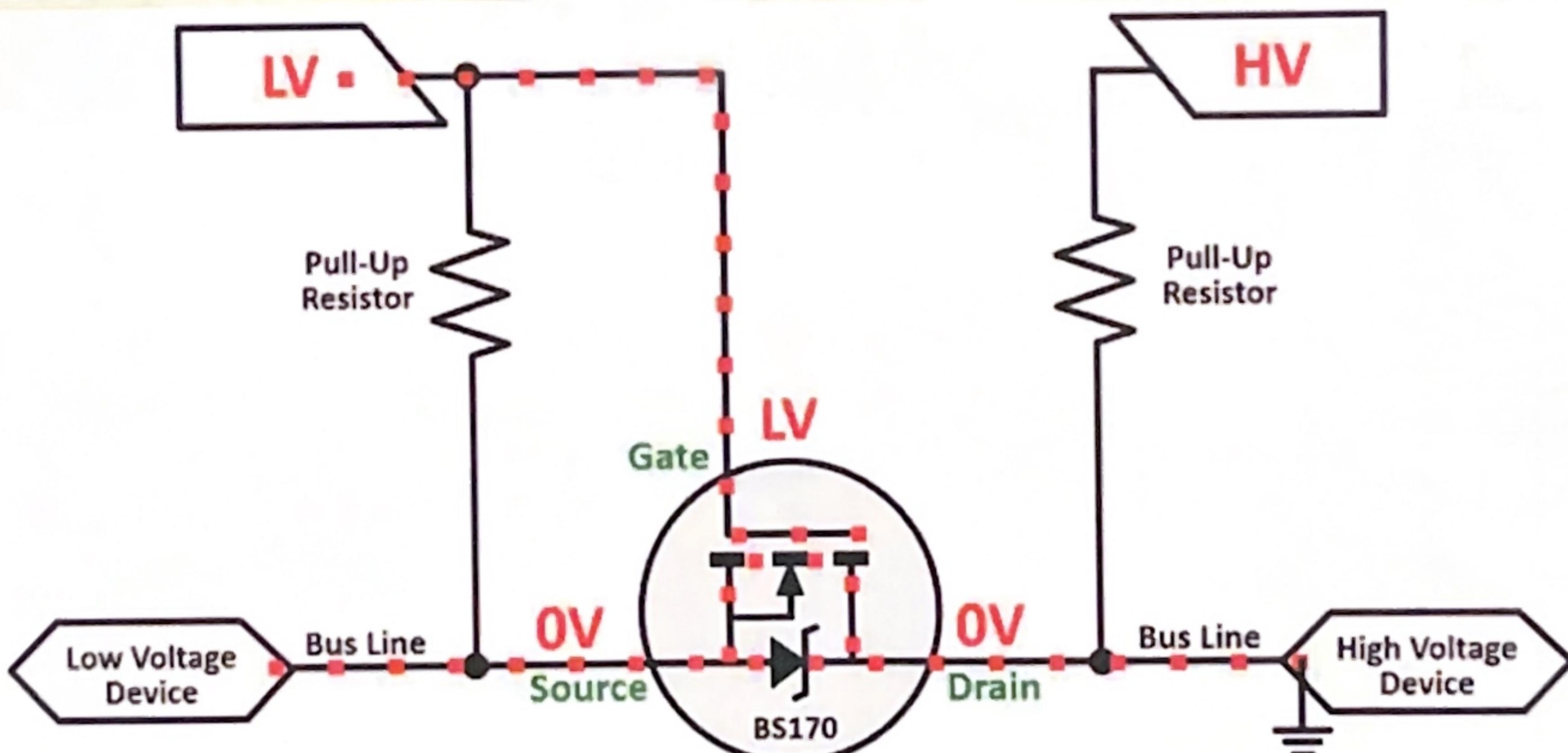
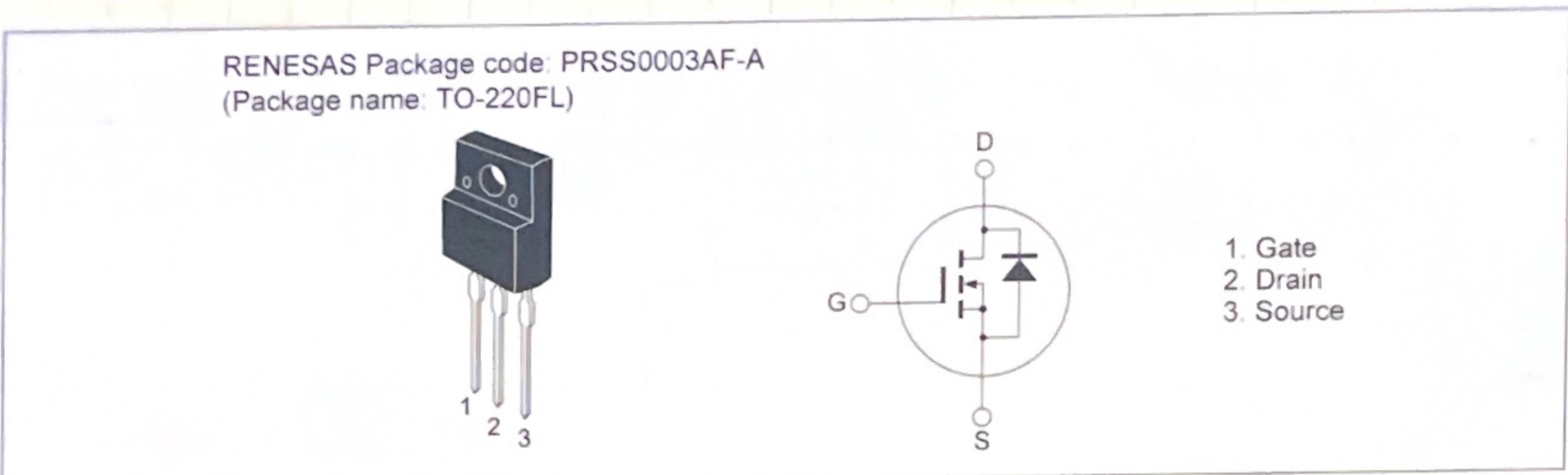


Figure 5: Full logical LOW voltage translation initiated by high voltage device.

The three states show transferred logic levels in both directions of the bus system, independent of the driving section. Many combinations of high and low voltage supplies are possible depending upon the capabilities of the MOSFET. Whether the logic level conflict involves point-to-point GPIO, sensor output, or bidirectional multi-line communication, MOSFET level shifters are useful tools. Figure 5 demonstrates the implementation of a translated, two-line, bidirectional communication circuit using two MOSFETs.

Enhancement Mode N-channel MOSFET

These will allow current to be pulled through the drain when a voltage difference exists between the gate and source. If $V_{GS} \geq 0$, then the mosfet is OFF and not conducting current through the drain.

RJK 5030**Absolute Maximum Ratings**

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	5	A
Drain peak current	I_D (pulse) <small>Note 1</small>	20	A
Avalanche current	I_{AP} <small>Note 3</small>	5	A
Channel dissipation	P_{ch} <small>Note 2</small>	28.5	W
Channel to case thermal Impedance	θ_{ch-c}	4.38	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. Pulse width limited by safe operating area.

2. Value at $T_c = 25^\circ\text{C}$ 3. $S T_{ch} = 25^\circ\text{C}$, $T_{ch} \leq 150^\circ\text{C}$

RJK5030DPP-M0**Electrical Characteristics**

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	500	—	—	V	I _D = 1 mA, V _{GS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 500 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±30 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	3.5	—	4.5	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	1.3	1.6	Ω	I _D = 2 A, V _{GS} = 10 V ^{Note 4}
Input capacitance	C _{iss}	—	550	—	pF	V _{DS} = 25 V
Output capacitance	C _{oss}	—	60	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	10	—	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	—	15	—	ns	V _{DD} = 200 V
Rise time	t _r	—	20	—	ns	I _D = 2 A
Turn-off delay time	t _{d(off)}	—	90	—	ns	V _{GS} = 10 V
Fall time	t _f	—	30	—	ns	R _g = 25 Ω
Total gate charge	Q _g	—	13	—	nC	V _{DD} = 400 V
Gate to source charge	Q _{gs}	—	3.3	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	6.6	—	nC	I _D = 5 A
Body-drain diode forward voltage	V _{DF}	—	0.9	1.5	V	I _F = 5 A, V _{GS} = 0 ^{Note 4}
Body-drain diode reverse recovery time	t _{rr}	—	250	—	ns	I _F = 5 A, V _{GS} = 0 V _{DD} = 250 V dI _F /dt = 100 A/μs

Note: 4. Pulse test

Notice that this mosfet requires somewhere between 3.5V and 4.5 V to conduct current.

This mosfet won't be very useful as a level shifter, but we can still try it out.

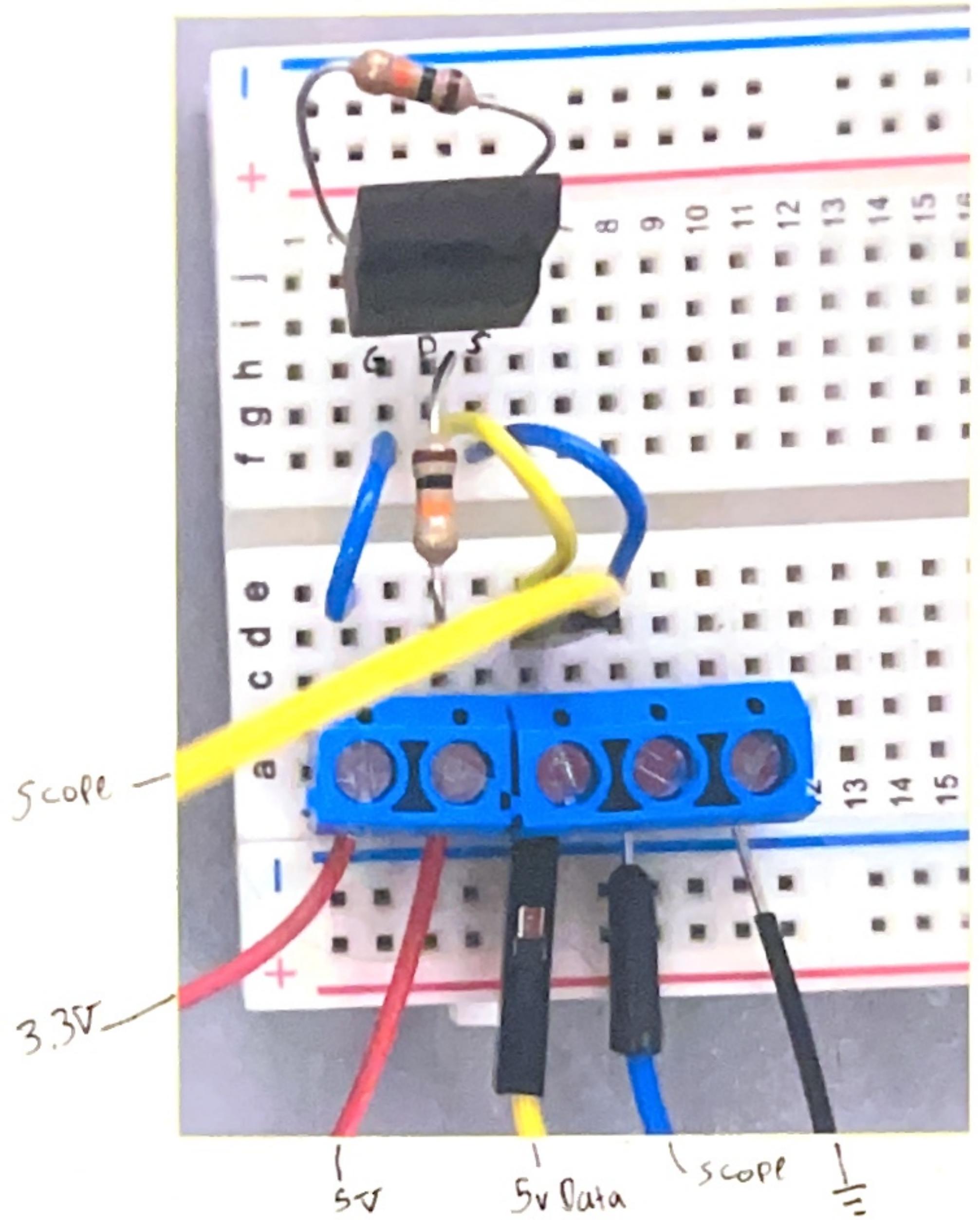
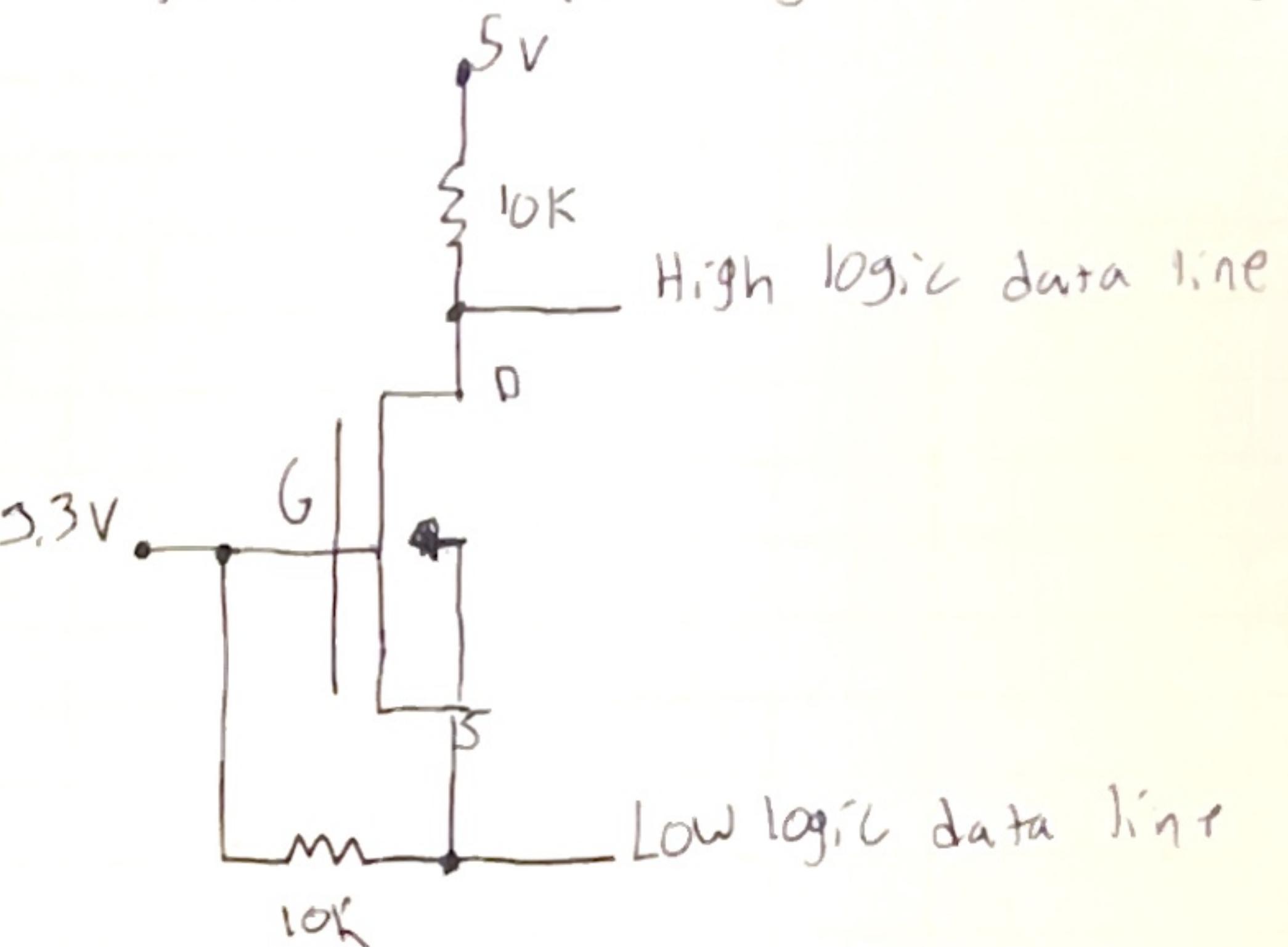


Figure 1

Creating the bidirectional level shifter.

It follows the following circuit diagram:



* This works to convert 5V down to 3.3, but will not work to convert 3.3 up to 5 because of V_{gs} specified by the data sheet.

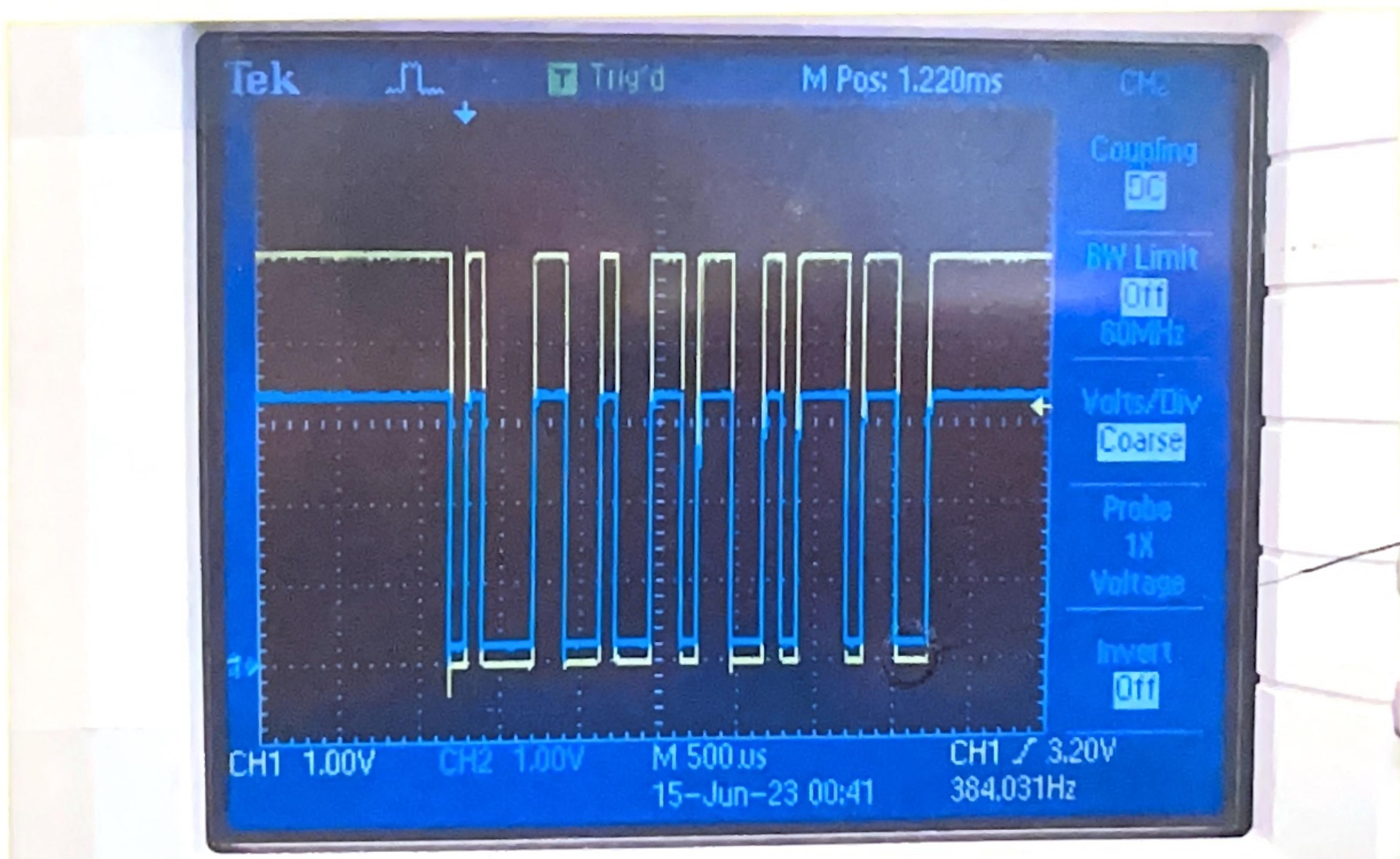


Figure 2

Shifting 5V data down to 3.3V.

Notice the voltage from the substrate diode when the high data line pulls the com low!

To show that the bidirectional feature works, we can first convert the 5V data to around 4.1V data using a voltage divider. Then allow the mosfet to bring it back up to 5V. This is a little bit of a bad example since we already have the 5V data line. However, it should be noted that normally we wouldn't do this. This is only because the V_{GS} on this mosfet is so high.

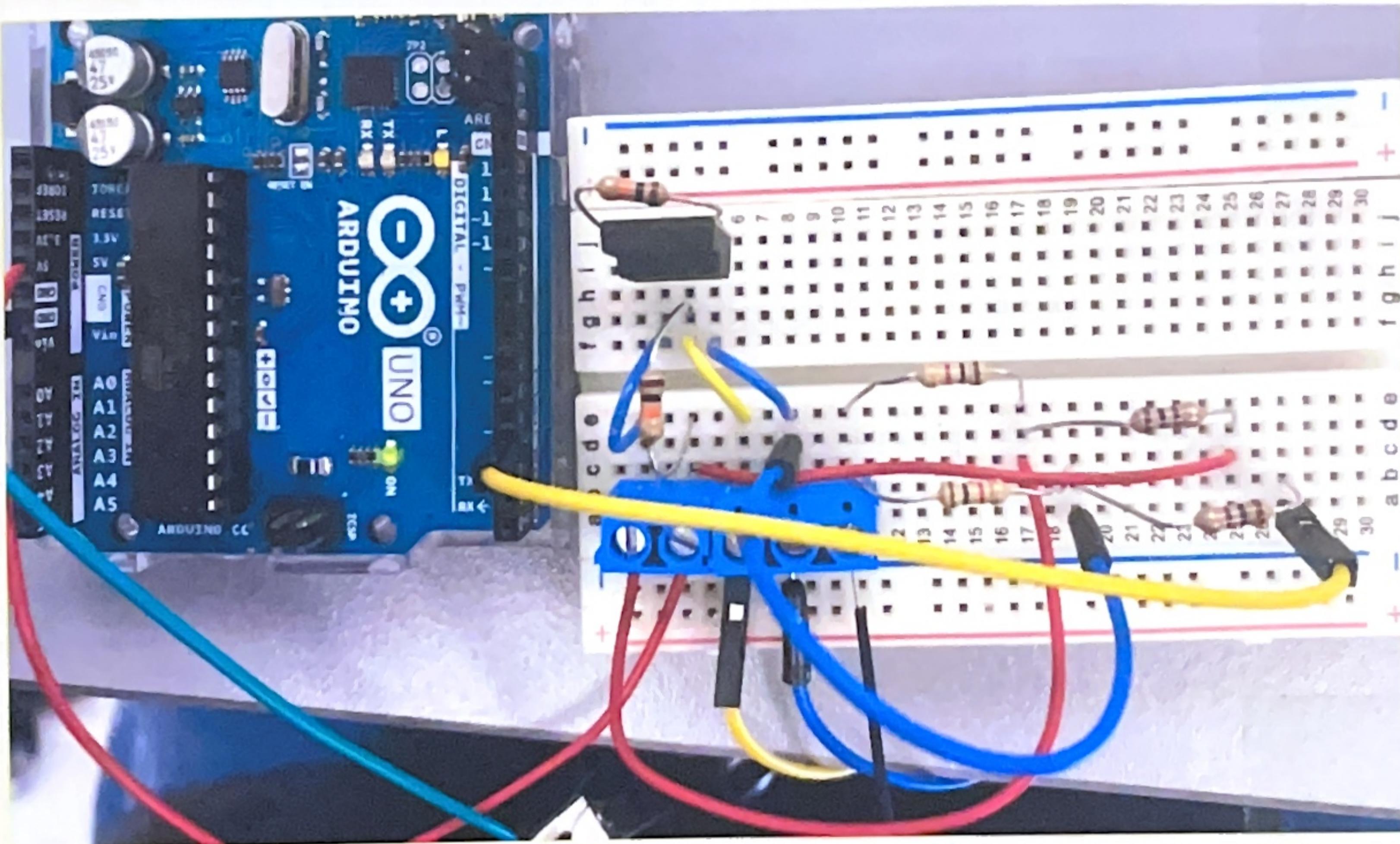
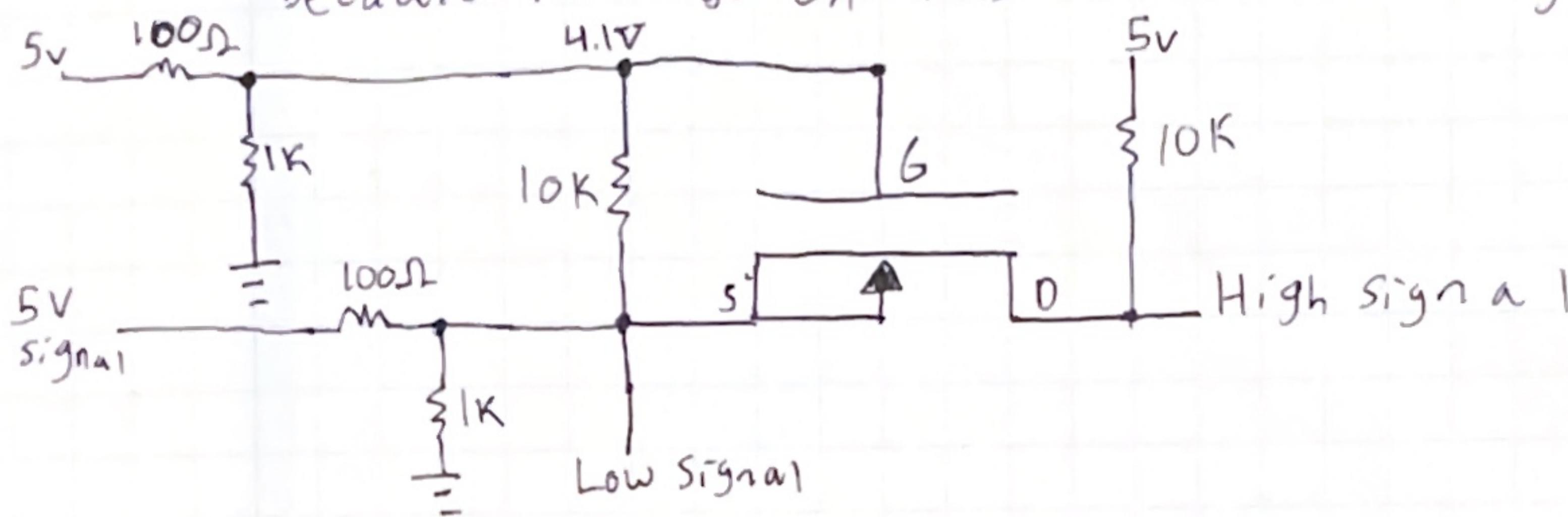
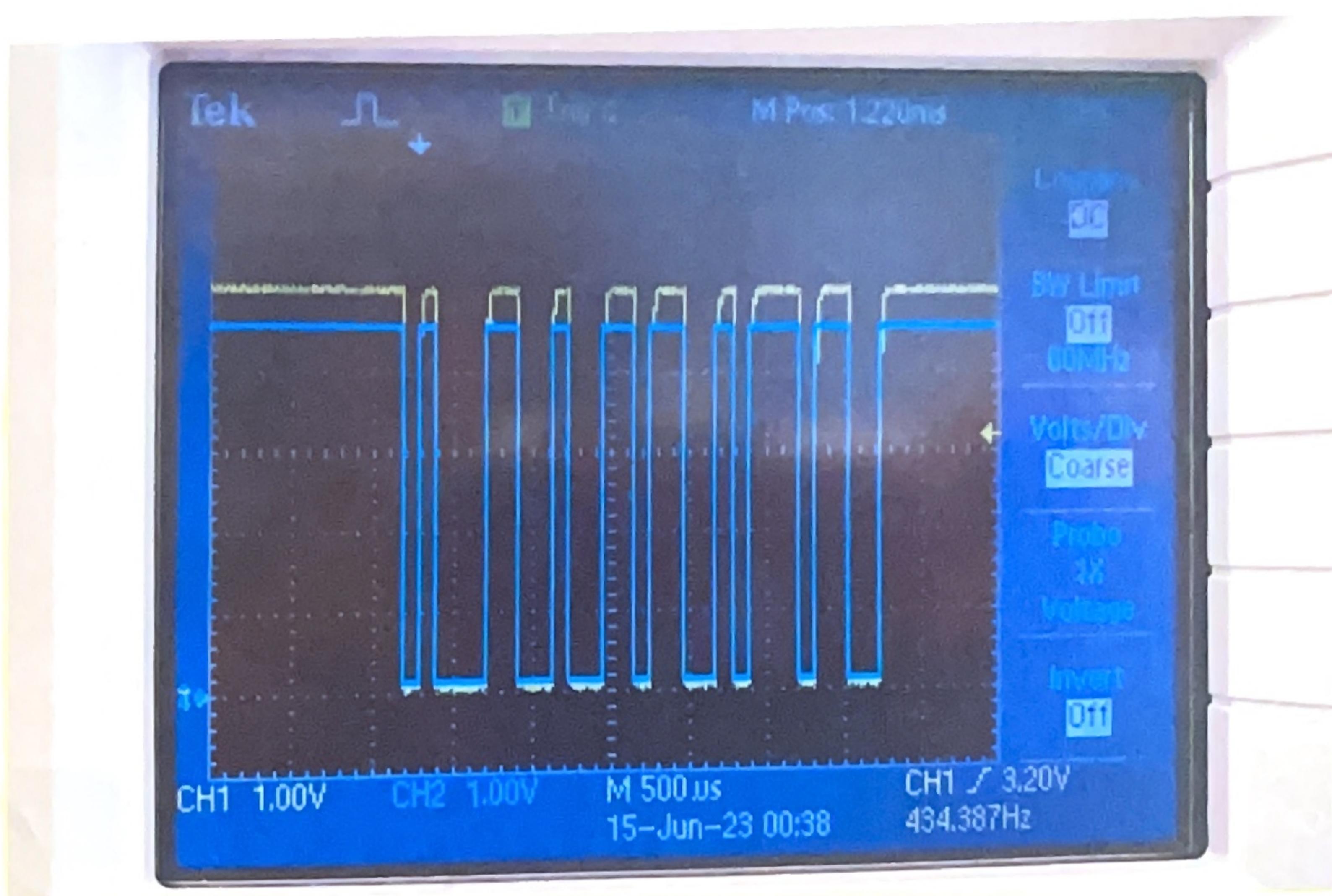


Figure 3

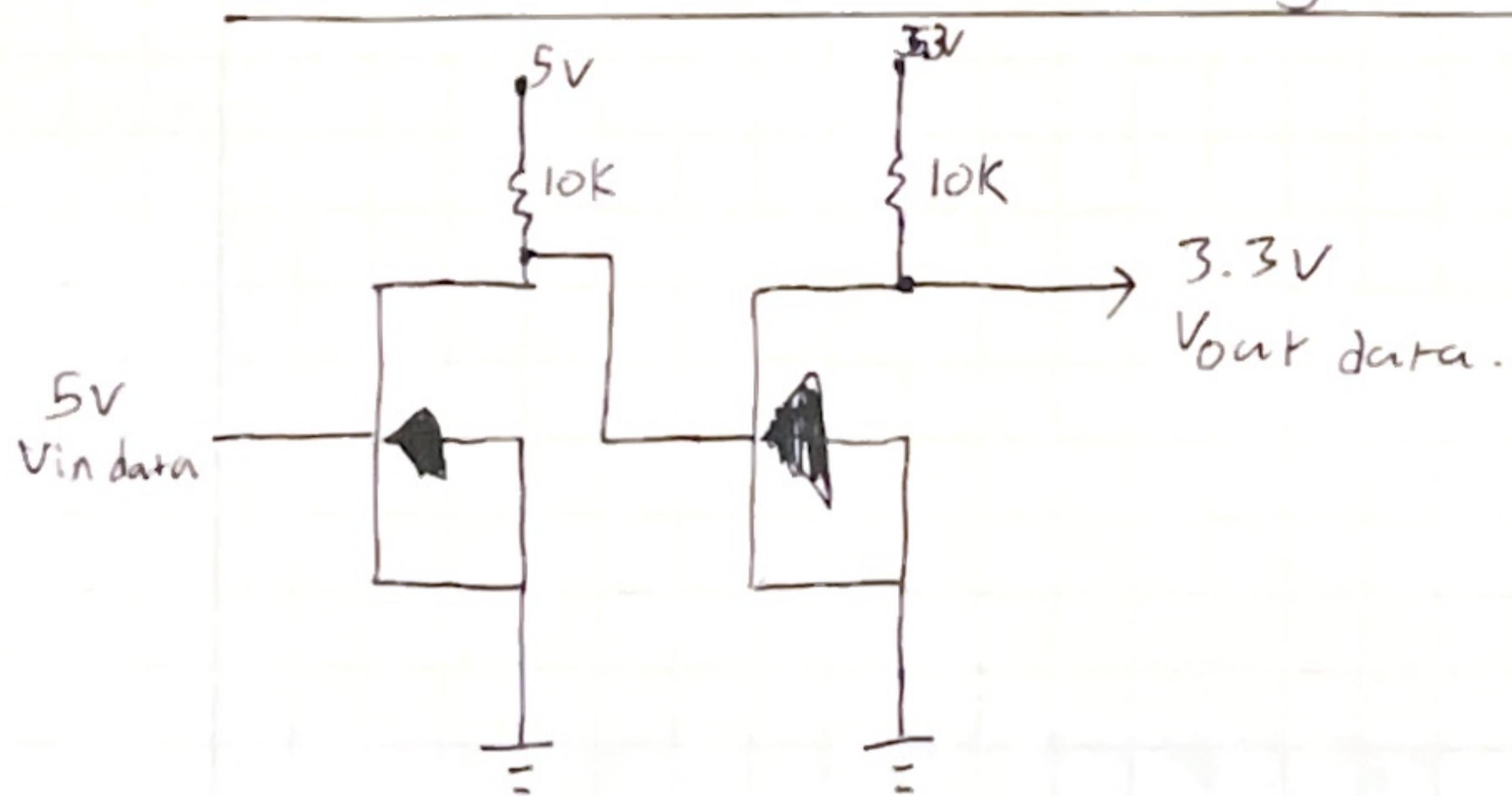
Creating the circuit to shift a 4.1V signal to 5V.

① ① ① ① ①
4.1V 5V 5V 4.1V GND

Figure 4

Showing the mosfet can shift a lower signal to a higher one.

One Direction Level Shifting using two mosFets

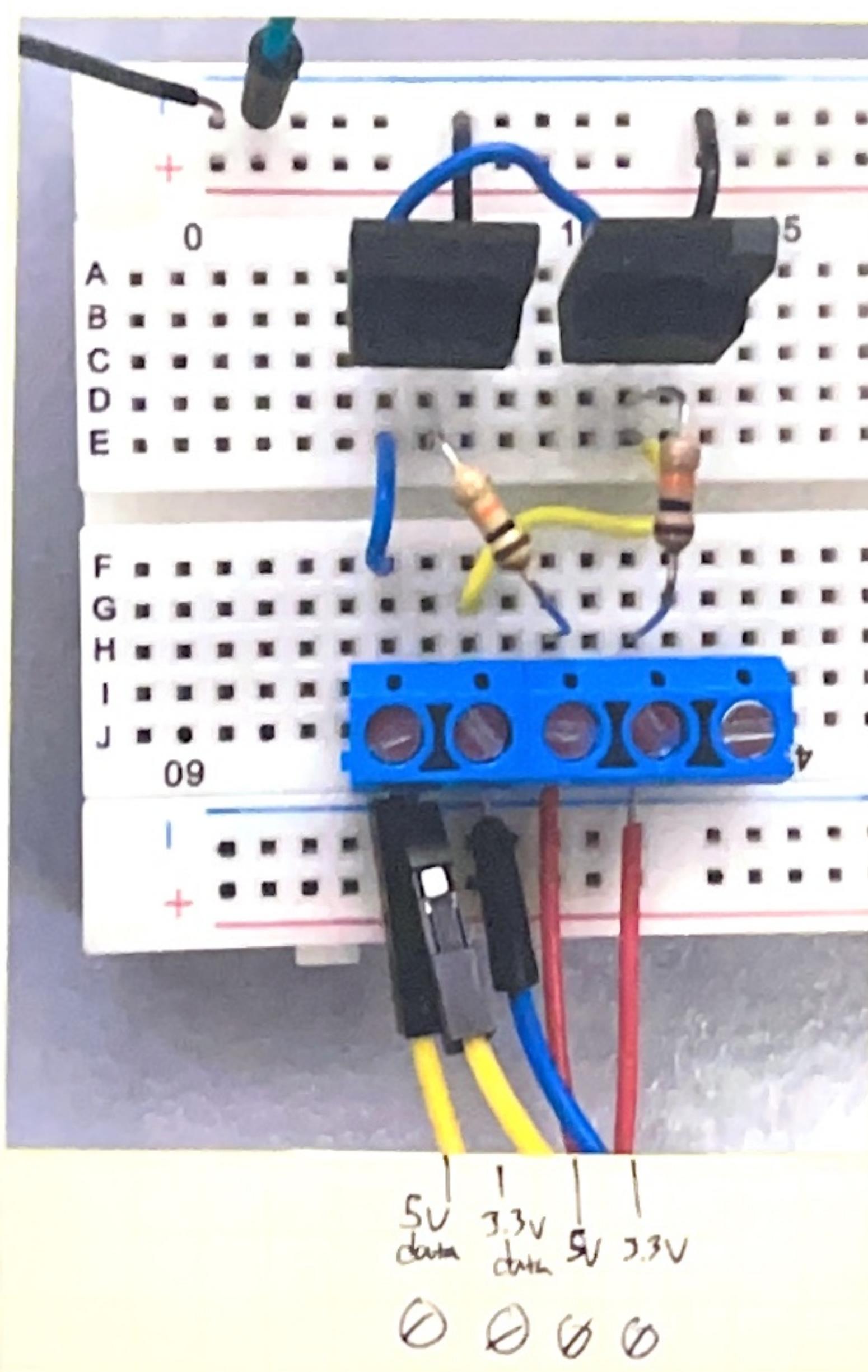
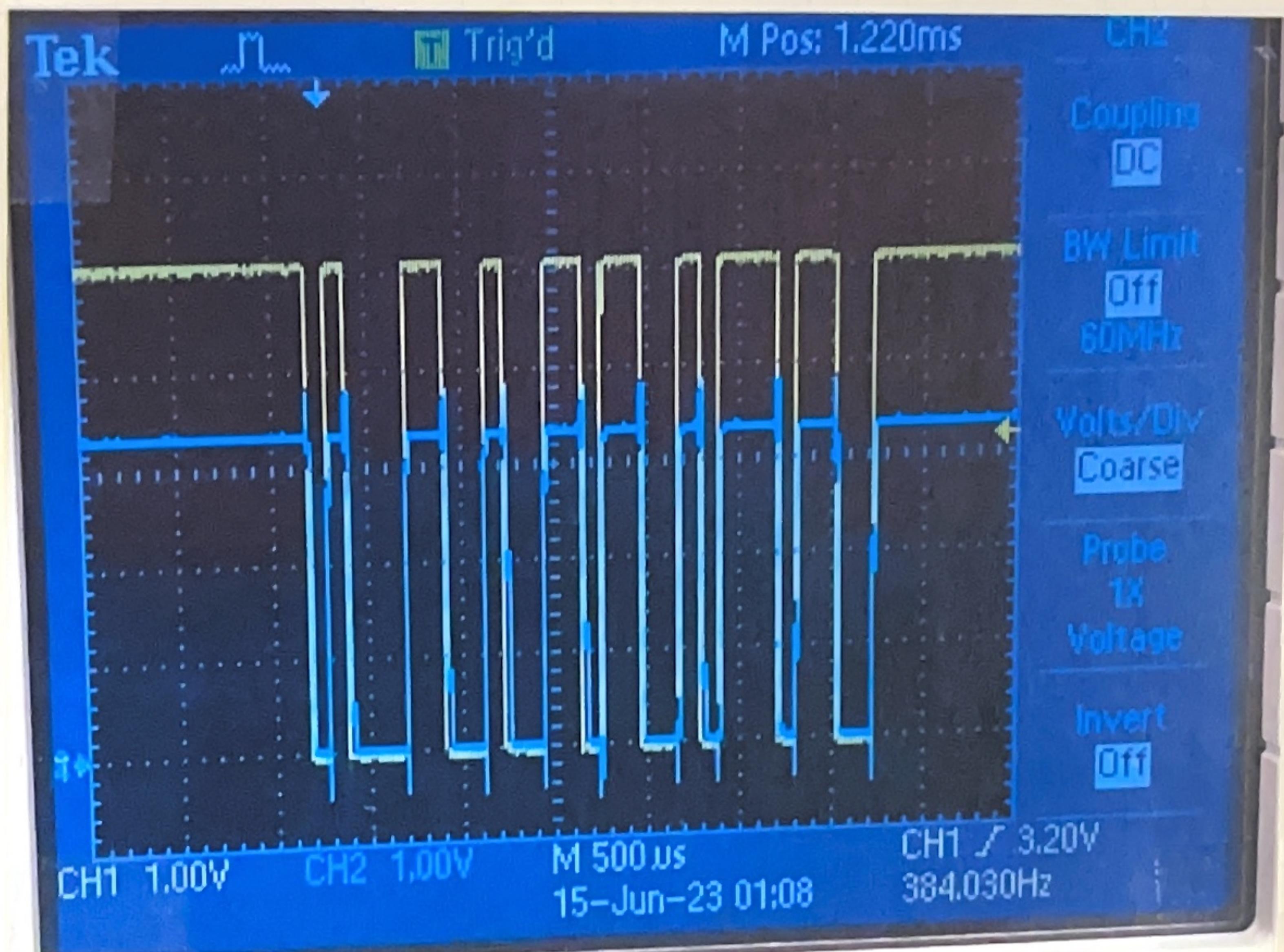


In this circuit, when the $V_{in\ data}$ goes high, current is pulled across the 5V and 10k. This will turn off the second mosfet. This makes the 3.3V not drop across the resistor, therefore $V_{out\ data}$ is also high.

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47



Figures 5 + 6
using two mosfets to level shift.

* One problem with the previous circuit is that if you are trying to convert from a lower voltage to a higher voltage, you are limited by V_{gs0} . In this case we need around 4.1V to activate the MOSFET.

To see the shift we can use the same trick as with the bidirectional level shifter. That is to use a voltage divider to convert a 5V signal to 4.1V signal.

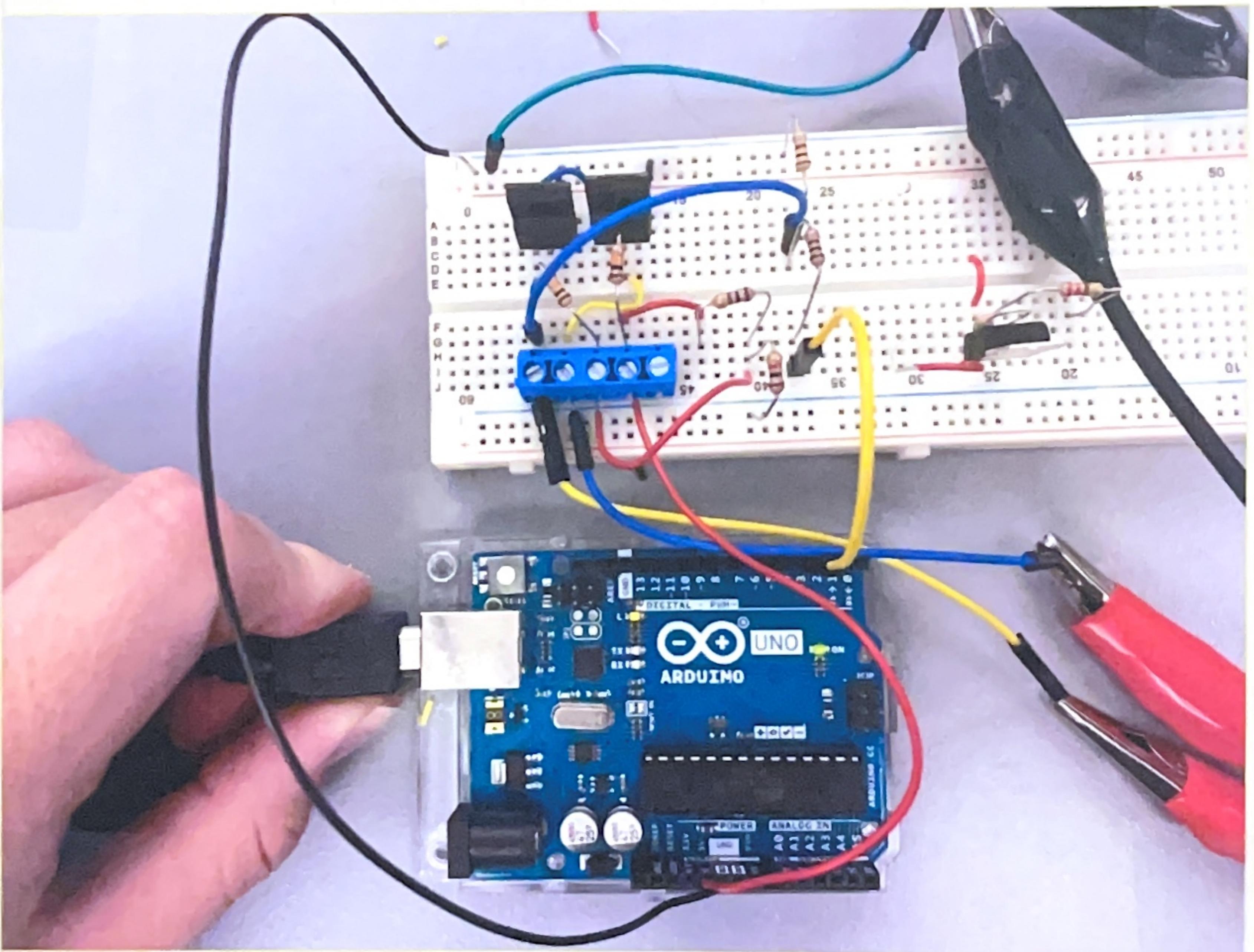
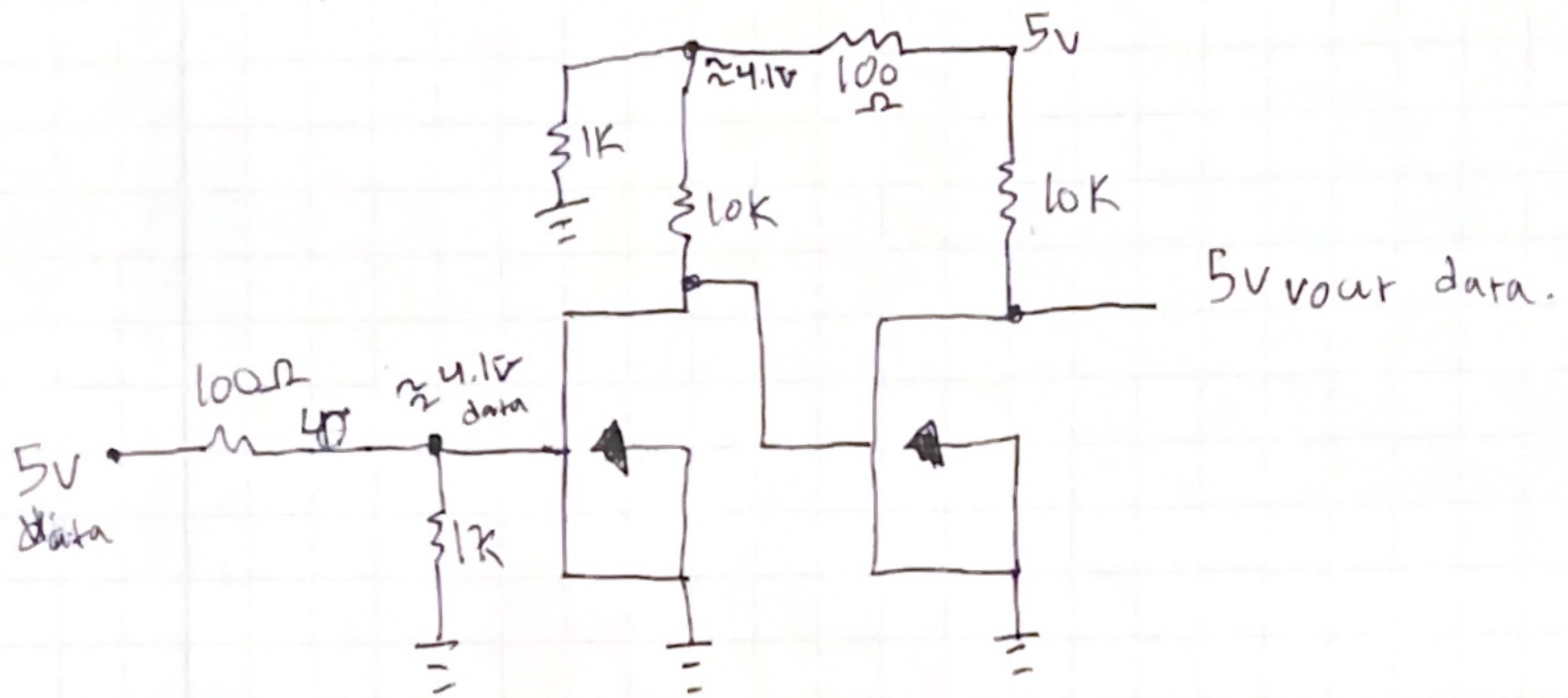


Figure 7
circuit.

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49



Figure 8

We see the 4.1V data is shifted to 5V.

Conclusions

Level Shifting is possible using the MOSFETs. However, it would be better to us a mosfet that has a lower V_{gs} . This would allow us a bigger range of shifting.