Implementation of IEEE 802.15.4 transceiver on software defined radio platform

Uroš Pešović, Dušan Gliech, Peter Planinšič, Zoran Stamenković, Siniša Randić

Abstract — Measurement of error probability parameters in IEEE 802.15.4 transmission requires clear access to all stages of commercially available IEEE 802.15.4 transceivers. Since these transceivers are realized as monolithic chips, with limited access to certain transceiver stages, we created an IEEE 802.15.4 transceiver on a Software Defined Radio (SDR) platform with clear access to all transceiver stages. Using the realized transceiver, we were able to create a system for measurement of error probability parameters in IEEE 802.15.4 transmission.

***Keywords* — IEEE 802.15.4, Software defined radio, Error probability**

I. Introduction

Information-bearing signal, sent through a wireless channel, is received together with some unwanted signals, which are referred as noise. Noise can change the received signal in such a manner that is decoded with some data errors. Knowledge of error probability of wireless transmission is of key importance when deploying networks in noisy environment. In order to increase immunity to noise, modern radio transceivers employ spreading techniques, such as transceivers compliant to IEEE 802.15.4 standard. Use of spreading adds to complexity of transceivers as well as complexity of determining mathematical relations for expected bit error rate (BER). In such case empirical models, based on measured results are used for modeling bit error rate in the channel. Since IEEE 802.15.4 compliant transceivers are composed from several stages, besides bit error probability, there are several probability parameters which could be interesting to analyze, such as chip, symbol and packet error rate. Packet and bit error rate can be measured on commercially available IEEE 802.15.4 transceivers, since packets and bits represents inputs and outputs for transceiver. Situation is quite different with chips and symbol error rate since these parameters are on lower level stages in transceivers which are inaccessible for user to monitor them.

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Recent introduction of SDR platforms [2] enabled researchers a fast way of prototyping radio communication equipment. The implementations of IEEE 802.15.4 transceivers on SDR platforms were recently presented in papers [3],[4], [5] and [6].

In this paper we described implementation of IEEE 802.15.4 transceiver in 2.4 GHz band on a NI USRP-2921 SDR platform which enables the measurement of all error probability parameters in radio transceiver chip.

II. IEEE 802.15.4 Wireless Transceivers

IEEE 802.15.4 standard specifies physical and Medium Access Control layers for Low Power Wireless Personal Area Networks [1]. It is designed for low power, low cost battery operated devices, which are used in home automation, precision agriculture, medicine and military applications. Its physical layer defines channels in several frequency bands, where a 2.4 GHz band is most commonly used. IEEE 802.15.4 standard compliant radio devices are designed as transceivers and they employ transmitter and receiver on the same chip and they share common antenna. Typical functional structure of such transceiver is separated into transmission and reception part (Fig. 1).

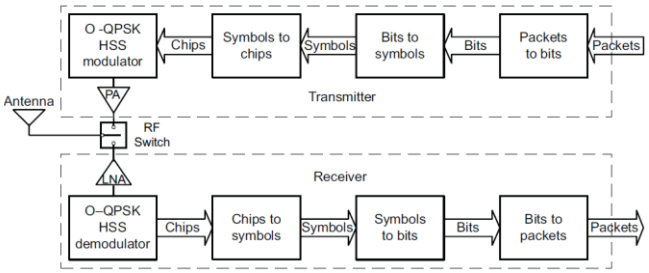

Fig. 1 Structure of IEEE 802.15.4 transceiver

Packet which is ready for transmission is firstly partitioned into groups of four bits, which are referred as symbol words. Coexistence of IEEE 802.15.4 networks in a crowded 2.4 GHz band, which is also used by other types of networks (WLAN and Bluetooth), is possible by usage of Direct-sequence spread spectrum (DSSS) signal spreading technique. Symbol words are spread into one of 16 nearly orthogonal sequences of 32 chips. Chip sequences are predetermined by standard and carefully chosen in order to be maximally dissimilar from each other. Chip sequences are divided into two groups of sequences (C_0 to C_7 and C_8 to C_{15}), whose sequences are created by right cyclic shifting of their respective previous chip sequences for four chip positions (Table 1). Chip's sequences of the other group are created through inversion of odd-indexed chip values of the respective chip sequence from the opposing group (C_0 to C_8; C_1 to C_9; . . . ; C_7 to C_{15}) [7].

TABLE 1: IEEE 802.15.4 SYMBOL TO CHIP MAPPING [7]

Symbol	*Chip sequence*	*Symbol*	*Chip sequence*
S_0 (0x0)	C_0 (0x744AC39B)	S_8 (0x8)	C_8 (0xDEE06931)
S_1 (0x1)	C_1 (0x44AC39B7)	S_9 (0x9)	C_9 (0xEE06931D)
S_2 (0x2)	C_2 (0x4AC39B74)	S_{10} (0xA)	C_{10} (0xE06931DE)
S_3 (0x3)	C_3 (0xAC39B744)	S_{11} (0xB)	C_{11} (0x06931DEE)
S_4 (0x4)	C_4 (0xC39B744A)	S_{12} (0xC)	C_{12} (0x6931DEE0)
S_5 (0x5)	C_5 (0x39B744AC)	S_{13} (0xD)	C_{13} (0x931DEE06)
S_6 (0x6)	C_6 (0x9B744AC3)	S_{14} (0xE)	C_{14} (0x31DEE069)
S_7 (0x7)	C_7 (0xB744AC39)	S_{15} (0xF)	C_{15} (0x1DEE0693)

Chips are modulated with the use of Offset QPSK with the Half Sine pulse Shaping (O-QPSK HSS) modulation. This modulation uses two orthogonal phases, where even indexed chips are modulated onto in-phase I signal, while the odd-indexed chips are modulated onto quadrature phase Q signal. Both binary phases are shaped by half sine pulses and the Q phase is delayed by one chip period after which the resulting signal is modulated on 2.4 GHz carrier (Fig. 2.). The use of the O-QPSK HSS modulation enables continuous phase change, which is the preferable phase change type in case of energy-efficient nonlinear amplifiers such as those present in IEEE 802.15.4 transceivers.

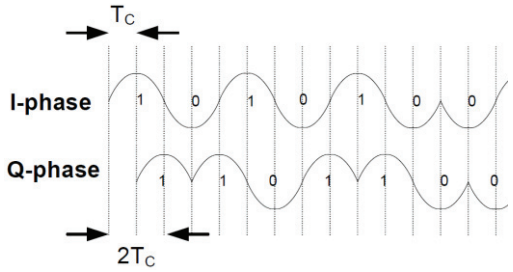

Fig. 2. O-QPSK HSS modulation

During reception, wireless signals received by an antenna, are amplified and processed by an analog front-end. After processing, they are brought to O-QPSK HSS demodulator, where information is extracted in a form of digital chips. Depending on the quality of the received wireless signal some of the chips can be decoded incorrectly. When received chip sequence is formed, it's cross-correlated with predefined chip sequences, and symbol of most similar sequence is fed to next stage. Symbol words are translated to bits, and finally, bits are grouped into packets, which are forwarded to the upper protocol layer.

Receiver in IEEE 802.15.4 transceiver is in most cases much more complex then transmitter. One of the reasons which add to receiver complexity is the need for synchronization which the receiver performs in order to successfully decode received data. Some radio receiver configurations, known as non-coherent demodulators, demodulate received signals directly form carrier, without need for synchronization. Such receiver structures are quite simple but their disadvantage is higher error probability introduced by demodulation process itself. Coherent demodulators are synchronized with received signal using preamble which is transmitted at beginning of IEEE 802.15.4 packet. Preamble represents a fixed pattern of symbol zero which is transmitted eight times. During that period the frequency of local oscillator in receiver is shifted using the Costas Loop circuitry in order to perform the phase locked loop (PLL). Coherent receivers are more complex than non-coherent, but they do not affect the bit error probability as non-coherent receivers do.

III. SOFTWARE RADIO PLATFORM

SDR is reconfigurable radio platform which is used for rapid prototyping of communication systems. It enables creation of physical layer algorithms with live physical signals on PC platform. It can be used for decoding received packets, monitoring spectrum of received signal, measuring bit error rate (BER) and etc. It's usually based on programmable FPGA chip coupled with analog front end which modulates and demodulates radio signals. FPGA enables reconfigurability as well as high processing power since all computations are carried out by hardware.

Software programmable radio transceiver NI USRP-2921 [8], designed for wireless communications in 2.4 GHz ISM band, is designed for prototyping of IEEE 802.11 and IEEE 802.15.4 transceivers. The NI USRP-2921 is connected to a host PC via Gigabit Ethernet Interface using appropriate USRP driver and can be integrated into Matlab and Labview applications. A simplified block diagram of NI USRP-2921 is presented in Fig. 3.

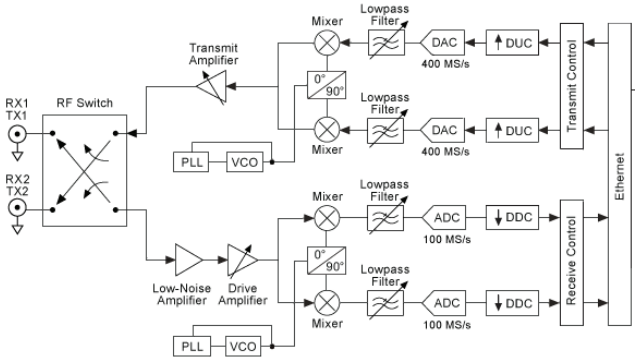

Fig. 3. NI USRP-2921 system block diagram

USRP radio employs two antennas which can be selected using internal radio switch. Received radio signals are amplified and then mixed with matching RF signal in order to extract baseband signal. Baseband signal is composed of I/Q components, which are filtered and sampled by a two channel, 100 MS/s, 14-bit analog-to-digital converter (ADC). The digitized I/Q data is down converted to user specified sample rate and passed to the host computer over a standard Gigabit Ethernet connection. Maximum sampling rate is 25 MS/s in full resolution mode, or 50 MS/s in 8-bit resolution mode.

During transmission baseband I/Q samples, synthesized by the host computer, are fed to a USRP-2921 over Gigabit Ethernet. The USRP hardware interpolates the incoming signals to 400 MS/s using a digital up conversion (DUC) process and then converts the signal to analog with a dual-channel, 16-bit digital-to-analog converter (DAC). The resulting analog signal is then mixed up with carrier and transmitted by transmitting antenna.

The USRP driver software provides functions for the the hardware/software configuration with tools for opening/closing sessions and performing read/write operations on the SDR platform. Using USRP driver, physical signals are transmitted to PC, where they can be analyzed and processed. Because of huge quantity of received information only slight data processing can be performed by PC computer in order to enable real-time operation. NI-USRP also enables that some of user defined computations can be carried on FPGA inside SDR in order to enable real time operation.

IV. IMPLEMENTATION AND RESULTS

Measurement of error probability in wireless communications is carried out by comparing data transmitted by the transmitter with data received by radio receiver. Since IEEE 802.15.4 uses signal spreading, several error probability parameters need to be monitored, such as: chip error rate at modulation level, symbol error rate at spread spectrum layer, and bit and packet error rate (Fig. 4).

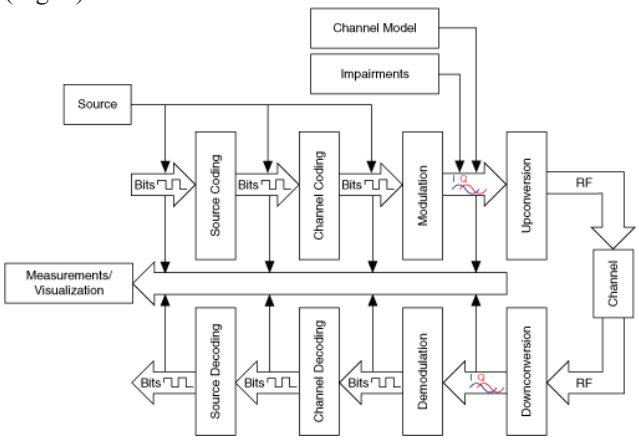

Fig. 4. Error probability measurement

Experiment was carried in Matlab, with one commercial MRF24J40 IEEE 802.15.4 transmitter and receiver implemented on SDR. Matlab application generated packet with random content which is forwarded to commercial IEEE 802.15.4 transmitter, which transmits packet to channel. Transmitted packet is mapped to transmitted chips, symbols and bytes in order to be compared with received data. Receiver processes chucks of data received by SDR platform, presented by I/Q signals in Fig. 5. Reception of a packet started from about 50th sample of the received data stream.

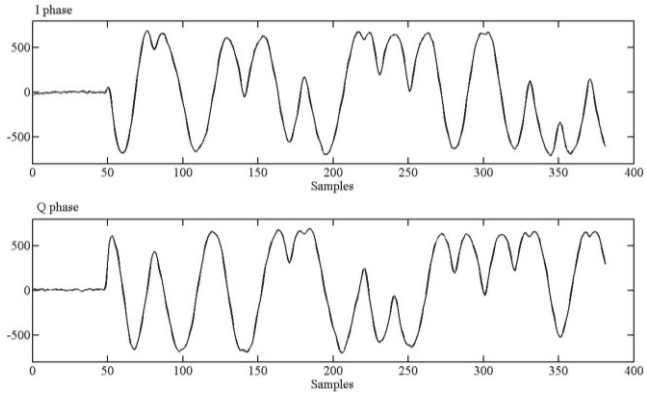

Fig. 5. I/Q signals at beginning of packet reception

Since IEEE 802.15.4 uses phase modulation, from received I/Q diagram we can monitor phase shift presented in Fig. 6. We can clearly saw continuous phase transition, characteristic for O-QPSK HSS modulation, starting form 50th sample at beginning of the packet. Phase discontinuations represents phase transition from $-\pi$ to π and vice versa. Before 50th sample, only noise was present in the channel, where phase therefore changes randomly.

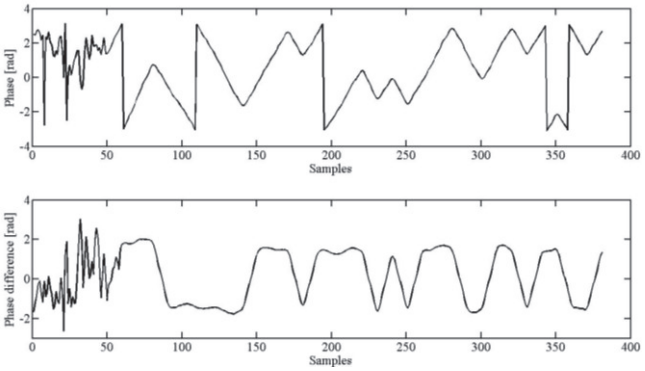

Fig. 6. Phase transitions at beginning of packet reception

Decoding of received information is carried out using differential detection. Phase values are sampled within one symbol period (in this case 10 samples) and phase difference was determined between phases of adjacent symbol samples. Positive value of the phase difference means that I/Q phasor is rotating counter-clockwise, while negative value means that I/Q phasor is rotating clockwise on phase transition diagram (Fig. 7).

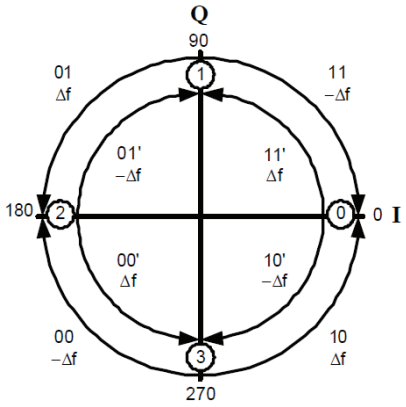

Fig. 7. Phase transitions diagram [9]

We can observe from phase transition diagram that increase or decrease of phase during two symbol periods will flip the previous state of I or Q chips; otherwise I or Q chip value will remain the same. Since packet starts with preamble which contains sequence “zero”, first two values for I and Q chips are logical ones. Values of other chips are alternatively determined by phase transitions, starting from first received symbol, until chip sequence is formed.

Received chip sequence is cross correlated with all 16 predefined chip sequences in order to find the most similar symbol sequence. If symbol sequence is equal to zero symbol of preamble sequence, receiver is successfully synchronized (Fig. 8). If not, it should resample symbols by delay of one sample and repeat whole process again.

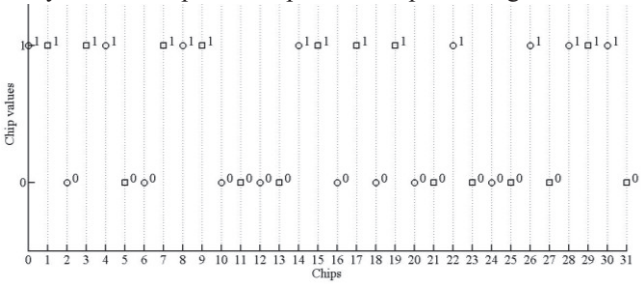

Fig. 8. Successful detection of preamble symbol

Receiver has eight preamble symbols for synchronization to incoming radio signal. After the receiver has successfully synchronized to incoming radio transmission, beginning of packet is signalized with start of frame delimiter sequence which lasts one byte. After that, receiver receives one byte long information, about length of the packet, which is followed by packet data. Received data is mapped to chips, symbols and bytes in order to be compared with transmitted data to determine error probability parameters in IEEE 802.15.4. wireless transmission.

V. CONCLUSION

This paper represents the implementation of IEEE 802.15.4 transceiver in 2.4 GHz band on SDR platform which enabled measurement of all error probability parameters in radio transceiver chip. This implementation enables simple demodulation which is carried out on PC, but because of huge amount of data and decoding on PC, real time operation cannot be achieved. Such lack did not affected measurement of the error probability parameters, because transmitter sent new packet after receiver finished with processing of previously received packet. Real time operation on SDR can be achieved by migrating software implemented algorithms, directly onto FPGA chip of the SDR platform, where it could be processed much faster, reducing processing delay to acceptable level.

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