THE GAUSS ELIMINATION FROM THE CIRCUIT THEORY POINT OF VIEW: DIAGONAL NODAL EQUIVALENT

Silvano Vergura[1]

***Abstract* — Nodal analysis is known to be the most used method to write the solving equations of electrical circuits. The matrix equation is usually solved by using Gauss Elimination (GE). This paper studies in depth the GE from a circuit theory point of view. It results that each step of GE constitutes a modification of the assigned circuit. The forward elimination can be considered as a successive removal of the independent nodes by introducing voltage-controlled current sources, while back substitution leads to independent elementary circuits. The whole procedure can be systematically applied; in this way, given a circuit, it is possible to switch to a modified circuit, by means of circuital transformations corresponding to mathematical ones.**

Similar approach can be used also when the mesh analysis is used to solve a circuit. In this case the forward elimination can be considered as a successive removal of the independent meshes by introducing current-controlled voltage sources.

***Keywords:* Circuit Theory, Gauss Elimination, Diagonal Nodal Equivalent, Forward Elimination, Back Substitution.**

I. INTRODUCTION

The method by which circuit equations are formulated is of key importance in a computer-aided circuit analysis and design program for integrated circuits. It affects significantly the set-up time, the programming effort, the storage requirements and the execution speed of the computer program. The method needs to be flexible, computationally efficient and saving storage. The nodal approach for formulating circuit equations is a classical method which not only meets these requirements but also brings to a numerically well-behaved diagonal [1]. To solve the formulated nodal equations, several strategies can be used. The choice depends on what the user want to determine. If anyone is interested only to obtain the solution set, then the fastest strategies will be considered; but in some cases the user could be interested even to determine other information about the circuit (e.g. the inverse coefficient matrix) and then other choices are realized. Let us focus the attention on the first case; the fastest solution strategies must utilize the smallest number of operations; obviously both of multiplications and divisions require much more computer time than additions or subtractions. Then, considering only the computer time necessary to realize the multiplication and/or the division operations, it result that the Cramer's rule is certainly excluded a priori, because it requires $2\cdot(n+1)!$ operations, where n represents the dimension of the coefficient matrix [2]. The inversion of the coefficient matrix employs n^3 operations, while the direct method with both the Gaussian Elimination (GE) and the LU factorization algorithms needs $\left(n^3+3n^2-n\right)/3 \cong n^3/3$ operations. Fig. 1 reports the number of operations versus the dimension of the coefficient matrix. The Cramer's rule case has not been reported for sake of clarity of the figure; in fact, for $n=100$, it require almost $2*10^{160}$ operations! Obviously, when the equations system has to be solved repeatedly as in the Newton-Raphson method for solving nonlinear functional equations, the problem becomes more serious.

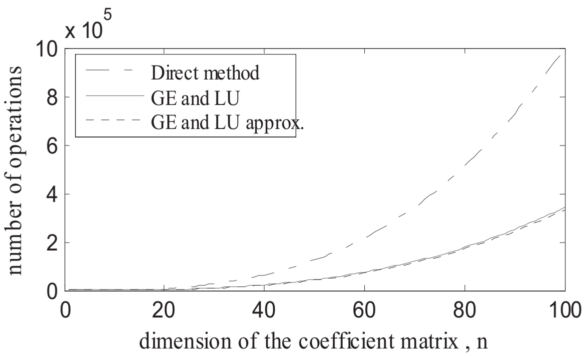

Fig. 1. Number of operations required by the direct method, GE and LU factorization.

The paper focus the attention on the GE algorithm, frequently used in methods devoted to hierarchical analysis [3]-[4] as well as to network reduction [5] of large analog circuits. Particularly, the scope of the paper is to interpret the GE from a circuit theory point of view. Section II consider the Nodal Analysis (NA) and the solution of the matrix equation by means of GE, which can be viewed as an iterative modification of the assigned circuit. Forward elimination leads to the Triangular Nodal Equivalent (TNE), while back

[1]*Department of Electrotechnics and Electronics*
Politecnico di Bari
Bari, Italy

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substitution leads a Diagonal Nodal Equivalent (DNE). In Section III the proposed method is extended to the AC analysis, while Section IV shows two examples.

II. GAUSS ELIMINATION FOR THE DC ANALYSIS

NA and Modified Nodal Analysis (MNA) are the most used methods in computer aided design of electric and electronic circuits.

In this paper we limits to examine only the GE applied to the NA. We start with the simple case of the DC analysis, considering the circuit under investigation constituted by conductances and DC independent current sources.

Transient analysis, at each integration step, solves equations related to the resistive companion model of the circuit; then transient analysis can be considered as a set of successive DC analyses. In this case, to utilize a fast solution method is particularly important because it allows a great computational saving.

Finally, all the results will be later extended to RLC circuits fed by AC sources.

For DC analysis, after choosing a datum node and applying Kirchhoff's Current Law (KCL) to n independent nodes, the following matrix formulation is obtained:

$$\boldsymbol{G} \cdot \boldsymbol{V} = \boldsymbol{J} \tag{1}$$

where $\boldsymbol{G}$ represents the $n \times n$ *node-conductance matrix*, $\boldsymbol{V}$ the *nodal voltage vector* and $\boldsymbol{J}$ the *equivalent nodal current source vector*.

Solving (1) allows all the nodal voltages and, subsequently, all the branch currents and voltages to be obtained. As yet explained in Section I, computational considerations indicate to solve (1) by applying GE or LU factorization. GE will be applied in this paper.

Expanding (1), is obtained:

$$\begin{cases} g_{11}V_1 + g_{12}V_2 + \dots + g_{1n}V_n = J_1 \\ g_{21}V_1 + g_{22}V_2 + \dots + g_{2n}V_n = J_2 \\ \quad \dots \\ \quad \dots \\ g_{n1}V_1 + g_{n2}V_2 + \dots + g_{nn}V_n = J_n \end{cases} \tag{2}$$

The GE consists in two steps: the Forward Elimination (FE) and the Back Substitution (BS). The former one allows to transform the assigned coefficient matrix $\boldsymbol{G}$ in an upper triangular matrix, while the latter one allows to transform the upper triangular matrix in a diagonal one (as it will be explained later). Then the *i-th* nodal voltage can be determined solving only the *i-th* equation.

As the matrix $\boldsymbol{G}$ represents the *node-conductance* matrix, it takes into account the topology of the circuit as well as the typology of each element belonging to the circuit. Each mathematical operation which introduces modifications onto the matrix $\boldsymbol{G}$ represents, from a circuit theory point of view, a modification of the circuit; nevertheless, after each matrix operation, the nodal voltages of the modified circuit are the same of those related to the previous circuit. Then, after each modification, the circuit corresponding to the modified matrix can be considered a *nodally equivalent circuit* of the previous one. It means that even if the modified circuit is, in general, topologically and typologically different from the previous one, nevertheless it is characterized by the same set of nodal voltages; i.e. the space of the nodal voltages is unmodified. After each matrix operation, the topology of the circuit corresponding to the modified matrix is fixed, even if the choice of the circuit to be considered is not unique.

At the end of all the matrix operations, the last considered circuit is characterized by the same set of nodal voltages as the assigned one and then its solution is constituted by the nodal voltages of the assigned circuit.

The overall procedure of GE is reported in Fig. 2; the bold path (first row) represents the direct method - computationally expensive - to obtain the solution set, while the alternative way is represented by the remaining rows.

At the first step, pre-multiplying left-hand and right-hand member of the matrix equation (box 1) by the product of the elementary matrixes (as defined later, box 2) a new matrix equation is obtained (box 3), characterizing a modified circuit (box 4), whose solution can be directly evaluated (box 5). This approach is iterated more and more times.

The first column represents the assigned circuit and the successive nodally equivalent modified circuits, while the last column highlights that each one of them is characterized by the same solution set, i.e. the nodal voltages.

From a theoretical point of view, at each generic step of GE the overall procedure can be stopped and its solution set is just the solution set of the assigned circuit, but this interruption does not take great computational advantages; nevertheless, for particular applications this possibility can be considered.

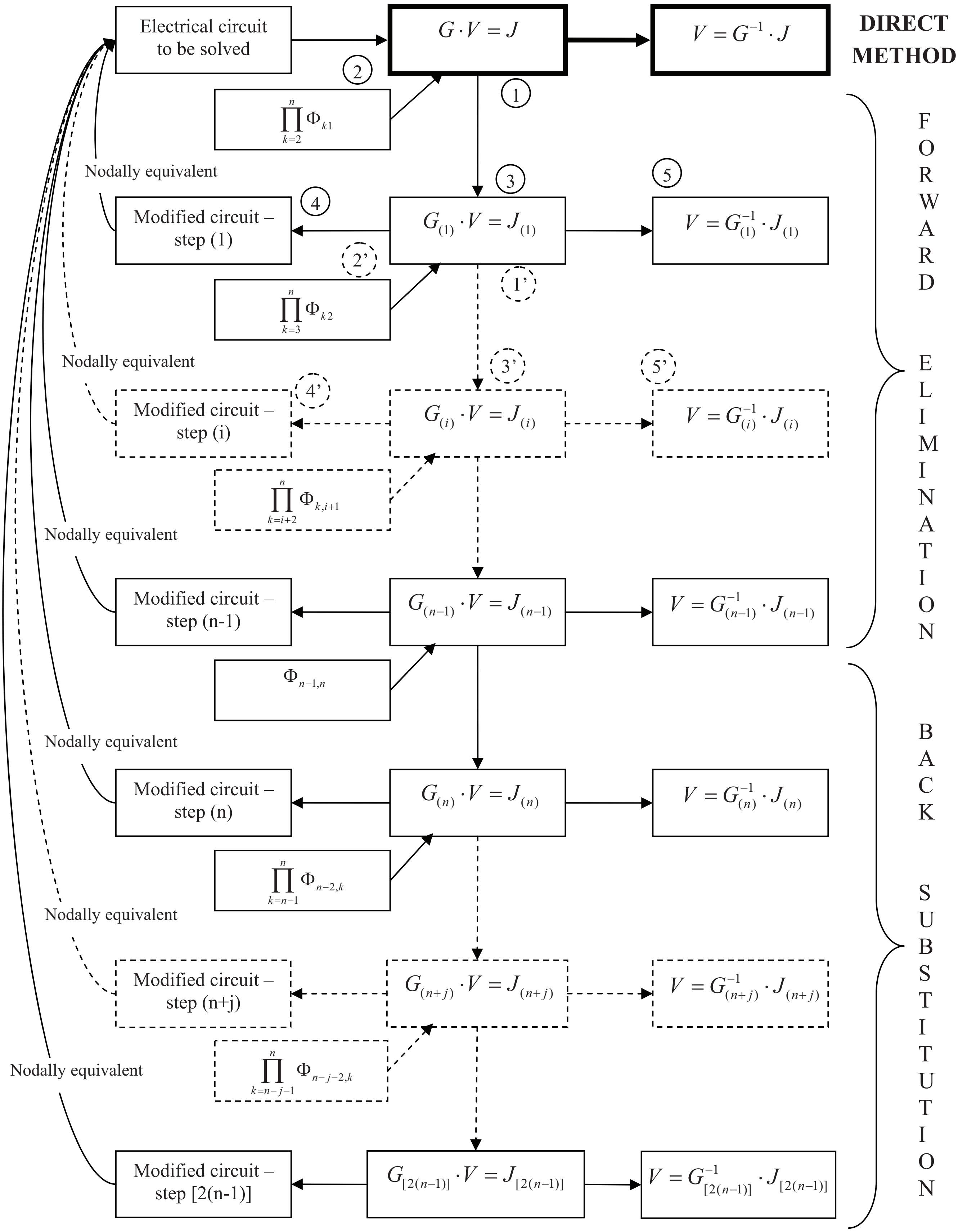

Fig. 2. Direct method (bold path) and GE to solve the assigned circuit

II.1) Forward Elimination (FE)

As yet explained, FE consists in transforming the matrix $\boldsymbol{G}$ into an upper triangular matrix. This operation can produce "fills"; then, let us suppose that *an optimal ordering technique* has been applied to eq. (1) in order to reduce the number of fills as more as possible.

The FE here described represents the *upper part* of Fig. 2.

FE is an iterative procedure; the first step consists in pre-multiplying the eq. (2) by the following elementary matrixes, i.e. unit matrixes with the exception of the entry $\varphi_{k1} = \frac{-g_{k1}}{g_{11}}$ for $k = 2...n$:

$$\Phi_{21} = \begin{bmatrix} 1 & 0 & ... & ... & ... & 0 \\ \frac{-g_{21}}{g_{11}} & 1 & 0 & ... & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & 0 & ... & 1 & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & ... & ... & ... & 0 & 1 \end{bmatrix} \quad \Phi_{31} = \begin{bmatrix} 1 & 0 & ... & ... & ... & 0 \\ 0 & 1 & 0 & ... & ... & 0 \\ \frac{-g_{31}}{g_{11}} & 0 & 1 & 0 & ... & 0 \\ 0 & 0 & 0 & 1 & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & 0 & ... & ... & 0 & 1 \end{bmatrix}$$

$$\Phi_{i,1} = \begin{bmatrix} 1 & 0 & ... & ... & ... & 0 \\ 0 & 1 & 0 & ... & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ \frac{-g_{i1}}{g_{11}} & 0 & ... & 1 & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & ... & ... & ... & 0 & 1 \end{bmatrix} \quad \Phi_{n,1} = \begin{bmatrix} 1 & 0 & ... & ... & ... & 0 \\ 0 & 1 & 0 & ... & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & 0 & ... & 1 & ... & 0 \\ ... & ... & ... & ... & ... & ... \\ \frac{-g_{n1}}{g_{11}} & 0 & ... & ... & 0 & 1 \end{bmatrix}$$

In this way, eq. (1) becomes:

$$\left(\Phi_{\boldsymbol{n}1} \cdot ... \cdot \Phi_{31} \cdot \Phi_{21}\right) \cdot \boldsymbol{G} \cdot \boldsymbol{V} = \left(\Phi_{\boldsymbol{n}1} \cdot ... \cdot \Phi_{31} \cdot \Phi_{21}\right) \cdot \boldsymbol{J} \quad (3)$$

and all the terms belonging to the first column of the eq. (2) are zero, except the first one. The procedure is newly applied to the eq. (3), pre-multiplying by $\left(\Phi_{n2} \cdot ... \cdot \Phi_{42} \cdot \Phi_{32}\right)$ so that all the terms belonging to the second column are zero, except the first and the second one, and so on. Each elementary matrix $\Phi_{kj} - type$ will be a unit matrix with the exception of the entry $\phi_{kj} = \frac{-g_{kj}}{g_{jj}}$.

When the procedure is finished, eq. (1) becomes, in compact form:

$$\boldsymbol{G}_{(\boldsymbol{n}-1)} \cdot \boldsymbol{V} = \boldsymbol{J}_{(\boldsymbol{n}-1)} \quad (4)$$

where $\boldsymbol{G}_{(\boldsymbol{n}-1)} = \left(\prod_{\substack{\boldsymbol{j}=\boldsymbol{n}-1,..1 \\ \boldsymbol{k}=\boldsymbol{n},..\boldsymbol{j}+1}} \Phi_{\boldsymbol{kj}} \right) \cdot \boldsymbol{G}$ is an upper triangular matrix with $g_{ii}^{(n-1)} \neq 0$ for $i = 1,...,n$, while $\boldsymbol{J}_{(\boldsymbol{n}-1)} = \left(\prod_{\substack{\boldsymbol{j}=1,..,\boldsymbol{n}-1 \\ \boldsymbol{k}=\boldsymbol{j}+1,..,\boldsymbol{n}}} \Phi_{\boldsymbol{kj}} \right) \cdot \boldsymbol{J}$ is the equivalent nodal vector $\boldsymbol{J}$ modified by the application of the elementary matrixes. The matrix equation (4) represents just the *Triangular Nodal Equivalent* (TNE) [6]. Similar equation is obtained when mesh analysis is used to solve a circuit [7].

From a circuit theory point of view to apply FE to eq. (2) means to transform the assigned circuit in accordance with the following:

***Theorem 1*[2]**

Let us consider an electrical circuit, constituted by only resistors and independent current sources. Applying the KCL to n independent nodes and then the FE corresponds to transform the assigned circuit as follows:

1. the elimination of the element g_{k1} (with $k = 2,...n$) implies to remove the *1-node* (i.e. the node number 1) from the assigned circuit; after the removal, between the *1-node* and datum node there will be:
   - all the current sources connected at the *1-node* in the assigned circuit;
   - a conductance $G_{eq,1} = \sum_j G_{1j}$;
   - as Voltage-Controlled Current Sources (VCCS) as mutual conductances G_{1j} are present; each VCCS$_j$ is controlled by the nodal voltage V_j, while its trans-conductance has the value of G_{1j}.
2. At every k-node which 1-node was connected to, it is needed to consider:
   - a current source between k-node and datum node (besides those already existing in the assigned circuit), having value $I_{s1} \cdot \frac{G_{k1}}{\sum_j G_{1j}}$, where I_{s1} is the current source connected to the 1-node, if present. This weighted current source will have the entering into or the going out direction according to the direction of I_{s1} in 1-node.

[2] For sake of clarity, $\mathrm{G_{kj}}$ represents the conductance between the nodes *k* and *j*, while $\mathrm{g_{kj}}$ represents the entry *(k,j)* of the matrix $\boldsymbol{G}$.

- A conductance $G_{k0}+G_{k1}-\dfrac{G_{k1}\cdot\sum_{j\neq 0}G_{1j}}{\sum_j G_{1j}}$ between the k-node and datum node, being G_{k0} the branch equivalent conductance between the k-node and the datum node in the assigned circuit;
- a conductance $G_{kh}+\dfrac{G_{k1}\cdot G_{h1}}{\sum_j G_{1j}}$ between *k-node* and *h-node*, if there was a conductance G_{1h} linking directly the 1-node with the h-node

3. The previous two steps, applied to remove the *1-node*, have to be iterated for all the remaining $(n-1)$ independent nodes.

Every time the steps 1 and 2 are applied to the *k-node*, it will result isolated from all the remaining nodes and its linkage information will be transferred to the subsequent nodes. Each removed node constitutes the *Standard Nodal Cell* (SNC), as shown in Fig. 3 for the *1-node*.

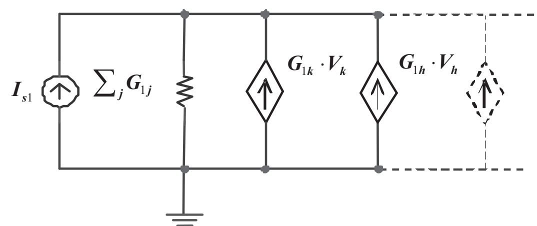

Fig. 3. Standard Nodal Cell (SNC) of the *1-node* after its removal.

Then, the starting circuit will result subdivided in n SNCs, whose the last one is constituted by only an equivalent independent current source with an equivalent parallel-connected conductance, called *elementary SNC* (e-SNC). This last cell is de-coupled from all the other nodes and allows to directly calculate the voltage of the *n-node*.

Now, let us study how this back substitution is obtained from a mathematical point of view and what it means from a circuit theory point of view.

II.2) Back Substitution (BS)

While the FE consists in transforming the matrix **G** into an upper triangular matrix $\boldsymbol{G}_{(n-1)}$, the BS transforms the previous triangular matrix $\boldsymbol{G}_{(n-1)}$ into a diagonal one. The BS here described represents the lower part of Fig. 3.

As FE, also BS is an iterative procedure. The first step consists in pre-multiplying the eq. (4) by the following elementary matrix:

$$\Phi_{n-1,n}=\begin{bmatrix}1 & 0 & \dots & \dots & \dots & 0\\ 0 & 1 & 0 & \dots & \dots & 0\\ \dots & \dots & \dots & \dots & \dots & \dots\\ 0 & 0 & \dots & 1 & \dots & 0\\ 0 & \dots & \dots & 0 & 1 & -g^{(n-1)}_{n-1,n}\\ 0 & \dots & \dots & \dots & 0 & 1\end{bmatrix} \tag{5}$$

After this, eq. (4) becomes:

$$\boldsymbol{G}_{(n)}\cdot\boldsymbol{V}=\boldsymbol{J}_{(n)} \tag{6}$$

with $G_{(n)}=\Phi_{n-1,n}\cdot G_{(n-1)}$ and $\mathrm{J}_{(n)}=\Phi_{n-1,n}\cdot \mathrm{J}_{(n-1)}$.

The *(n-1)-th* row of the coefficient matrix $\boldsymbol{G}_{(n)}$ will contain only one non-zero entry, just the pivoting element *(n-1,n-1)*. The procedure is newly applied, pre-multiplying eq. (6) by the following elementary matrixes:

$$\Phi_{n-2,n-1}=\begin{bmatrix}1 & 0 & \dots & \dots & \dots & 0\\ 0 & 1 & 0 & \dots & \dots & 0\\ \dots & \dots & \dots & \dots & \dots & \dots\\ 0 & 0 & \dots & 1 & -g^{(n-1)}_{n-2,n-1} & 0\\ \dots & \dots & \dots & 0 & 1 & 0\\ 0 & \dots & \dots & \dots & 0 & 1\end{bmatrix}\quad \Phi_{n-2,n}=\begin{bmatrix}1 & 0 & \dots & \dots & \dots & 0\\ 0 & 1 & 0 & \dots & \dots & 0\\ \dots & \dots & \dots & \dots & \dots & \dots\\ 0 & 0 & \dots & 1 & 0 & -g^{(n-1)}_{n-2,n}\\ \dots & \dots & \dots & 0 & 1 & 0\\ 0 & \dots & \dots & \dots & 0 & 1\end{bmatrix}$$

obtaining:

$$\left(\Phi_{n-2,n-1}\cdot\Phi_{n-2,n}\right)\cdot G_{(n)}\cdot V=\left(\Phi_{n-2,n-1}\cdot\Phi_{n-2,n}\right)J_{(n)}\,. \tag{7}$$

After this step also the *(n-2)-th* row will contain only one non-zero entry, just the pivoting element *(n-2,n-2)*.

The procedure is iteratively applied and each step allows to transform a row in another row in which only the pivoting element is non-zero. The BS finishes when also the first row will have only one non-zero entry, just *(1,1)* entry.

When the procedure is finished, eq. (4) becomes, in compact form:

$$\boldsymbol{G}_{[2(n-1)]}\cdot\boldsymbol{V}=\boldsymbol{J}_{[2(n-1)]} \tag{8}$$

where $\boldsymbol{G}_{[2(n-1)]}=\left(\prod_{\substack{j=1,..,n-1\\ k=j+1,..,n}}\Phi_{jk}\right)\cdot\boldsymbol{G}_{(n-1)}$ is a diagonal matrix with $g^{[2(n-1)]}_{ii}\neq 0$ for $i=1,\dots,n$, while $\boldsymbol{J}_{[2(n-1)]}=\left(\prod_{\substack{j=1,..,n-1\\ k=j+1,..,n}}\Phi_{jk}\right)\cdot\boldsymbol{J}_{(n-1)}$ is the equivalent nodal vector **J** modified by the application of the elementary matrixes.

The matrix equation (8) represents just the *Diagonal Nodal Equivalent* (DNE).

From a circuit theory point of view to apply BS to eq. (4) means to transform the circuit constituted by n SNCs in accordance with the following:

Theorem 2

Let us consider an electrical circuit constituted by only resistors, independent and voltage-controlled current sources, and suppose that KCL has been applied to n independent nodes. Moreover, let us suppose that the node-conductance matrix is un upper[3] triangular matrix, eventually obtained after a FE procedure. Applying BS corresponds to transform the assigned circuit as follows:

1. the elimination of the element $g_{n-1,n}$ implies to de-couple the $(n-1)-th$ SNC from the *n-node;* after the de-coupling, the $(n-1)-th$ SNC becomes an e-SNC with:
   - a current source between *(n-1)-node* and datum node having value $J_{n-1} + J_n \cdot \dfrac{g_{n-1,n}}{G_{nn}}$, where J_{n-1} is the pre-existing current source, J_n and G_{nn} are current source and conductance of the *n-th* e-SNC, respectively; $g_{n-1,n}$ is the trans-conductance of the voltage-controlled current source of the $(n-1)-th$ SNC. The weighted current source will have the entering into or the going out direction according to the direction of J_n in the *n-node*.
   - The same pre-existing conductance $G_{n-1,n-1}$.
2. The previous step, applied to de-couple the $(n-1)-$node, has to be iterated for all the remaining nodes until the first one. Every time the previous step is applied to the general *k-node*, it will result de-coupled from all the other nodes constituting an e-SNC.

Then, the starting circuit will result transformed in n de-coupled e-SNCs and all the nodal voltages will be directly calculated.

III. Extension to the AC Analysis

In previous section DNE has been considered for the DC analysis for sake of simplicity. Obviously, the whole algorithm of the previous section can be extended to circuits constituted by R-L-C elements fed by AC independent and voltage-controlled current sources, substituting:

- the conductance G_{ij} with the admittance $\dot{Y}_{ij}$;
- the DC current sources with AC current sources.

Equation (8) becomes:

$$\dot{\boldsymbol{D}} \cdot \overline{\boldsymbol{V}} = \overline{\boldsymbol{J}}' \qquad (9)$$

where $\dot{\boldsymbol{D}}$ is a complex diagonal matrix, $\overline{\boldsymbol{V}}$ the nodal voltages vector in AC domain and $\overline{\boldsymbol{J}}'$ the nodal currents vector in AC domain. Equation (9) represents DNE in AC domain.

[3] If the obtained node-conductance matrix is a lower triangular matrix, analogous considerations can be made.

IV. Application Example

IV.1) Example 1

Fig. 4 shows a DC circuit fed by two current sources. The independent nodes are numbered as 1,2,3.

Let us suppose: $I_{s1} = 20[A]$, $I_{s2} = 20[A]$ and $G_i = i[S] \quad \forall i = 1,2,...6$.

Applying NA, following matrix equation is obtained:

$$\begin{bmatrix} G_1+G_2+G_6 & -G_2 & -G_6 \\ -G_2 & G_2+G_3+G_4 & -G_4 \\ -G_6 & -G_4 & G_4+G_5+G_6 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} -I_{s1} \\ 0 \\ I_{s2} \end{bmatrix} \quad (10)$$

whose solution is $V_1 = -1.93[V]$, $V_2 = -0.20[V]$, $V_3 = 0.51[V]$.

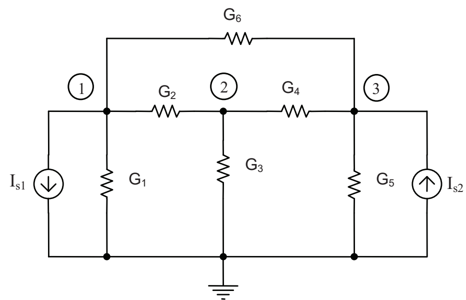

Fig. 4. DC circuit

Now, let us apply the GE according to the algorithm of section II.1) - FE. The first step provides the removal of the *1-node* from the circuit. After this step the circuit is modified as in Fig. 5, while the values of the conductances G_α, G_β, G_γ and G_δ are reported in Table 1. At the *3-node* the two current sources (the assigned one, I_{s2}, and the reported one from the *1-node*, $I_{s1} \cdot \dfrac{G_6}{G_{126}}$) have been fused in a unique current source; the minus sign takes into account that the weighted current source is going out from the node (Fig. 6).

In the following the sum of more conductances will be reported in the subscript, i.e. $G_{126} = G_1 + G_2 + G_6$.

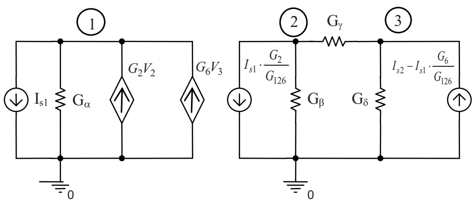

Fig. 5. Modified circuit after removing the *1-node*.

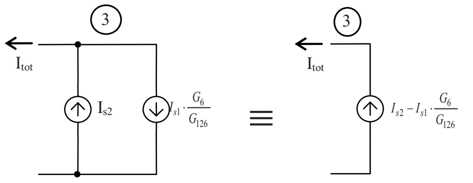

Fig. 6. More current sources in the same node are fused in only one.

TABLE 1: EXPRESSIONS AND VALUES OF G_α, G_β, G_γ and G_δ

G_α[S]	G_β [S]	G_γ [S]	G_δ [S]
G_{126}	$G_{23} - \frac{G_2 \cdot (G_2 + G_6)}{G_{126}}$	$G_4 + \frac{G_2 \cdot G_6}{G_{126}}$	$G_{56} - \frac{G_6 \cdot (G_2 + G_6)}{G_{126}}$
9	3,22	5,33	5,67

The second step provides the removal of the *2-node* from the circuit in Fig. 5. The final circuit is reported in Fig. 7, while I_η and G_η are reported in Table 2. The last SNC of Fig. 7 allows V_3 to be directly calculated. At this point the FE is finished.

Applying the algorithm of section II.2) – BS, Fig. 7 is modified as in Fig. 8 and then as in Fig. 9. Values are reported in Table 3.

Now, also BS is finished and the assigned circuit, having three independent nodes, result decoupled in three e-SNC. For each one of them the nodal voltage can be directly calculated; it results $V_3 = 0.51[V]$, $V_2 = -0.20[V]$, $V_1 = -1.93[V]$, as expected.

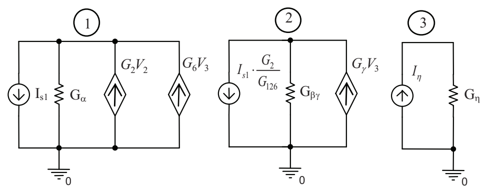

Fig. 7. Equivalent circuit after FE

TABLE 2: EXPRESSIONS AND VALUES OF Iη AND Gη

Iη [A]	Gη [S]
$I_{s2} - I_{s1} \cdot \frac{G_6}{G_{126}} - I_{s1} \cdot \frac{G_2}{G_{126}} \cdot \frac{G_\gamma}{G_{\beta\gamma}}$	$G_{\delta\gamma} - \frac{G_\gamma \cdot G_\gamma}{G_{\beta\gamma}}$
3.90	7.68

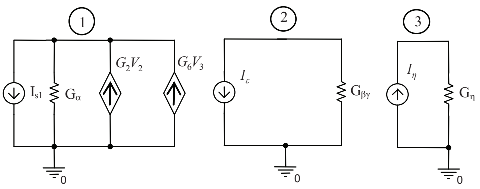

Fig. 8. Equivalent circuit after the first step of BS

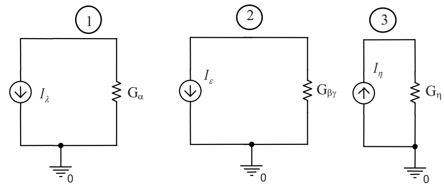

Fig. 9. Equivalent circuit when BS is finished.

TABLE 3: EXPRESSIONS AND VALUES OF I_ε AND I_λ

Iε [A]	I_λ [A]
$-I_{s1} \cdot \frac{G_2}{G_{126}} + I_\eta \cdot \frac{G_\gamma}{G_\eta}$	$-I_{s1} + I_\varepsilon \cdot \frac{G_2}{G_{\beta\gamma}} + I_\eta \cdot \frac{G_6}{G_\eta}$
-1.74	-17.34

IV.2) Example 2

Application of GE to the ladder circuits gives an important simplification. In fact, as each node is connected only to two another independent nodes, the SNC (Fig. 3) obtained at each elimination step will present only one VCCS. Moreover the conductances linking directly two independent nodes do not change during the GE process.

Fig. 10 reports a ladder DC circuit, in which six independent nodes are present. It is observed there is only one independent current source. If the node, which it is connected to, is labeled as *1-node*, in the GE process a weighted current source will appear in all the SNCs.

Otherwise, if the nodes are labeled so that the node, which the current source is connected to, results the last one, then only in the last SNC a current source appears; the other SNCs will be constituted by only one VCCS with a parallel-connected conductance, providing a great computation reduction. In Fig. 10 just this choice has been done in numbering the nodes.

Let us suppose: $I_s = 20[A]$ and $G_i = i[S] \quad \forall i = 1, 2, \ldots 11$.

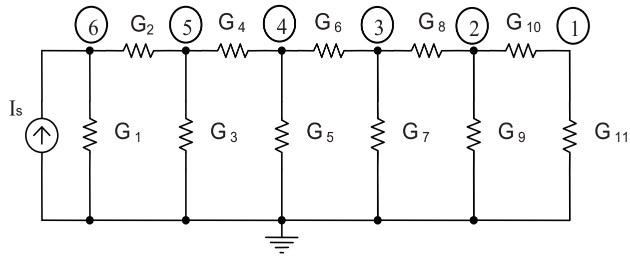

Fig. 10. Ladder circuit

The resulting matrix equation is:

$$\begin{bmatrix} G_{10}+G_{11} & -G_{10} & 0 & 0 & 0 & 0 \\ -G_{10} & G_{89}+G_{10} & -G_8 & 0 & 0 & 0 \\ 0 & -G_8 & G_{678} & -G_6 & 0 & 0 \\ 0 & 0 & -G_6 & G_{456} & -G_4 & 0 \\ 0 & 0 & 0 & -G_4 & G_{234} & -G_2 \\ 0 & 0 & 0 & 0 & -G_2 & G_{12} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ I_{s1} \end{bmatrix} \quad (10)$$

whose solution is reported in Table 4.

TABLE 4: NODAL VOLTAGES OF THE LADDER CIRCUIT.

V_1[V]	V_2[V]	V_3[V]	V_4[V]	V_5[V]	V_6[V]
0.036	0.076	0.211	0.637	2.071	8.047

Now, let us apply the rules introduced in Section II to the circuit of Fig 10. The circuit, after FE, is reported in Fig. 11, while the values of the conductances are reported in Table 5.

Now, BS is applied and circuit of Fig. 12 is obtained, whose values are reported in Table 6. Then, nodal voltages can be directly calculated by each e-SNC and the same values of Table 4 are obtained.

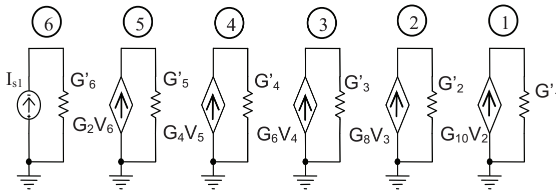

Fig. 11. Equivalent ladder circuit after FE.

TABLE 5: VALUES OF THE CONDUCTANCES IN FIG. 11

G'_6[S]	G'_5[S]	G'_4[S]	G'_3[S]	G'_2[S]	G'_1[S]
2,485	7,77	13,01	18,12	22,24	21

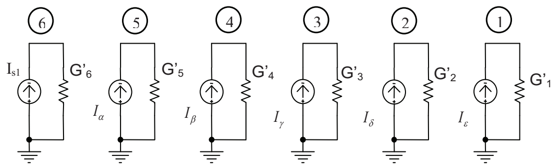

Fig. 12. Equivalent ladder circuit after BS.

TABLE 6: VALUES OF THE CURRENT SOURCES OF FIG.12

I_α [A]	I_β [A]	I_γ [A]	I_δ [A]	I_ε [A]
$I_{s1} \cdot \frac{G_2}{G'_6}$	$I_\alpha \cdot \frac{G_4}{G'_5}$	$I_\beta \cdot \frac{G_6}{G'_4}$	$I_\gamma \cdot \frac{G_8}{G'_3}$	$I_\varepsilon \cdot \frac{G_{10}}{G'_2}$
16,1	8,28	3,82	1.69	0.76

V. CONCLUSION

Applying GE to the matrix equation characteristic of an electrical circuit means, from a circuit theory point of view, to modify the assigned circuit. The forward process of GE can be interpreted as an iterative removal of the nodes from the assigned circuit. The removal of *k-node* corresponds to the definition of one-node circuit, called *standard nodal cell,* with node voltage dependent on the remaining *(n-k)* nodal voltages. Back substitution, instead, leads to elementary standard nodal cells in which no voltage-controlled current source is present.

Then, each nodal voltage can be directly evaluated by solving the related elementary cell.

Similar approach can be used when mesh analysis is applied to solve a circuit. Future work will consist in defining a structured and detailed analysis of GE for mesh analysis as here proposed for nodal analysis.

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Silvano Vergura received the MSc degree and the PhD degree in Electrical Engineering from Politecnico di Bari, Italy, in 1999 and 2003, respectively. From 2004 he is Assistant Professor in Politecnico di Bari, where he is currently teaching Electrotechnics and Circuit Simulation. His main research interests concern the monitoring of renewable energy sources. He has devoted particular attention to the energy performance analysis of photovoltaic plants by means of statistical approach. Other research areas regard the non destructive (infrared) analysis of both photovoltaic components and structure. Another research area concerns the modelling and simulation of switching circuits. Co-simulation, homotopy methods and topological techniques are the principal approaches utilized to study the transient analysis of switching circuits. He has joined to several local and national research projects as member and coordinator since 2005. He is member of the reviewer board of the International Journal of Computational Science and reviewer of IEEE-Trans. on Circuits and Systems, IEEE-Trans. on Industrial Electronics and other international journals and conferences.

Finally, he is the project head for the establishment of an academic Spin-Off, called Renew Energy (www.renewenergy.it). The mission of the enterprise is the technology transfer of the skills acquired during the last years of research activity about RES plants