The block diagram of a d.c. power supply is shown in Fig. 6.1. Since the mains input is at a relatively high voltage, a step-down transformer of appropriate turns ratio is used to convert this to a low voltage. The a.c. output from the transformer secondary is then rectified using conventional silicon rectifier diodes (see Chapter 5) to produce an unsmoothed (sometimes referred to as **pulsating d.c.**) output. This is then smoothed and filtered before being applied to a circuit which will **regulate** (or **stabilize**) the output voltage so that it remains relatively constant in spite of variations in both load current and incoming mains voltage. Fig. 6.2 shows how some of the electronic components that we have already met can be used in the realization of the block diagram in Fig. 6.1. The iron-cored step-down transformer feeds a rectifier arrangement (often based on a bridge circuit). The output of the rectifier is then applied to a high-value **reservoir** capacitor. This capacitor stores a considerable amount of charge and is being constantly topped-up by the rectifier arrangement. The capacitor also helps to smooth out the voltage pulses produced by the rectifier. Finally, a stabilizing circuit (often based on a **series transistor regulator** and a zener diode **voltage reference**) provides a constant output voltage. We shall now examine each stage of this arrangement in turn, building up to some complete power supply circuits at the end of the chapter.

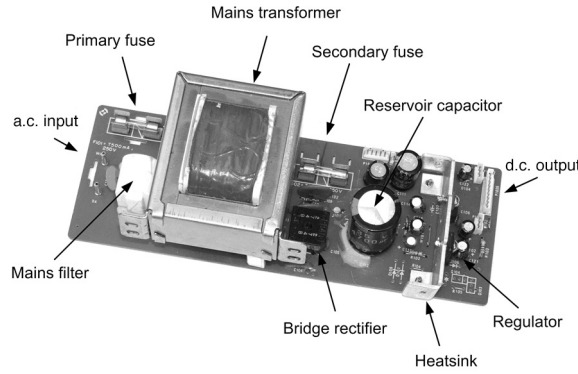


**Figure 6.3** A simple d.c. power supply

## Rectifiers

Semiconductor diodes (see Chapter 5) are commonly used to convert alternating current (a.c.) to direct current (d.c), in which case they are referred to as **rectifiers**. The simplest form of rectifier circuit makes use of a single diode and, since it operates on only either positive or negative half-cycles of the supply, it is known as a **half-wave** rectifier.

Fig. 6.4 shows a simple half-wave rectifier circuit. Mains voltage (220 to 240 V) is applied to the primary of a step-down transformer (T1). The secondary of T1 steps down the 240 V r.m.s. to 12 V r.m.s. (the turns ratio of T1 will thus

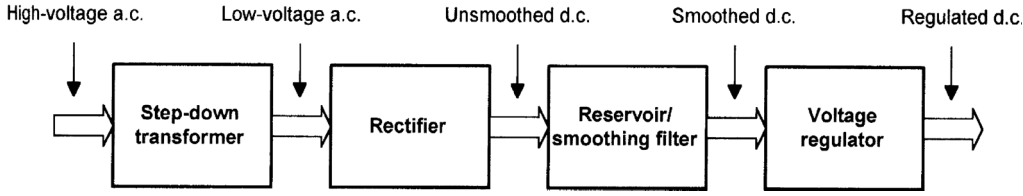


**Figure 6.1** Block diagram of a d.c. power supply

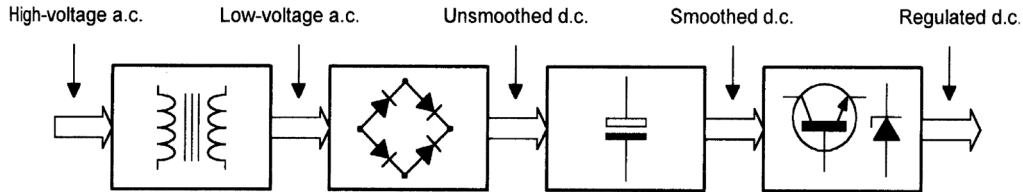


**Figure 6.2** Block diagram of a d.c. power supply showing principal components

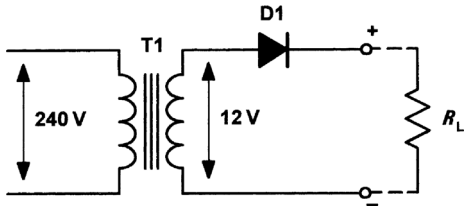


**Figure 6.4** A simple half-wave rectifier circuit

be 240/12 or 20:1). Diode D1 will only allow the current to flow in the direction shown (i.e. from cathode to anode). D1 will be forward biased during each positive half-cycle (relative to common) and will effectively behave like a closed switch. When the circuit current tries to flow in the opposite direction, the voltage bias across the diode will be reversed, causing the diode to act like an open switch (see Figs 6.5(a) and 6.5(b), respectively).

The switching action of D1 results in a pulsating output voltage which is developed across the load resistor ($R_L$). Since the mains supply is at 50 Hz, the pulses of voltage developed across $R_L$ will also be at 50 Hz even if only half the a.c. cycle is present. During the positive half-cycle, the diode will drop the 0.6 V to 0.7 V forward threshold voltage normally associated with silicon diodes. However, during the negative half-cycle the peak a.c. voltage will be dropped across D1 when it is reverse biased. This is an important consideration when selecting a diode for a particular application. Assuming that the secondary of T1 provides 12 V r.m.s., the peak voltage output from the transformer's secondary winding will be given by:

$$V_{pk} = 1.414 \times V_{r.m.s.} = 1.414 \times 12 \text{ V} = 16.97 \text{ V}$$

The peak voltage applied to D1 will thus be approximately 17 V. The negative half-cycles are blocked by D1 and thus only the positive half-cycles appear across $R_L$. Note, however, that the actual peak voltage across $R_L$ will be the 17 V positive peak being supplied from the secondary on T1, *minus* the 0.7 V forward threshold voltage dropped by D1. In other words, positive half-cycle pulses having a peak amplitude of 16.3 V will appear across $R_L$.

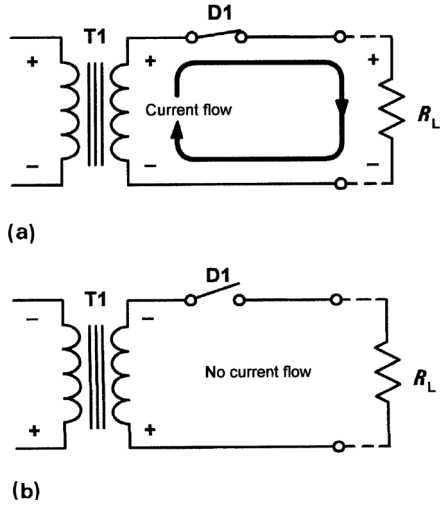


**Figure 6.5** (a) Half-wave rectifier circuit with D1 conducting (positive-going half-cycles of secondary voltage); (b) half-wave rectifier with D1 not conducting (negative-going half-cycles of secondary voltage)

### Example 6.1

A mains transformer having a turns ratio of 44:1 is connected to a 220 V r.m.s. mains supply. If the secondary output is applied to a half-wave rectifier, determine the peak voltage that will appear across a load.

### Solution

The r.m.s. secondary voltage will be given by:

$$V_S = V_P / 44 = 220 / 44 = 5 \text{ V}$$

The peak voltage developed after rectification will be given by:

$$V_{PK} = 1.414 \times 5 \text{ V} = 7.07 \text{ V}$$

Assuming that the diode is a silicon device with a forward voltage drop of 0.6 V, the actual peak voltage dropped across the load will be:

$$V_L = 7.07 \text{ V} - 0.6 \text{ V} = 6.47 \text{ V}$$

## Reservoir and smoothing circuits

Fig. 6.6 shows a considerable improvement to the circuit of Fig. 6.4. The capacitor, *C*1, has been added to ensure that the output voltage remains at, or near, the peak voltage even when the diode is not conducting. When the primary voltage is

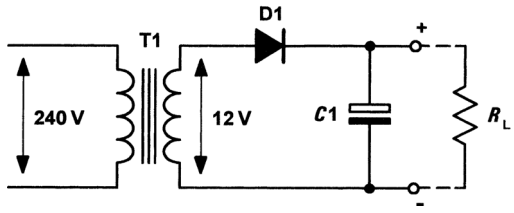


**Figure 6.6** A simple half-wave rectifier circuit with reservoir capacitor

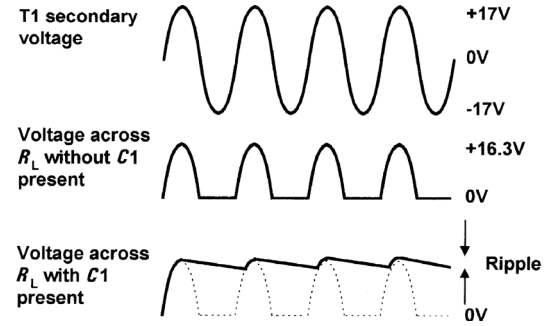


**Figure 6.7** A simple half-wave rectifier circuit with reservoir capacitor

first applied to T1, the first positive half-cycle output from the secondary will charge *C*1 to the peak value seen across $R_L$. Hence *C*1 charges to 16.3 V at the peak of the positive half-cycle. Because *C*1 and $R_L$ are in parallel, the voltage across $R_L$ will be the same as that across *C*1.

The time required for *C*1 to charge to the maximum (peak) level is determined by the charging circuit time constant (the series resistance multiplied by the capacitance value). In this circuit, the series resistance comprises the secondary winding resistance together with the forward resistance of the diode and the (minimal) resistance of the wiring and connections. Hence *C*1 charges very rapidly as soon as D1 starts to conduct.

The time required for *C*1 to discharge is, in contrast, very much greater. The discharge time constant is determined by the capacitance value and the load resistance, $R_L$. In practice, $R_L$ is very much larger than the resistance of the secondary circuit and hence *C*1 takes an appreciable time to discharge. During this time, D1 will be reverse biased and will thus be held in its non-conducting state. As a consequence, the only discharge path for *C*1 is through $R_L$.

*C*1 is referred to as a **reservoir** capacitor. It stores charge during the positive half-cycles of secondary voltage and releases it during the negative half-cycles. The circuit of Fig. 6.6 is thus able to maintain a reasonably constant output voltage across $R_L$. Even so, *C*1 will discharge by a small amount during the negative half-cycle periods from the transformer secondary.

Fig. 6.7 shows the secondary voltage waveform together with the voltage developed across $R_L$ with and without *C*1 present. This gives rise to a small variation in the d.c. output voltage (known as **ripple**). Since ripple is undesirable we must take additional precautions to reduce it. One obvious method of reducing the amplitude of the ripple is that of simply increasing the discharge time constant. This can be achieved either by increasing the value of *C*1 or by increasing the resistance value of $R_L$. In practice, however, the latter is not really an option because $R_L$ is the effective resistance of the circuit being supplied and we don't usually have the ability to change it! Increasing the value of *C*1 is a more practical alternative and very large capacitor values (often in excess of 4,700 μF) are typical.

Fig. 6.8 shows a further refinement of the simple power supply circuit. This circuit employs two additional components, *R*1 and *C*1, which act as a filter to remove the ripple. The value of *C*1 is chosen so that the component exhibits a negligible reactance at the ripple frequency (50 Hz for a half-wave rectifier or 100 Hz for a full-wave

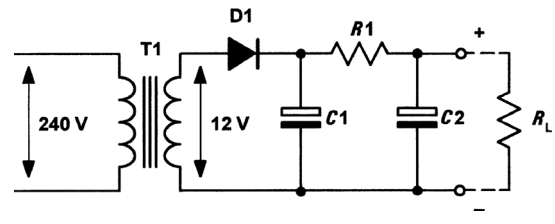


**Figure 6.8** Half-wave rectifier circuit with *R–C* smoothing filter

rectifier – see later). In effect, $R1$ and $C1$ act like a potential divider. The amount of ripple is reduced by an approximate factor equal to:

$$\frac{X_C}{\sqrt{R^2 + X_C^2}}$$

**Example 6.2**

The $R$–$C$ smoothing filter in a 50 Hz mains operated half-wave rectifier circuit consists of $R1 = 100\ \Omega$ and $C2 = 1{,}000\ \mu F$. If 1 V of ripple appears at the input of the circuit, determine the amount of ripple appearing at the output.

**Solution**

First we must determine the reactance of the capacitor, $C1$, at the ripple frequency (50 Hz):

$$X_C = \frac{1}{2\pi fC} = \frac{1}{6.28 \times 50 \times 1{,}000 \times 10^{-6}}$$
$$= \frac{1{,}000}{314} = 3.18\ \Omega$$

The amount of ripple at the output of the circuit (i.e. appearing across $C1$) will be given by:

$$V_{ripple} = 1 \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = 1 \times \frac{3.18}{\sqrt{100^2 + 3.18^2}}$$

From which:

$V = 0.032\ V = 32\ mV$

## Improved ripple filters

A further improvement can be achieved by using an inductor, $L1$, instead of a resistor in the smoothing circuit. This circuit also offers the advantage that the minimum d.c. voltage is dropped across the inductor (in the circuit of Fig. 6.7, the d.c. output voltage is *reduced* by an amount equal to the voltage drop across $R1$).

Fig. 6.9 shows the circuit of a half-wave power supply with an $L$–$C$ smoothing circuit. At the ripple frequency, $L1$ exhibits a high value of inductive reactance while $C1$ exhibits a low value of capacitive reactance. The combined effect is that of an attenuator which greatly reduces the amplitude of the ripple while having a negligible effect on the direct voltage.

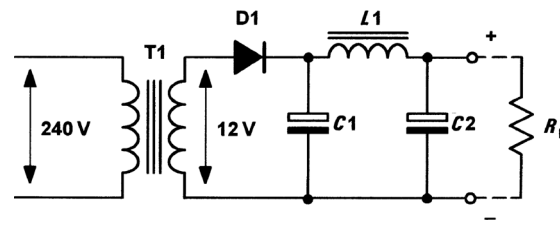


**Figure 6.9** Half-wave rectifier circuit with $L$–$C$ smoothing filter

**Example 6.3**

The $L$–$C$ smoothing filter in a 50 Hz mains operated half-wave rectifier circuit consists of $L1 = 10$ H and $C2 = 1{,}000\ \mu F$. If 1 V of ripple appears at the input of the circuit, determine the amount of ripple appearing at the output.

**Solution**

Once again, the reactance of the capacitor, $C1$, is 3.18 Ω (see Example 6.2). The reactance of $L1$ at 50 Hz can be calculated from:

$$X_L = 2\pi fL = 2 \times 3.14 \times 50 \times 10 = 3{,}140\ \Omega$$

The amount of ripple at the output of the circuit (i.e. appearing across $C1$) will be approximately given by:

$$V = 1 \times \frac{X_C}{X_C + X_L} = 1 \times \frac{3.18}{3140 + 3.18} \approx 0.001\ V$$

Hence the ripple produced by this arrangement (with 1 V of 50 Hz a.c. superimposed on the rectified input) will be a mere 1 mV. It is worth comparing this value with that obtained from the previous example!

Finally, it is important to note that the amount of ripple present at the output of a power supply will increase when the supply is loaded.

## Full-wave rectifiers

Unfortunately, the half-wave rectifier circuit is relatively inefficient as conduction takes place only on alternate half-cycles. A better rectifier arrangement would make use of both positive *and* negative half-cycles. These **full-wave rectifier** circuits offer a considerable improvement over their half-wave counterparts. They are not only more efficient but are significantly less demanding in terms of the reservoir and smoothing

components. There are two basic forms of full-wave rectifier; the bi-phase type and the bridge rectifier type.

## Bi-phase rectifier circuits

Fig. 6.10 shows a simple bi-phase rectifier circuit. Mains voltage (240 V) is applied to the primary of the step-down transformer (T1) which has two identical secondary windings, each providing 12 V r.m.s. (the turns ratio of T1 will thus be 240/12 or 20:1 for *each* secondary winding).

On positive half-cycles, point A will be positive with respect to point B. Similarly, point B will be positive with respect to point C. In this condition D1 will allow conduction (its anode will be positive with respect to its cathode) while D2 will not allow conduction (its anode will be negative with respect to its cathode). Thus D1 alone conducts on positive half-cycles.

On negative half-cycles, point C will be positive with respect to point B. Similarly, point B will be positive with respect to point A. In this condition D2 will allow conduction (its anode will be positive with respect to its cathode) while D1 will not allow conduction (its anode will be negative with respect to its cathode). Thus D2 alone conducts on negative half-cycles.

Fig. 6.11 shows the bi-phase rectifier circuit with the diodes replaced by switches. In Fig. 6.11(a) D1 is shown conducting on a positive half-cycle while in Fig. 6.11(b) D2 is shown conducting. The result is that current is routed through the load *in the same direction* on successive half-cycles.

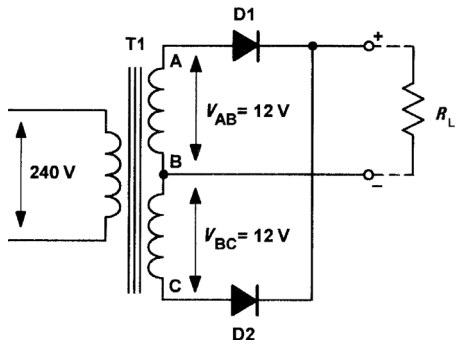


**Figure 6.10** Bi-phase rectifier circuit

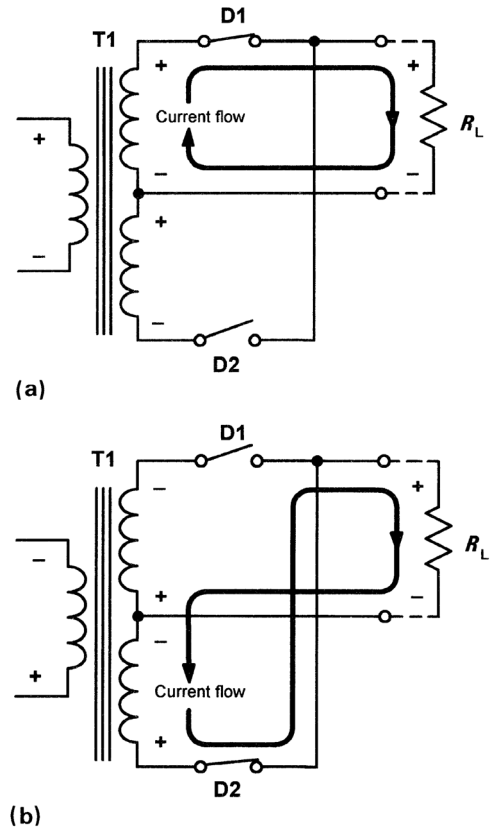


**Figure 6.11** (a) Bi-phase rectifier with D1 conducting and D2 non-conducting (b) bi-phase rectifier with D2 conducting and D1 non-conducting

Furthermore, this current is derived alternately from the two secondary windings.

As with the half-wave rectifier, the switching action of the two diodes results in a pulsating output voltage being developed across the load resistor ($R_L$). However, unlike the half-wave circuit the pulses of voltage developed across $R_L$ will occur at a frequency of 100 Hz (*not* 50 Hz). This doubling of the ripple frequency allows us to use smaller values of reservoir and smoothing capacitor to obtain the same degree of ripple reduction (recall that the reactance of a capacitor is reduced as frequency increases).

As before, the peak voltage produced by each of the secondary windings will be approximately 17 V and the peak voltage across $R_L$ will be 16.3 V

(i.e. 17 V less the 0.7 V forward threshold voltage dropped by the diodes).

Fig. 6.12 shows how a reservoir capacitor (*C*1) can be added to ensure that the output voltage remains at, or near, the peak voltage even when the diodes are not conducting. This component operates in exactly the same way as for the half-wave circuit, i.e. it charges to approximately 16.3 V at the peak of the positive half-cycle and holds the voltage at this level when the diodes are in their non-conducting states. The time required for C1 to charge to the maximum (peak) level is determined by the charging circuit time constant (the series resistance multiplied by the capacitance value). In this circuit, the series resistance comprises the secondary winding resistance together with the forward resistance of the diode and the (minimal) resistance of the wiring and connections. Hence *C*1 charges very rapidly as soon as either D1 or D2 starts to conduct. The time required for *C*1 to discharge is, in contrast, very much greater. The discharge time contrast is determined by the capacitance value and the load resistance, $R_L$. In practice, $R_L$ is very much larger than the resistance of the secondary circuit and hence *C*1 takes an appreciable time to discharge. During this time, D1 and D2 will be reverse biased and held in a non-conducting state. As a consequence, the only discharge path for *C*1 is through $R_L$. Fig. 6.13 shows voltage waveforms for the bi-phase rectifier, with and without *C*1 present. Note that the ripple frequency (100 Hz) is twice that of the half-wave circuit shown previously in Fig. 6.7.

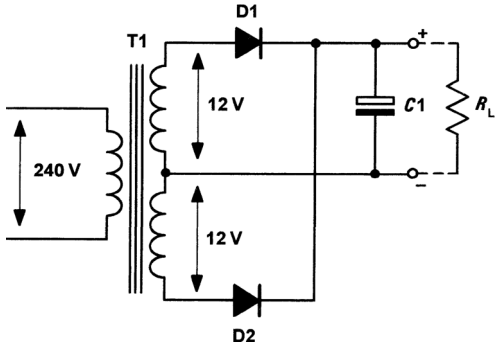


**Figure 6.12** Bi-phase rectifier with reservoir capacitor

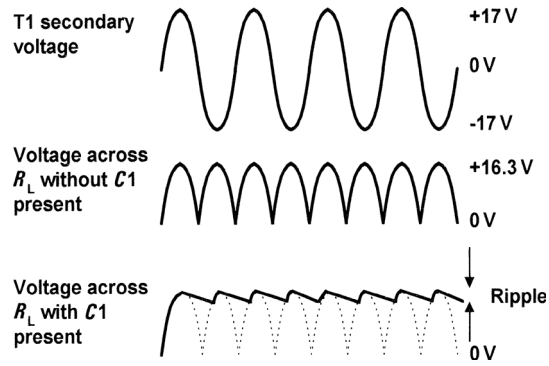


**Figure 6.13** Waveforms for the bi-phase rectifier

## Bridge rectifier circuits

An alternative to the use of the bi-phase circuit is that of using a four-diode bridge rectifier (see Fig. 6.14) in which opposite pairs of diodes conduct on alternate half-cycles. This arrangement avoids the need to have two separate secondary windings.

A full-wave bridge rectifier arrangement is shown in Fig. 6.15. Mains voltage (240 V) is applied to the primary of a step-down transformer (T1). The secondary winding provides 12 V r.m.s. (approximately 17 V peak) and has a turns ratio of 20:1, as before. On positive half-cycles, point A will be positive with respect to point B. In this condition D1 and D2 will allow conduction while D3 and D4 will not allow conduction. Conversely, on negative half-cycles, point B will be positive with respect to point A. In this condition D3 and D4 will allow conduction while D1 and D2 will not allow conduction.

Fig. 6.16 shows the bridge rectifier circuit with the diodes replaced by four switches. In Fig. 6.16(a) D1 and D2 are conducting on a positive half-cycle while in Fig. 6.16(b) D3 and

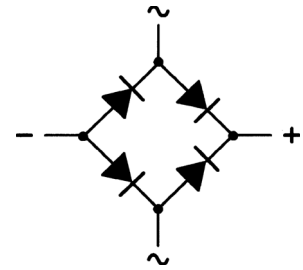


**Figure 6.14** Four diodes connected as a bridge

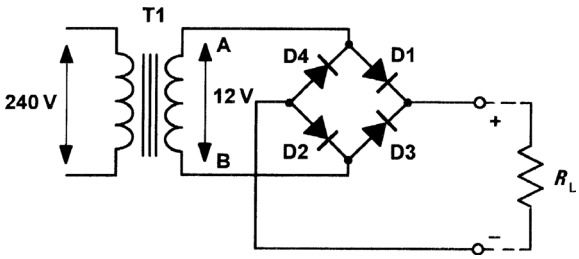


**Figure 6.15** Full-wave bridge rectifier circuit

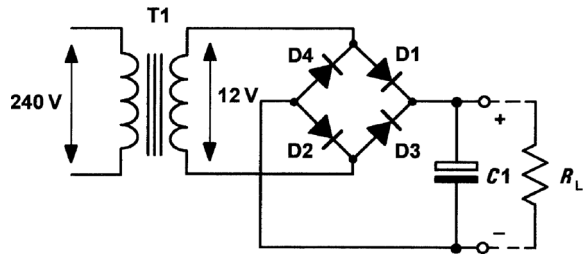


**Figure 6.17** Bridge rectifier with reservoir capacitor

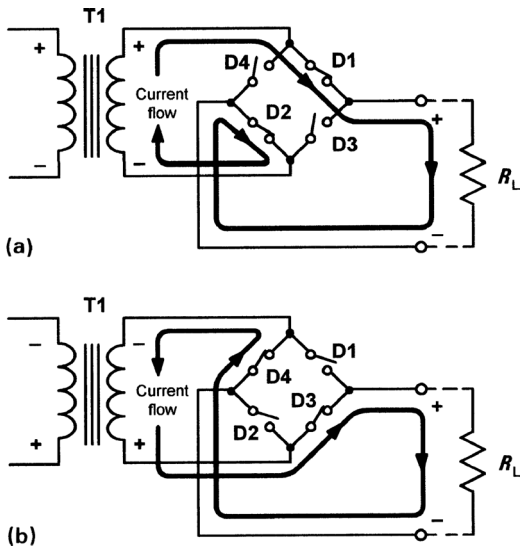


**Figure 6.16** (a) Bridge rectifier with D1 and D2 conducting, D3 and D4 non-conducting (b) bridge rectifier with D1 and D2 non-conducting, D3 and D4 conducting

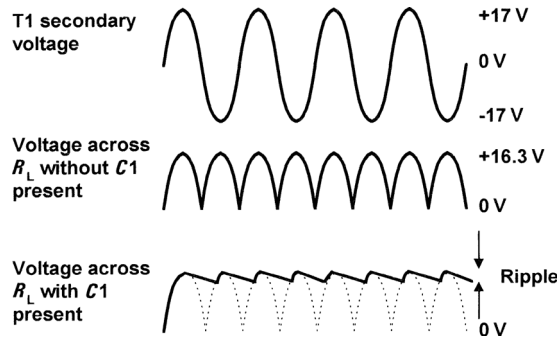


**Figure 6.18** Waveforms for the bridge rectifier

D4 are conducting. Once again, the result is that current is routed through the load *in the same direction* on successive half-cycles. As with the bi-phase rectifier, the switching action of the two diodes results in a pulsating output voltage being developed across the load resistor ($R_L$). Once again, the peak output voltage is approximately 16.3 V (i.e. 17 V less the 0.7 V forward threshold voltage).

Fig. 6.17 shows how a reservoir capacitor (*C*1) can be added to maintain the output voltage when the diodes are not conducting. This component operates in exactly the same way as for the bi-phase circuit, i.e. it charges to approximately 16.3 V at the peak of the positive half-cycle and holds the voltage at this level when the diodes are in their non-conducting states. This component operates in exactly the same way as for the bi-phase circuit and the secondary and rectified output waveforms are shown in Fig. 6.18. Once again note that the ripple frequency is twice that of the incoming a.c. supply.

Finally, *R–C* and *L–C* ripple filters can be added to bi-phase and bridge rectifier circuits in exactly the same way as those shown for the half-wave rectifier arrangement (see Figs 6.8 and 6.9).

## Voltage regulators

A simple voltage regulator is shown in Fig. 6.19. $R_S$ is included to limit the zener current to a safe value when the load is disconnected. When a load ($R_L$) is connected, the zener current ($I_Z$) will fall as current is diverted into the load resistance (it is usual to allow a minimum current of 2 mA to 5 mA in order to ensure that the diode regulates). The output voltage ($V_Z$) will remain at the zener voltage until regulation fails at the point at which the potential divider formed by $R_S$ and $R_L$

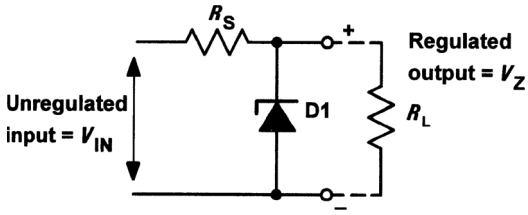


**Figure 6.19** A simple shunt zener voltage regulator

produces a lower output voltage that is less than $V_Z$. The ratio of $R_S$ to $R_L$ is thus important. At the point at which the circuit just begins to fail to regulate:

$$V_Z = V_{IN} \times \frac{R_L}{R_L + R_S}$$

where $V_{IN}$ is the unregulated input voltage. Thus the *maximum* value for $R_S$ can be calculated from:

$$R_S \text{ max.} = R_L \times \left(\frac{V_{IN}}{V_{IN}} - 1\right)$$

The power dissipated in the zener diode will be given by $P_Z = I_Z \times V_Z$, hence the minimum value for $R_S$ can be determined from the off-load condition when:

$$R_S \text{ min.} = \frac{V_{IN} - V_Z}{I_Z} = \frac{V_{IN} - V_Z}{\left(\frac{P_Z \text{ max.}}{V_Z}\right)} = \frac{(V_{IN} - V_Z) \times V_Z}{P_Z \text{ max.}}$$

Thus:

$$R_S \text{ min.} = \frac{V_{IN}V_Z - V_Z^2}{P_Z \text{ max.}}$$

where $P_Z$ max. is the maximum rated power dissipation for the zener diode.

### Example 6.4

A 5 V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5 V to a load having a resistance of 400 Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9 V.

### Solution

We shall use an arrangement similar to that shown in Fig. 6.19. First we should determine the maximum value for the series resistor, $R_S$:

$$R_S \text{ max.} = R_L \times \left(\frac{V_{IN}}{V_{IN}} - 1\right)$$

thus:

$$R_S \text{ max.} = 400 \times \left(\frac{9}{5} - 1\right) = 400 \times (1.8 - 1) = 320 \ \Omega$$

Now we need to determine the minimum value for the series resistor, $R_S$:

$$R_S \text{ min.} = \frac{V_{IN}V_Z - V_Z^2}{P_Z \text{ max.}}$$

thus:

$$R_S \text{ min.} = \frac{(9 \times 5) - 5^2}{0.5} = \frac{45 - 25}{0.5} = 40 \ \Omega$$

Hence a suitable value for $R_S$ would be 150 Ω (roughly mid-way between the two extremes).

## Output resistance and voltage regulation

In a perfect power supply, the output voltage would remain constant regardless of the current taken by the load. In practice, however, the output voltage falls as the load current increases. To account for this fact, we say that the power supply has **internal resistance** (ideally this should be zero). This internal resistance appears at the output of the supply and is defined as the change in output voltage divided by the corresponding change in output current. Hence:

$$R_{out} = \frac{\text{change in output voltage}}{\text{change in output current}} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

where $\Delta I_{out}$ represents a small change in output (load) current and $\Delta V_{out}$ represents a corresponding small change in output voltage.

The **regulation** of a power supply is given by the relationship:

$$\text{Regulation} = \frac{\text{change in output voltage}}{\text{change in line (input) voltage}} \times 100\%$$

Ideally, the value of regulation should be very small. Simple shunt zener diode regulators of the type shown in Fig. 6.19 are capable of producing values of regulation of 5% to 10%. More sophisticated circuits based on discrete components produce values of between 1% and 5% and integrated circuit regulators often provide values of 1% or less.

**Example 6.5**

The following data were obtained during a test carried out on a d.c. power supply:

**(i)** *Load test*

Output voltage (no-load) = 12 V
Output voltage (2 A load current) = 11.5 V

**(ii)** *Regulation test*

Output voltage (mains input, 220 V) = 12 V
Output voltage (mains input, 200 V) = 11.9 V

Determine (a) the equivalent output resistance of the power supply and (b) the regulation of the power supply.

**Solution**

The output resistance can be determined from the load test data:

$$R_{out} = \frac{\text{change in output voltage}}{\text{change in output current}} = \frac{12 - 11.5}{2 - 0} = 0.25\ \Omega$$

The regulation can be determined from the regulation test data:

$$\text{Regulation} = \frac{\text{change in output voltage}}{\text{change in line (input) voltage}} \times 100\%$$

thus

$$\text{Regulation} = \frac{12 - 1.9}{220 - 200} \times 100\% = \frac{0.1}{20} \times 100\% = 0.5\%$$

## Practical power supply circuits

Fig. 6.20 shows a simple power supply circuit capable of delivering an output current of up to 250 mA. The circuit uses a full-wave bridge rectifier arrangement (D1 to D4) and a simple *C–R* filter. The output voltage is regulated by the shunt-connected 12 V zener diode.

Fig. 6.21 shows an improved power supply in which a transistor is used to provide current gain and minimize the power dissipated in the zener diode (TR1 is sometimes referred to as a **series-pass transistor**). The zener diode, D5, is rated at 13 V and the output voltage will be approximately 0.7 V less than this (i.e. 13 V minus the base-emitter voltage drop associated with TR1). Hence the output voltage is about 12.3 V. The circuit is capable of delivering an output current of up to 500 mA (note that TR1 should be fitted with a small heatsink to conduct away any heat produced). Fig. 6.22 shows a variable power supply. The base voltage to the series-pass transistor is derived from a potentiometer connected across the zener diode, D5. Hence the base voltage is variable from 0 V to 13 V. The transistor requires a substantial heatsink (note that TR1's dissipation *increases* as the output voltage is reduced).

Finally, Fig. 6.23 shows a d.c. power supply based on a fixed-voltage **three-terminal integrated**

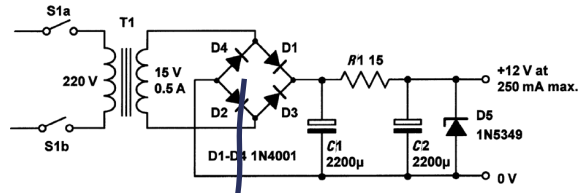


**Figure 6.20** Simple d.c. power supply with shunt zener regulated output

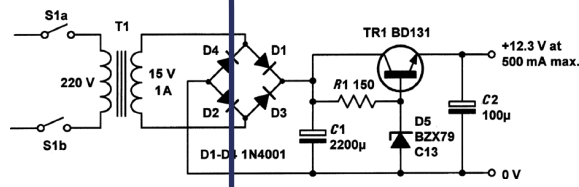


**Figure 6.21** Improved regulated d.c. power supply with series-pass transistor

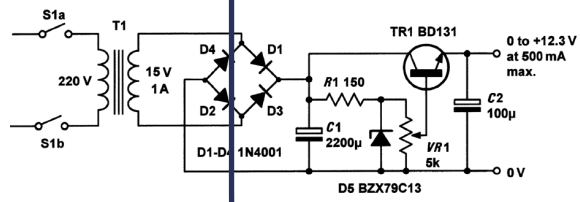


**Figure 6.22** Variable d.c. power supply

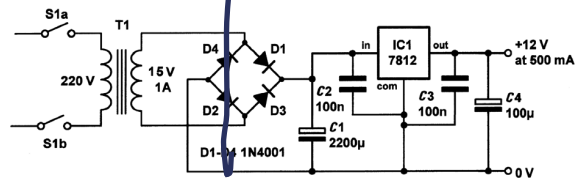


**Figure 6.23** Power supply with three-terminal IC voltage regulator

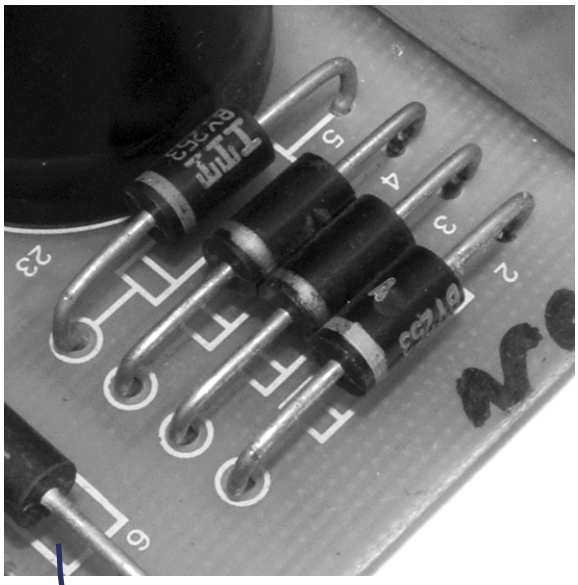

**Figure 6.24** This four-diode bridge rectifier arrangement is part of a high-voltage d.c. supply. Each BY253 diode is rated for a reverse repetitive maximum voltage ($V_{RRM}$) of 600 V, and a maximum forward current ($I_F$ max.) of 3 A

**circuit voltage regulator**. These devices are available in standard voltage and current ratings (e.g. 5 V, 12 V, 15 V at 1 A, 2 A and 5 A) and they provide excellent performance in terms of output resistance, ripple rejection and voltage regulation.

In addition, such devices usually incorporate overcurrent protection and can withstand a direct short-circuit placed across their output terminals. This is an essential feature in many practical applications!

## Voltage multipliers

By adding a second diode and capacitor, we can increase the output of the simple half-wave rectifier that we met earlier. A voltage doubler using this technique is shown in Fig. 6.25. In this arrangement C1 will charge to the positive peak secondary voltage while C2 will charge to the negative peak secondary voltage. Since the output is taken from C1 and C2 connected in series the resulting output voltage is twice that produced by one diode alone.

The voltage doubler can be extended to produce higher voltages using the cascade

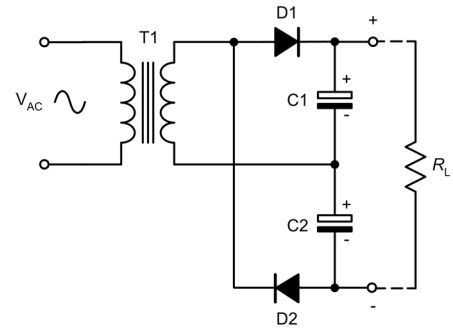


**Figure 6.25** A voltage doubler

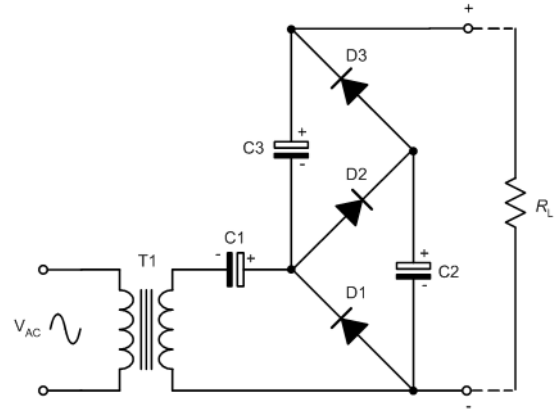


**Figure 6.26** A voltage tripler

arrangement shown in Fig. 6.26. Here C1 charges to the positive peak secondary voltage, while C2 and C3 charge to twice the positive peak secondary voltage. The result is that the output voltage is the sum of the voltages across C1 and C3 which is three times the voltage that would be produced by a single diode. The ladder arrangement shown in Fig. 6.25 can be easily extended to provide even higher voltages but the efficiency of the circuit becomes increasingly impaired and high-order voltage multipliers of this type are only suitable for providing relatively small currents.

## Switched mode power supplies

Power supplies can be divided into two principal categories, linear and non-linear types. **Linear power supplies** make use of conventional

Minimum value of series resistor for a simple shunt zener diode voltage regulator: (page 125)

$$R_S \text{ min.} = \frac{V_{IN}V_Z - V_Z^2}{P_Z \text{max.}}$$

Output resistance of a power supply: (page 125)

$$R_{out} = \frac{\text{change in output voltage}}{\text{change in output current}} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

Input (line) regulation of a power supply: (page 125)

$$\text{Regulation} = \frac{\text{change in output voltage}}{\text{change in line (input) voltage}} \times 100\%$$

## Symbols introduced in this chapter

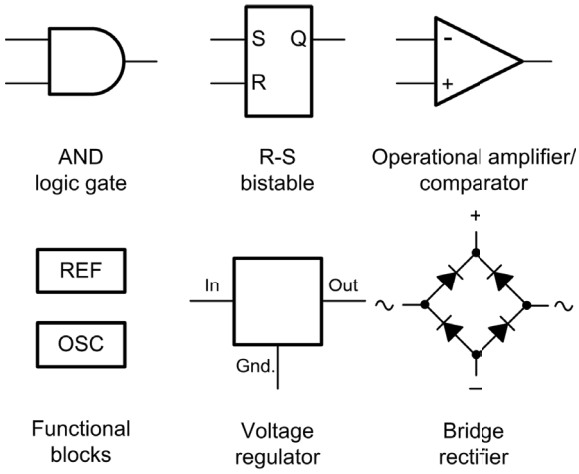


**Figure 6.36** Circuit symbols introduced in this chapter

## Problems

6.1 A half-wave rectifier is fitted with an *R–C* smoothing filter comprising $R = 200\ \Omega$ and $C = 50\ \mu F$. If 2 V of 400 Hz ripple appear at the input of the circuit, determine the amount of ripple appearing at the output.

6.2 The *L–C* smoothing filter fitted to a 50 Hz mains operated full-wave rectifier circuit consists of $L = 4$ H and $C = 500\ \mu F$. If 4 V of ripple appear at the input of the circuit, determine the amount of ripple appearing at the output.

6.3 If a 9 V zener diode is to be used in a simple shunt regulator circuit to supply a load having a nominal resistance of 300 Ω, determine the maximum value of series resistor for operation in conjunction with a supply of 15 V.

6.4 The circuit of a d.c. power supply is shown in Fig. 6.37. Determine the voltages that will appear at test points A, B and C.

6.5 In Fig. 6.37, determine the current flowing in *R*1 and the power dissipated in D5 when the circuit is operated without any load connected.

6.6 In Fig. 6.37, determine the effect of each of the following fault conditions:

(a) *R*1 open-circuit;
(b) D5 open-circuit;
(c) D5 short-circuit.

6.7 A 220 V a.c supply feeds a 20:1 step-down transformer, the secondary of which is connected to a bridge rectifier and reservoir capacitor. Determine the approximate d.c. voltage that will appear

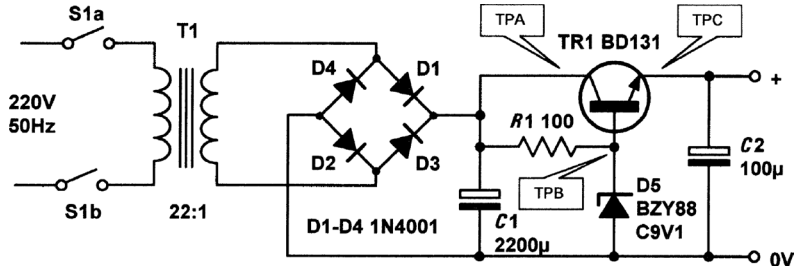


**Figure 6.37** See Questions 6.4, 6.5 and 6.6

across the reservoir capacitor under 'no-load' conditions.

6.8 The following data were obtained during a load test carried out on a d.c. power supply:

Output voltage (no-load) = 8.5 V

Output voltage (800 mA load) = 8.1 V

Determine the output resistance of the power supply and estimate the output voltage at a load current of 400 mA.

6.9 The following data were obtained during a regulation test on a d.c. power supply:

Output voltage (a.c. input: 230 V) = 15 V

Output voltage (a.c. input: 190 V) = 14.6 V

Determine the regulation of the power supply and estimate the output voltage when the input voltage is 245 V.

6.10 Fig. 6.38 shows a switching regulator circuit that produces an output of 9 V for an input of 4.5 V. What type of regulator is this? Between which pins of IC1 is the switching transistor connected? Which pin on IC1 is used to feed back a proportion of the output voltage to the internal comparator stage?

Answers to these problems appear on page 417.

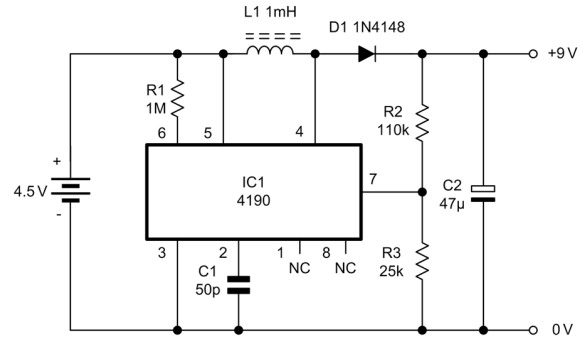


**Figure 6.38** See Question 6.10

## Types of amplifier

Many different types of amplifier are found in electronic circuits. Before we explain the operation of transistor amplifiers in detail, we shall briefly describe the main types of amplifier.

*a.c. coupled amplifiers*

In a.c. coupled amplifiers, stages are coupled together in such a way that d.c. levels are isolated and only the a.c. components of a signal are transferred from stage to stage.

*d.c. coupled amplifiers*

In d.c. (or direct) coupled amplifiers, stages are coupled together in such a way that stages are not isolated to d.c. potentials. Both a.c. and d.c. signal components are transferred from stage to stage.

*Large-signal amplifiers*

Large-signal amplifiers are designed to cater for appreciable voltage and/or current levels (typically from 1 V to 100 V or more).

*Small-signal amplifiers*

Small-signal amplifiers are designed to cater for low-level signals (normally less than 1 V and often much smaller). Small-signal amplifiers have to be specially designed to combat the effects of noise.

*Audio frequency amplifiers*

Audio frequency amplifiers operate in the band of frequencies that is normally associated with audio signals (e.g. 20 Hz to 20 kHz).

*Wideband amplifiers*

Wideband amplifiers are capable of amplifying a very wide range of frequencies, typically from a few tens of hertz to several megahertz.

*Radio frequency amplifiers*

Radio frequency amplifiers operate in the band of frequencies that is normally associated with radio signals (e.g. from 100 kHz to over 1 GHz). Note that it is desirable for amplifiers of this type to be frequency selective and thus their frequency response may be restricted to a relatively narrow band of frequencies (see Fig. 7.9 on page 139).

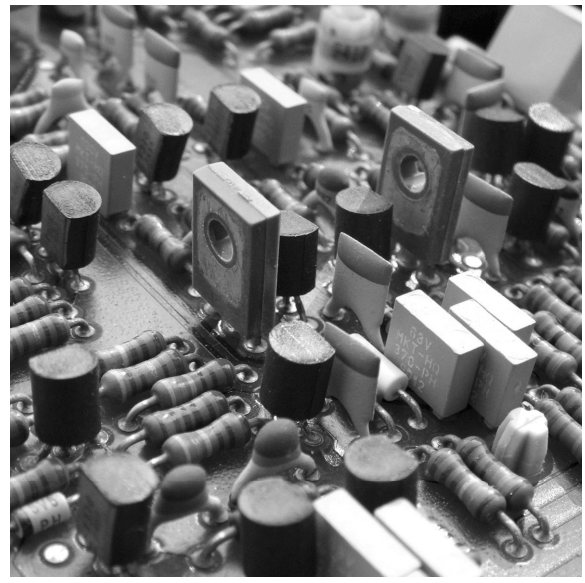

**Figure 7.1** Part of a high-gain, wideband d.c. coupled amplifier using discrete components

*Low-noise amplifiers*

Low-noise amplifiers are designed so that they contribute negligible noise (signal disturbance) to the signal being amplified. These amplifiers are usually designed for use with very small signal levels (usually less than 10 mV or so).

## Gain

One of the most important parameters of an amplifier is the amount of amplification or gain that it provides. Gain is simply the ratio of output voltage to input voltage, output current to input current, or output power to input power (see Fig. 7.2). These three ratios give, respectively, the voltage gain, current gain and power gain. Thus:

$$\text{Voltage gain, } A_v = \frac{V_{out}}{V_{in}}$$

$$\text{Current gain, } A_i = \frac{I_{out}}{I_{in}}$$

$$\text{Power gain, } A_p = \frac{P_{out}}{P_{in}}$$

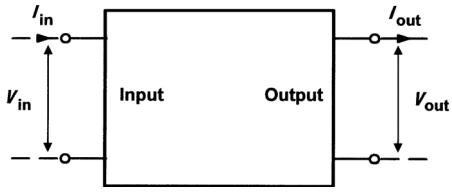


**Figure 7.2** Block diagram for an amplifier showing input and output voltages and currents

Note that, since power is the product of current and voltage ($P = I\,V$), we can infer that:

$$A_p = \frac{P_{out}}{P_{in}} = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} = \frac{I_{out}}{I_{in}} \times \frac{V_{out}}{V_{in}} = A_i \times A_v$$

### Example 7.1

An amplifier produces an output voltage of 2 V for an input of 50 mV. If the input and output currents in this condition are, respectively, 4 mA and 200 mA, determine:

**(a)** the voltage gain;
**(b)** the current gain;
**(c)** the power gain.

### Solution

**(a)** The voltage gain is calculated from:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{2\text{ V}}{50\text{ mV}} = 40$$

**(b)** The current gain is calculated from:

$$A_i = \frac{I_{out}}{I_{in}} = \frac{200\text{ mA}}{4\text{ mA}} = 50$$

**(c)** The power gain is calculated from:

$$A_p = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} = \frac{200\text{ mA} \times 2\text{ V}}{4\text{ mA} \times 50\text{ mV}} = \frac{0.4\text{ W}}{200\ \mu\text{W}} = 2{,}000$$

Note that the same result is obtained from:

$$A_p = A_i \times A_v = 50 \times 40 = 2{,}000$$

## Class of operation

An important requirement of most amplifiers is that the output signal should be a faithful copy of the input signal, albeit somewhat larger in amplitude. Other types of amplifier are non-linear, in which case their input and output waveforms will not necessarily be similar. In practice, the degree of **linearity** provided by an amplifier can be affected by a number of factors including the amount of bias applied (see later) and the amplitude of the input signal.

It is also worth noting that a linear amplifier will become non-linear when the applied input signal exceeds a threshold value. Beyond this value the amplifier is said to be **overdriven** and the output will become increasingly distorted if the input signal is further increased.

Amplifiers are usually designed to be operated with a particular value of bias supplied to the active devices (i.e. transistors). For linear operation, the active device(s) must be operated in the linear part of their **transfer characteristic** ($V_{out}$ plotted against $V_{in}$). In Fig. 7.3 the input and output signals for an amplifier are operating in linear mode. This form of operation is known as **Class A** and the **bias point** is adjusted to the mid-point of the linear part of the transfer characteristic. Furthermore, current will flow in the active devices used in a Class A amplifier during a complete cycle of the signal waveform. At no time does the current fall to zero.

Fig. 7.4 shows the effect of moving the bias point down the transfer characteristic and, at the same time, increasing the amplitude of the input signal. From this, you should notice that the extreme negative portion of the output signal has become distorted. This effect arises from the non-linearity of the transfer characteristic that occurs near the origin (i.e. the zero point). Despite the obvious

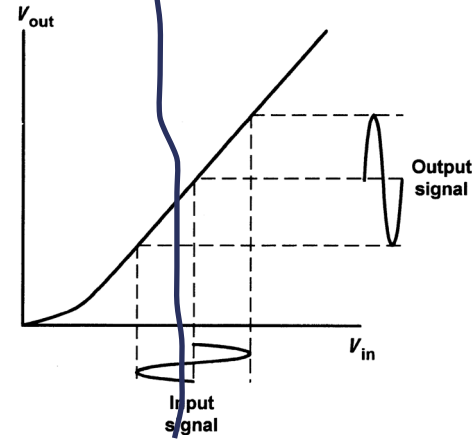


**Figure 7.3** Class A (linear) operation

**Table 7.1** Classes of operation

| Class of operation | Bias point | Conduction angle (typical) | Efficiency (typical) | Application |
|---|---|---|---|---|
| A | Mid-point | 360° | 5% to 20% | Linear audio amplifiers |
| AB | Projected cut-off | 210° | 20% to 40% | Push–pull audio amplifiers |
| B | At cut-off | 180° | 40% to 70% | Push–pull audio amplifiers |
| C | Beyond cut-off | 120° | 70% to 90% | Radio frequency power amplifiers |

and its inherent flywheel action will produce a sinusoidal output waveform. This mode of operation is only used in RF power amplifiers that must operate at very high levels of efficiency. Table 7.1 summarizes the classes of operation used in amplifiers.

## Input and output resistance

Input resistance is the ratio of input voltage to input current and it is expressed in ohms. The input of an amplifier is normally purely resistive (i.e. any reactive component is negligible) in the middle of its working frequency range (i.e. the **mid-band**). In some cases, the reactance of the input may become appreciable (e.g. if a large value of stray capacitance appears in parallel with the input resistance). In such cases we would refer to **input impedance** rather than input resistance.

Output resistance is the ratio of open-circuit output voltage to short-circuit output current and is measured in ohms. Note that this resistance is internal to the amplifier and should not be confused with the resistance of a load connected externally.

As with input resistance, the output of an amplifier is normally purely resistive and we can safely ignore any reactive component. If this is not the case, we would once again need to refer to **output impedance** rather than output resistance.

Fig. 7.8 shows how the input and output resistances are 'seen' looking into the input and output terminals, respectively. We shall be returning to this equivalent circuit a little later in this chapter. Finally, it's important to note that, although these resistances are meaningful in terms of the signals present, they cannot be measured using a conventional meter!

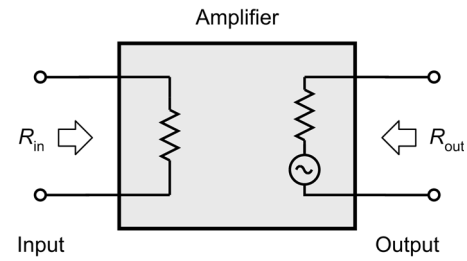


**Figure 7.8** Input and output resistances 'seen' looking into the input and output terminals, respectively

## Frequency response

The frequency response characteristics for various types of amplifier are shown in Fig. 7.9. Note that, for response curves of this type, frequency is almost invariably plotted on a **logarithmic scale**.

The frequency response of an amplifier is usually specified in terms of the upper and lower **cut-off frequencies** of the amplifier. These frequencies are those at which the output power has dropped to 50% (otherwise known as the **–3 dB points**) or where the voltage gain has dropped to 70.7% of its mid-band value.

Figs 7.10 and 7.11, respectively, show how the bandwidth can be expressed in terms of either power or voltage (the cut-off frequencies, $f_1$ and $f_2$, and bandwidth are identical).

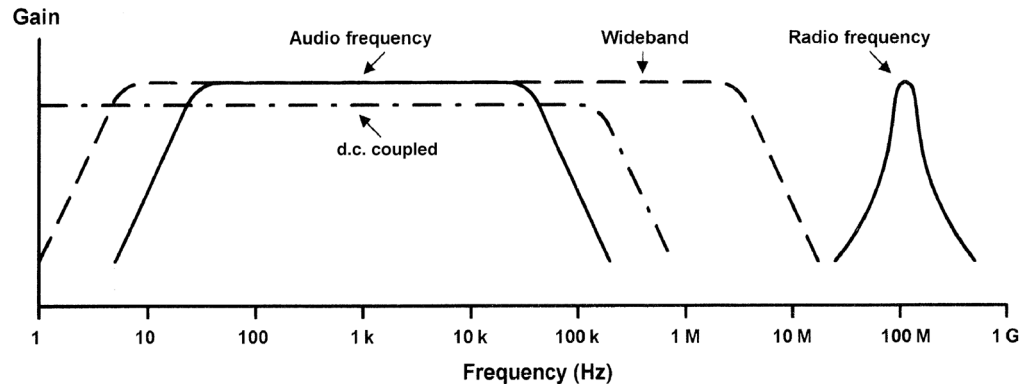


**Figure 7.9** Frequency response and bandwidth (output power plotted against frequency)

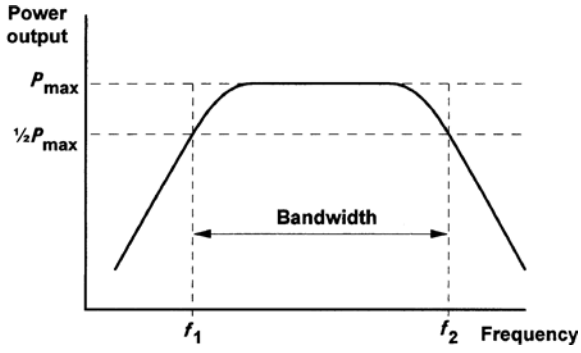


**Figure 7.10** Frequency response and bandwidth (output power plotted against frequency)

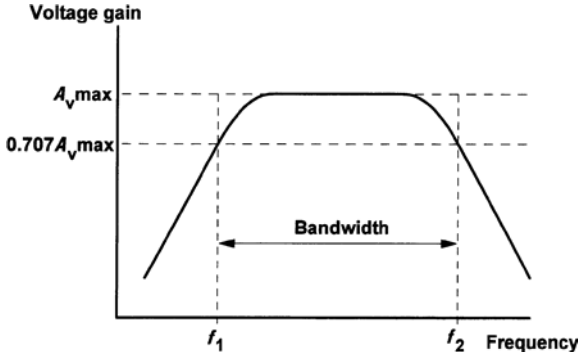


**Figure 7.11** Frequency response and bandwidth (output voltage plotted against frequency)

### Example 7.2

Determine the mid-band voltage gain and upper and lower cut-off frequencies for the amplifier whose frequency response is shown in Fig. 7.12.

### Solution

The mid-band voltage gain corresponds with the flat part of the frequency response characteristic. At that point the voltage gain reaches a maximum of 35 (see Fig. 7.12).

The voltage gain at the two cut-off frequencies can be calculated from:

$$A_v \text{ cut-off} = 0.707 \times A_v \text{ max} = 0.707 \times 35 = 24.7$$

This value of gain intercepts the frequency response graph at $f_1 = 57$ Hz and $f_2 = 590$ kHz (see Fig. 7.12).

## Bandwidth

The bandwidth of an amplifier is usually taken as the difference between the upper and lower cut-off frequencies (i.e. $f_2 - f_1$ in Figs 7.10 and 7.11). The bandwidth of an amplifier must be sufficient to accommodate the range of frequencies present within the signals that it is to be presented with. Many signals contain **harmonic** components (i.e. signals at $2f$, $3f$, $4f$, etc. where $f$ is the frequency of the **fundamental** signal). To reproduce a square wave, for example, requires an amplifier with a very wide bandwidth (note that a square wave comprises an infinite series of harmonics). Clearly it is not possible to *perfectly* reproduce such a wave, but it does explain why it can be desirable for an amplifier's bandwidth to greatly exceed the highest signal frequency that it is required to handle!

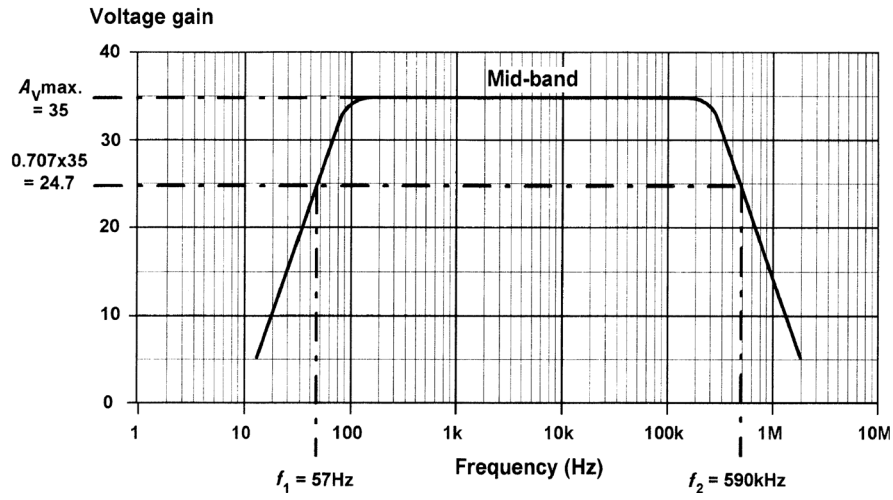


**Figure 7.12** See Example 7.2

## Phase shift

Phase shift is the phase angle between the input and output signal voltages measured in degrees. The measurement is usually carried out in the mid-band where, for most amplifiers, the phase shift remains relatively constant. Note also that conventional single-stage transistor amplifiers provide phase shifts of either 180° or 360°.

## Negative feedback

Many practical amplifiers use negative feedback in order to precisely control the gain, reduce distortion and improve bandwidth. The gain can be reduced to a manageable value by feeding back a small proportion of the output. The amount of feedback determines the overall (or **closed-loop**) gain. Because this form of feedback has the effect of reducing the overall gain of the circuit, this form of feedback is known as **negative feedback**. An alternative form of feedback, where the output is fed back in such a way as to reinforce the input (rather than to subtract from it) is known as **positive feedback**. This form of feedback is used in oscillator circuits (see Chapter 9).

Fig. 7.13 shows the block diagram of an amplifier stage with negative feedback applied. In this circuit, the proportion of the output voltage fed back to the input is given by β and the overall voltage gain will be given by:

$$\text{Overall gain, } G = \frac{V_{out}}{V_{in}}$$

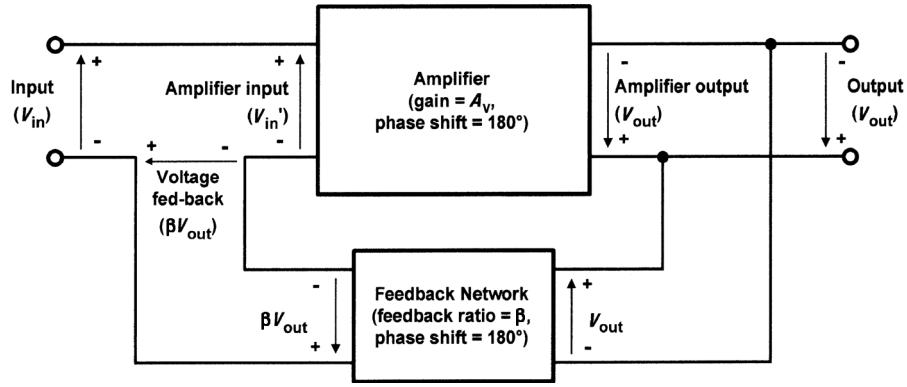


**Figure 7.13** Amplifier with negative feedback applied

Now $V_{in}' = V_{in} - \beta V_{out}$ (by applying Kirchhoff's Voltage Law) (note that the amplifier's input voltage has been *reduced* by applying negative feedback) thus:

$$V_{in} = V_{in}' + \beta V_{out}$$

and

$V_{out} = A_v \times V_{in}$ (note that $A_v$ is the **internal gain** of the amplifier)

Hence:

$$\text{Overall gain, } G = \frac{A_v \times V'_{in}}{V'_{in} + \beta V_{out}} = \frac{A_v \times V'_{in}}{V'_{in} + \beta\left(A_v \times V'_{in}\right)}$$

Thus:

$$G = \frac{A_v}{1 + \beta A_v}$$

Hence, the overall gain with negative feedback applied will be less than the gain without feedback. Furthermore, if $A_v$ is very large (as is the case with an operational amplifier – see Chapter 8) the overall gain with negative feedback applied will be given by:

$G = 1/\beta$ (when $A_v$ is very large)

Note, also, that the **loop gain** of a feedback amplifier is defined as the product of $\beta$ and $A_v$.

### Example 7.3

An amplifier with negative feedback applied has an open-loop voltage gain of 50, and one-tenth of its output is fed back to the input (i.e. $\beta = 0.1$). Determine the overall voltage gain with negative feedback applied.

### Solution

With negative feedback applied the overall voltage gain will be given by:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{50}{1 + (0.1 \times 50)} = \frac{50}{6} = 8.33$$

### Example 7.4

If, in Example 7.3, the amplifier's open-loop voltage gain increases by 20%, determine the percentage increase in overall voltage gain.

### Solution

The new value of voltage gain will be given by:

$$A_v = A_v + 0.2A_v = 1.2 \times 50 = 60$$

The overall voltage gain with negative feedback will then be:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{60}{1 + (0.1 \times 60)} = \frac{60}{7} = 7.14$$

The increase in overall voltage gain, expressed as a percentage, will thus be:

$$\frac{8.57 - 8.33}{8.33} \times 100\% = 2.88\%$$

Note that this example illustrates one of the important benefits of negative feedback in stabilizing the overall gain of an amplifier stage.

### Example 7.5

An integrated circuit that produces an open-loop gain of 100 is to be used as the basis of an amplifier stage having a precise voltage gain of 20. Determine the amount of feedback required.

### Solution

Re-arranging the formula, $G = \frac{A_v}{1 + \beta A_v}$ to make $\beta$ the subject gives:

$$\beta = \frac{1}{G} - \frac{1}{A_v}$$

Thus:

$$\beta = \frac{1}{20} - \frac{1}{100} = 0.05 - 0.01 = 0.04$$

## Transistor amplifiers

Regardless of what type of transistor is employed, three basic circuit configurations are used. These three circuit configurations depend upon which one of the three transistor connections is made common to both the input and the output. In the case of bipolar transistors, the configurations are known as **common emitter**, **common collector** (or **emitter follower**) and **common base**. Where field effect transistors are used, the corresponding configurations are **common source**, **common drain** (or **source follower**) and **common gate**.

The three basic circuit configurations (Figs 7.14 to 7.19) exhibit quite different performance

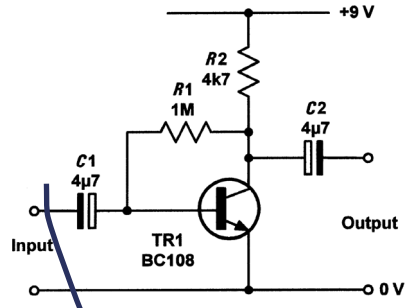


**Figure 7.38** A practical common-emitter amplifier stage

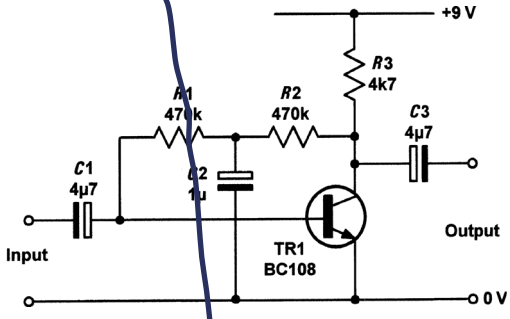


**Figure 7.39** An improved version of the common-emitter amplifier stage

Fig. 7.40 shows a practical common-emitter amplifier with bias stabilization. This stage provides a gain of 150 to well over 200 (depending upon the current gain, $h_{fe}$, of the individual transistor used). The circuit will operate with supply voltages of between 6 V and 18 V.

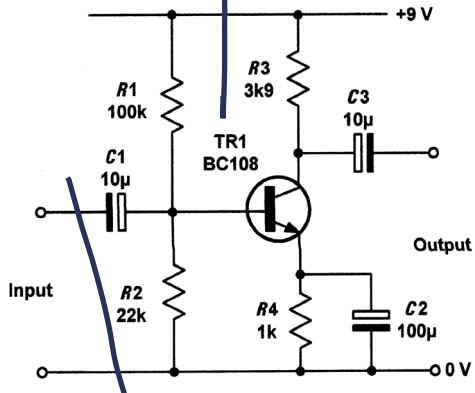


**Figure 7.40** Operating point and quiescent values shown on the load line for a bipolar transistor operating in common-emitter mode

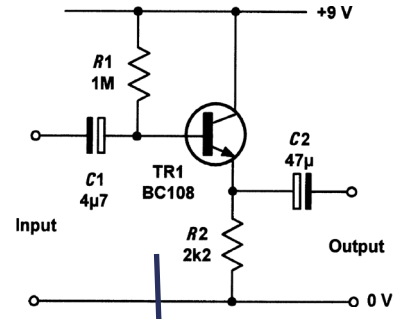


**Figure 7.41** A practical emitter-follower stage

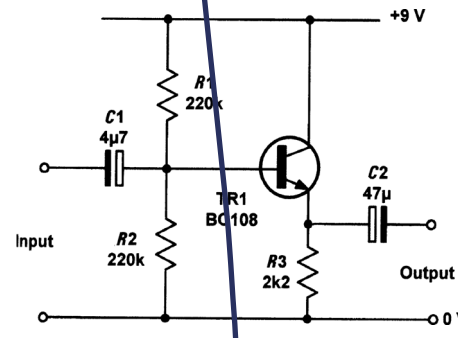


**Figure 7.42** An improved emitter-follower stage

Two practical emitter-follower circuits are shown in Figs 7.41 and 7.42. These circuits offer a voltage gain of unity (1) but are ideal for matching a high-resistance source to a low-resistance load. It is important to note that the input resistance varies with the load connected to the output of the circuit (it is typically in the range 50 kΩ to 150 kΩ). The input resistance can be calculated by multiplying $h_{fe}$ by the effective resistance of *R*2 in parallel with the load connected to the output terminals.

Fig. 7.42 is an improved version of Fig. 7.41 in which the base current is derived from the potential divider formed by *R*1 and *R*2. Note, however, that the input resistance is reduced since *R*1 and *R*2 effectively appear in parallel with the input. The input resistance of the stage is thus typically in the region of 40 kΩ to 70 kΩ.

## Multi-stage amplifiers

In order to provide sufficiently large values of gain, it is frequently necessary to use a number of interconnected stages within an amplifier. The

overall gain of an amplifier with several stages (i.e. a multi-stage amplifier) is simply the product of the individual voltage gains. Hence:

$A_V = A_{V1} \times A_{V2} \times A_{V3}$, etc.

Note, however, that the bandwidth of a multi-stage amplifier will be less than the bandwidth of each individual stage. In other words, an increase in gain can only be achieved at the expense of a reduction in bandwidth.

Signals can be coupled between the individual stages of a multi-stage amplifier using one of a number of different methods shown in Fig. 7.43.

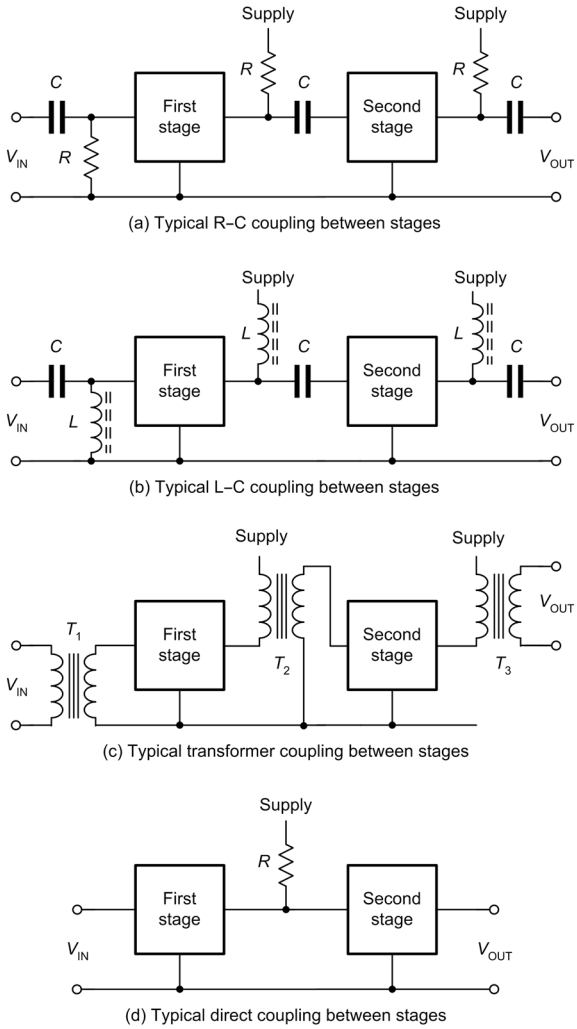


**Figure 7.43** Different methods used for interstage coupling

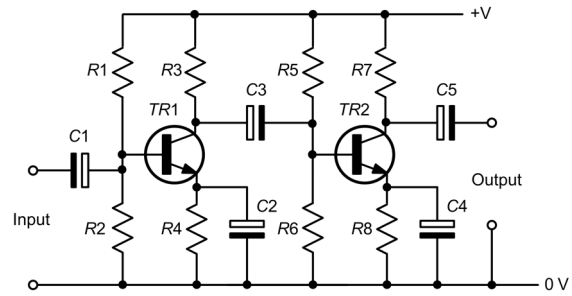


**Figure 7.44** A typical two-stage high-gain *R–C* coupled common-emitter amplifier

The most commonly used method is that of ***R–C* coupling** as shown in In Fig. 7.43(a). In this coupling method, the stages are coupled together using capacitors having a low reactance at the signal frequency and resistors (which also provide a means of connecting the supply). Fig. 7.44 shows a practical example of this coupling method.

A similar coupling method, known as ***L–C* coupling**, is shown in Fig. 7.43(b). In this method, the inductors have a high reactance at the signal frequency. This type of coupling is generally only used in RF and high-frequency amplifiers.

Two further methods, **transformer coupling** and **direct coupling,** are shown in Figs 7.43(c) and 7.43(d), respectively. The latter method is used where d.c. levels present on signals must be preserved.

## Power amplifiers

The term 'power amplifier' can be applied to any amplifer that is designed to deliver an appreciable level of power. There are several important considerations for amplifiers of this type, including the ability to deliver current (as well as voltage) to a load, and also the need to operate with a reasonable degree of efficiency (recall that conventional Class A amplifiers are inefficient).

In order to deliver sufficient current to the load, power amplifiers must have a very low value of output impedance. Thus the final stage (or **output stage**) is usually based on a device operating in emitter-follower configuration. In order to operate at a reasonable level of efficiency, the output stage must operate in Class AB or

Power gain:
(page 135)

$$A_p = \frac{P_{out}}{P_{in}}$$

Gain with negative feedback applied:
(page 141)

$$G = \frac{A_v}{1 + \beta A_v}$$

Gain (when $A_v$ is very large):
(page 141)

$$G = 1/\beta$$

Loop gain:
(page 141)

$$G_{loop} = \beta \times A_v.$$

Input resistance (common emitter):
(page 143)

$$h_{ie} = \frac{\Delta V_{be}}{\Delta I_b}$$

Forward current transfer ratio (common-emitter):
(page 143)

$$h_{fe} = \frac{\Delta I_c}{\Delta I_b}$$

Output conductance (common-emitter):
(page 143)

$$h_{oe} = \frac{\Delta I_c}{\Delta V_{ce}}$$

Reverse voltage transfer ratio (common-emitter):
(page 143)

$$h_{re} = \frac{\Delta V_{be}}{\Delta V_{ce}}$$

Voltage gain (common-emitter) assuming $h_{re}$ and $h_{oe}$ can be neglected):
(page 147)

$$A_v = \frac{h_{fe} \times R_L}{h_{ie}}$$

## Symbols introduced in this chapter

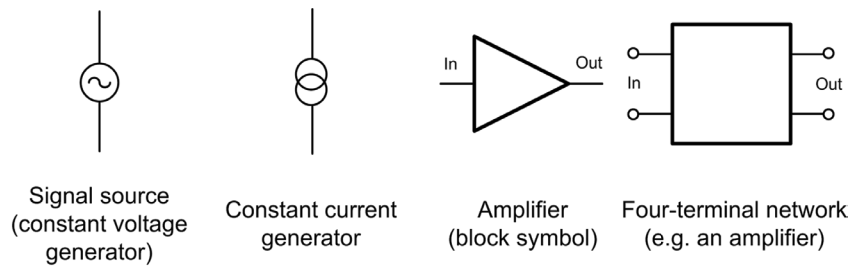


**Figure 7.52** Circuit symbols introduced in this chapter

## Problems

7.1 The following measurements were made during a test on an amplifier:

$V_{in}$ = 250 mV, $I_{in}$ = 2.5 mA,
$V_{out}$ = 10 V, $I_{out}$ = 400 mA

Determine:

(a) the voltage gain;
(b) the current gain;
(c) the power gain;
(d) the input resistance.

7.2 An amplifier has a power gain of 25 and identical input and output resistances of 600 Ω. Determine the input voltage required to produce an output of 10 V.

7.3 Determine the mid-band voltage gain and upper and lower cut-off frequencies for the amplifier whose frequency response curve is shown in Fig. 7.53. Also determine the voltage gain at frequencies of:

(a) 10 Hz
(b) 1 MHz

## Symbols and connections

The symbol for an operational amplifier is shown in Fig. 8.2. There are a few things to note about this. The device has two inputs and one output and no common connection. Furthermore, we often don't show the supply connections – it is often clearer to leave them out of the circuit altogether!

In Fig. 8.2, one of the inputs is marked '–' and the other is marked '+'. These polarity markings have nothing to do with the supply connections – they indicate the overall phase shift between each input and the output. The '+' sign indicates zero phase shift while the '–' sign indicates 180° phase shift. Since 180° phase shift produces an inverted waveform, the '–' input is often referred to as the **inverting input**. Similarly, the '+' input is known as the **non-inverting** input.

Most (but not all) operational amplifiers require a symmetrical supply (of typically ±6 V to ±15 V) which allows the output voltage to swing both positive (above 0 V) and negative (below 0 V). Fig. 8.3 shows how the supply connections would appear if we decided to include them. Note that we usually have two separate supplies; a positive supply and an equal, but opposite, negative supply. The common connection to these two supplies (i.e. the 0 V supply connection) acts as the **common rail** in our circuit. The input and output voltages are usually measured relative to this rail.

## Operational amplifier parameters

Before we take a look at some of the characteristics of 'ideal' and 'real' operational amplifiers it is important to define some of the terms and parameters that we apply to these devices.

### *Open-loop voltage gain*

The open-loop voltage gain of an operational amplifier is defined as the ratio of output voltage to input voltage measured with no feedback applied. In practice, this value is exceptionally high (typically greater than 100,000) but is liable to considerable variation from one device to another.

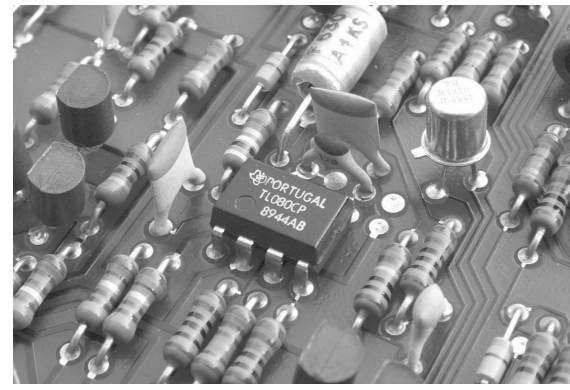


**Figure 8.1** A typical operational amplifier. This device is supplied in an eight-pin dual-in-line (DIL) package. It has a JFET input stage and produces a typical open-loop voltage gain of 200,000

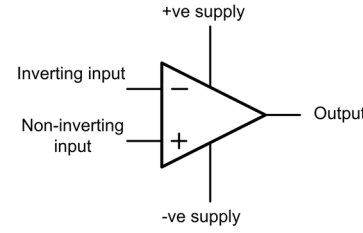


**Figure 8.2** Symbol for an operational amplifier

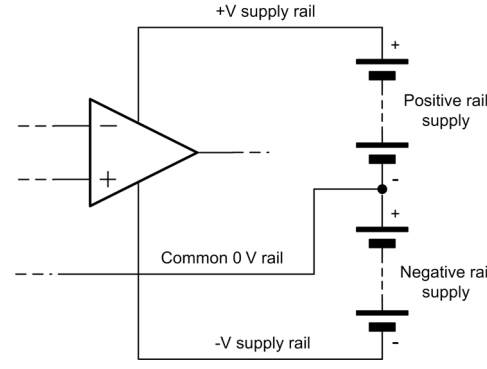


**Figure 8.3** Supply connections for an operational amplifier

Open-loop voltage gain may thus be thought of as the 'internal' voltage gain of the device, thus:

$$A_{V(OL)} = \frac{V_{OUT}}{V_{IN}}$$

where $A_{V(OL)}$ is the open-loop voltage gain, $V_{OUT}$ and $V_{IN}$ are the output and input voltages, respectively, under open-loop conditions.

In linear voltage amplifying applications, a large amount of negative feedback will normally be applied and the open-loop voltage gain can be thought of as the internal voltage gain provided by the device.

The open-loop voltage gain is often expressed in **decibels** (**dB**) rather than as a ratio. In this case:

$$A_{V(OL)} = 20\log_{10}\frac{V_{OUT}}{V_{IN}}$$

Most operational amplifiers have open-loop voltage gains of 90 dB or more.

*Closed-loop voltage gain*

The closed-loop voltage gain of an operational amplifier is defined as the ratio of output voltage to input voltage measured with a small proportion of the output fed-back to the input (i.e. with feedback applied). The effect of providing negative feedback is to reduce the loop voltage gain to a value that is both predictable and manageable. Practical closed-loop voltage gains range from one to several thousand but note that high values of voltage gain may make unacceptable restrictions on bandwidth (see later).

Closed-loop voltage gain is once again the ratio of output voltage to input voltage but with negative feedback applied, hence:

$$A_{V(CL)} = \frac{V_{OUT}}{V_{IN}}$$

where $A_{V(CL)}$ is the open-loop voltage gain, $V_{OUT}$ and $V_{IN}$ are the output and input voltages, respectively, under closed-loop conditions. The closed-loop voltage gain is normally very much less than the open-loop voltage gain.

**Example 8.1**

An operational amplifier operating with negative feedback produces an output voltage of 2 V when supplied with an input of 400 μV. Determine the value of closed-loop voltage gain.

**Solution**

Now:

$$A_{V(CL)} = \frac{V_{OUT}}{V_{IN}}$$

Thus:

$$A_{V(CL)} = \frac{2}{400\times10^{-6}} = \frac{2\times10^{6}}{400} = 5{,}000$$

Expressed in decibels (rather than as a ratio) this is:

$$A_{V(CL)} = 20\log_{10}(5{,}000) = 20\times3.7 = 74\ \text{dB}$$

*Input resistance*

The input resistance of an operational amplifier is defined as the ratio of input voltage to input current expressed in ohms. It is often expedient to assume that the input of an operational amplifier is purely resistive, though this is not the case at high frequencies where shunt capacitive reactance may become significant. The input resistance of operational amplifiers is very much dependent on the semiconductor technology employed. In practice values range from about 2 MΩ for common bipolar types to over $10^{12}$ Ω for FET and CMOS devices.

Input resistance is the ratio of input voltage to input current:

$$R_{IN} = \frac{V_{IN}}{I_{IN}}$$

where $R_{IN}$ is the input resistance (in ohms), $V_{IN}$ is the input voltage (in volts) and $I_{IN}$ is the input current (in amps). Note that we usually assume that the input of an operational amplifier is purely resistive though this may not be the case at high frequencies where shunt capacitive reactance may become significant.

The input resistance of operational amplifiers is very much dependent on the semiconductor technology employed. In practice, values range from about 2 MΩ for bipolar operational amplifiers to over $10^{12}$ Ω for CMOS devices.

**Example 8.2**

An operational amplifier has an input resistance of 2 MΩ. Determine the input current when an input voltage of 5 mV is present.

**Solution**

Now:

$$R_{IN} = \frac{V_{IN}}{I_{IN}}$$

thus

$$I_{IN} = \frac{V_{IN}}{R_{IN}} = \frac{5 \times 10^{-3}}{2 \times 10^{6}} = 2.5 \times 10^{-9}\,\text{A} = 2.5\,\text{nA}$$

*Output resistance*

The output resistance of an operational amplifier is defined as the ratio of open-circuit output voltage to short-circuit output current expressed in ohms. Typical values of output resistance range from less than 10 Ω to around 100 Ω, depending upon the configuration and amount of feedback employed.

Output resistance is the ratio of open-circuit output voltage to short-circuit output current, hence:

$$R_{OUT} = \frac{V_{OUT(OC)}}{I_{OUT(SC)}}$$

where $R_{OUT}$ is the output resistance (in ohms), $V_{OUT(OC)}$ is the open-circuit output voltage (in volts) and $I_{OUT(SC)}$ is the short-circuit output current (in amps).

*Input offset voltage*

An ideal operational amplifier would provide zero output voltage when 0 V difference is applied to its inputs. In practice, due to imperfect internal balance, there may be some small voltage present at the output. The voltage that must be applied differentially to the operational amplifier input in order to make the output voltage exactly zero is known as the input offset voltage.

Input offset voltage may be minimized by applying relatively large amounts of negative feedback or by using the offset null facility provided by a number of operational amplifier devices. Typical values of input offset voltage range from 1 mV to 15 mV. Where a.c. rather than d.c. coupling is employed, offset voltage is not normally a problem and can be happily ignored.

*Full-power bandwidth*

The full-power bandwidth for an operational amplifier is equivalent to the frequency at which the maximum undistorted peak output voltage swing falls to 0.707 of its low-frequency (d.c.) value (the sinusoidal input voltage remaining constant). Typical full-power bandwidths range from 10 kHz to over 1 MHz for some high-speed devices.

*Slew rate*

Slew rate is the rate of change of output voltage with time, when a rectangular step input voltage is applied (as shown in Fig. 8.4). The slew rate of an operational amplifier is the rate of change of output voltage with time in response to a perfect step-function input. Hence:

$$\text{Slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

where $\Delta V_{OUT}$ is the change in output voltage (in volts) and $\Delta t$ is the corresponding interval of time (in seconds).

Slew rate is measured in V/s (or V/μs) and typical values range from 0.2 V/μs to over 20 V/μs. Slew rate imposes a limitation on circuits in which large amplitude pulses rather than small amplitude sinusoidal signals are likely to be encountered.

## Operational amplifier characteristics

Having defined the parameters that we use to describe operational amplifiers we shall now

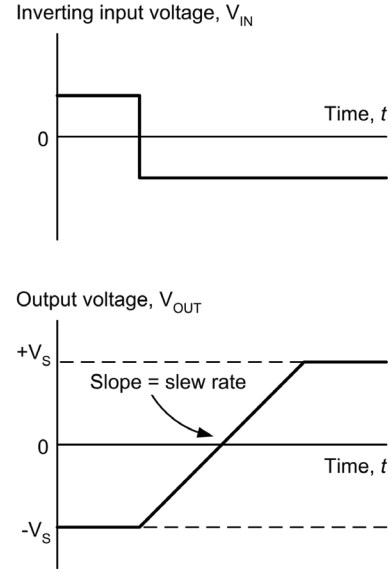


**Figure 8.4** Slew rate for an operational amplifier

consider the desirable characteristics for an 'ideal' operational amplifier. These are:

**(a)** The open-loop voltage gain should be very high (ideally infinite).
**(b)** The input resistance should be very high (ideally infinite).
**(c)** The output resistance should be very low (ideally zero).
**(d)** Full-power bandwidth should be as wide as possible.
**(e)** Slew rate should be as large as possible.
**(f)** Input offset should be as small as possible.

The characteristics of most modern integrated circuit operational amplifiers (i.e. 'real' operational amplifiers) come very close to those of an 'ideal' operational amplifier, as witnessed by the data shown in Table 8.1.

**Table 8.1** Comparison of operational amplifier parameters for 'ideal' and 'real' devices

| Parameter | Ideal | Real |
|---|---|---|
| Voltage gain | Infinite | 100,000 |
| Input resistance | Infinite | 100 MΩ |
| Output resistance | Zero | 20 Ω |
| Bandwidth | Infinite | 2 MHz |
| Slew rate | Infinite | 10 V/μs |
| Input offset | Zero | Less than 5 mV |

### Example 8.3

A perfect rectangular pulse is applied to the input of an operational amplifier. If it takes 4 μs for the output voltage to change from –5 V to +5 V, determine the slew rate of the device.

### Solution

The slew rate can be determined from:

$$\text{Slew rate} = \frac{\Delta V_{OUT}}{\Delta t} = \frac{10\text{ V}}{4\,\mu\text{s}} = 2.5\text{ V}/\mu\text{s}$$

### Example 8.4

A wideband operational amplifier has a slew rate of 15 V/μs. If the amplifier is used in a circuit with a voltage gain of 20 and a perfect step input of 100 mV is applied to its input, determine the time taken for the output to change level.

### Solution

The output voltage change will be 20 × 100 = 2,000 mV (or 2 V). Re-arranging the formula for slew rate gives:

$$\Delta t = \frac{\Delta V_{OUT}}{\text{Slew rate}} = \frac{2\text{ V}}{15\text{ V}/\mu\text{s}} = 0.133\ \mu\text{s}$$

## Operational amplifier applications

Table 8.2 shows abbreviated data for some common types of integrated circuit operational amplifier together with some typical applications.

### Example 8.5

Which of the operational amplifiers in Table 8.2 would be most suitable for each of the following applications:

**(a)** amplifying the low-level output from a piezoelectric vibration sensor
**(b)** a high-gain amplifier that can be used to faithfully amplify very small signals

**Table 8.2** Some common examples of integrated circuit operational amplifiers

| Device | Type | Open-loop voltage gain (dB) | Input bias current | Slew rate (V/μs) | Application |
|---|---|---|---|---|---|
| AD548 | Bipolar | 100 min. | 0.01 nA | 1.8 | Instrumentation amplifier |
| AD711 | FET | 100 | 25 pA | 20 | Wideband amplifier |
| CA3140 | CMOS | 100 | 5 pA | 9 | Low-noise wideband amplifier |
| LF347 | FET | 110 | 50 pA | 13 | Wideband amplifier |
| LM301 | Bipolar | 88 | 70 nA | 0.4 | General-purpose operational amplifier |
| LM348 | Bipolar | 96 | 30 nA | 0.6 | General-purpose operational amplifier |
| TL071 | FET | 106 | 30 pA | 13 | Wideband amplifier |
| 741 | Bipolar | 106 | 80 pA | 0.5 | General-purpose operational amplifier |

**(c)** a low-frequency amplifier for audio signals.

**Solution**

**(a)** AD548 (this operational amplifier is designed for use in instrumentation applications and it offers a very low input offset current which is important when the input is derived from a piezoelectric transducer).

**(b)** CA3140 (this is a low-noise operational amplifier that also offers high gain and fast slew rate).

**(c)** LM348 or LM741 (both are general-purpose operational amplifiers and are ideal for non-critical applications such as audio amplifiers).

## Gain and bandwidth

It is important to note that the product of gain and bandwidth is a constant for any particular operational amplifier. Hence, an increase in gain can only be achieved at the expense of bandwidth, and vice versa.

Fig. 8.5 shows the relationship between voltage gain and bandwidth for a typical operational amplifier (note that the axes use logarithmic rather than linear scales). The open-loop voltage gain (i.e. that obtained with no feedback applied) is 100,000 (or 100 dB) and the bandwidth obtained in this condition is a mere 10 Hz. The effect of applying increasing amounts of negative feedback (and consequently reducing the gain to a more manageable amount) is that the bandwidth increases in direct proportion.

The frequency response curves in Fig. 8.5 show the effect on the bandwidth of making the closed-loop gains equal to 10,000, 1,000, 100, and 10. Table 8.3 summarizes these results. You should also note that the (gain × bandwidth) product for this amplifier is $1 \times 10^6$ Hz (i.e. 1 MHz).

We can determine the bandwidth of the amplifier when the closed-loop voltage gain is set to 46 dB by constructing a line and noting the intercept point on the response curve. This shows that the bandwidth will be 10 kHz (note that, for this operational amplifier, the (gain × bandwidth) product is $2 \times 10^6$ Hz (or 2 MHz).

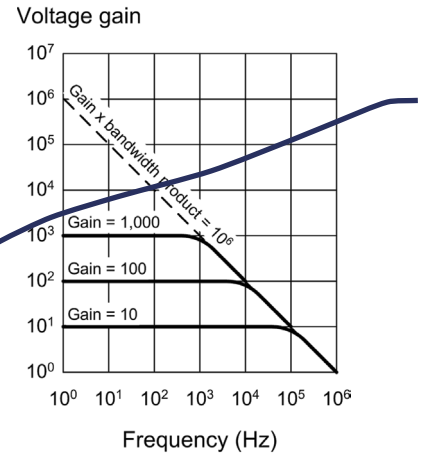


**Figure 8.5** Frequency response curves for an operational amplifier

**Table 8.3** Corresponding values of voltage gain and bandwidth for an operational amplifier with a gain × bandwidth product of $1 \times 10^6$

| Voltage gain ($A_V$) | Bandwidth |
|---|---|
| 1 | d.c. to 1 MHz |
| 10 | d.c. to 100 kHz |
| 100 | d.c. to 10 kHz |
| 1,000 | d.c. to 1 kHz |
| 10,000 | d.c. to 100 Hz |
| 100,000 | d.c. to 10 Hz |

## Inverting amplifier with feedback

Fig. 8.6 shows the circuit of an inverting amplifier with negative feedback applied. For the sake of our explanation we will assume that the operational amplifier is 'ideal'. Now consider what happens when a small positive input voltage is applied. This voltage ($V_{IN}$) produces a current ($I_{IN}$) flowing in the input resistor $R1$.

Since the operational amplifier is 'ideal' we will assume that:

**(a)** the input resistance (i.e. the resistance that appears between the inverting and non-inverting input terminals, $R_{IC}$) is infinite

**(b)** the open-loop voltage gain (i.e. the ratio of $V_{OUT}$ to $V_{IN}$ with no feedback applied) is infinite.

As a consequence of (a) and (b):

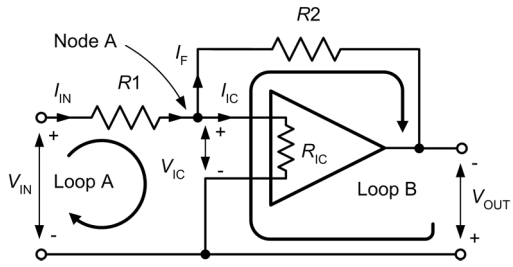


**Figure 8.6** Operational amplifier with negative feedback applied

**(i)** the voltage appearing between the inverting and non-inverting inputs ($V_{IC}$) will be zero, and

**(ii)** the current flowing into the chip ($I_{IC}$) will be zero (recall that $I_{IC} = V_{IC}/R_{IC}$ and $R_{IC}$ is infinite)

Applying Kirchhoff's Current Law at node A gives:

$$I_{IN} = I_{IC} + I_F \text{ but } I_{IC} = 0 \text{ thus } I_{IN} = I_F \quad (1)$$

(this shows that the current in the feedback resistor, $R2$, is the same as the input current, $I_{IN}$).

Applying Kirchhoff's Voltage Law to loop A gives:

$$V_{IN} = (I_{IN} \times R1) + V_{IC}$$

$$\text{but } V_{IC} = 0 \text{ thus } V_{IN} = I_{IN} \times R1 \quad (2)$$

Using Kirchhoff's Voltage Law in loop B gives:

$$V_{OUT} = -V_{IC} + (I_F \times R2)$$

$$\text{but } V_{IC} = 0 \text{ thus } V_{OUT} = I_F \times R2 \quad (3)$$

Combining (1) and (3) gives:

$$V_{OUT} = I_{IN} \times R2 \quad (4)$$

The voltage gain of the stage is given by:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (5)$$

Combining (4) and (2) with (5) gives:

$$A_v = \frac{I_{IN} \times R2}{I_{IN} \times R1} = \frac{R2}{R1}$$

To preserve symmetry and minimize offset voltage, a third resistor is often included in series with the non-inverting input. The value of this resistor should be equivalent to the parallel combination of $R1$ and $R2$. Hence:

$$R3 = \frac{R1 \times R2}{R1 + R2}$$

From this point onwards (and to help you remember the function of the resistors) we shall refer to the input resistance as $R_{IN}$ and the feedback resistance as $R_F$ (instead of the more general and less meaningful $R1$ and $R2$, respectively).

## Operational amplifier configurations

The three basic configurations for operational voltage amplifiers, together with the expressions for their voltage gain, are shown in Fig. 8.7. Supply rails have been omitted from these diagrams for clarity but are assumed to be symmetrical about 0 V.

All of the amplifier circuits described previously have used direct coupling and thus have frequency response characteristics that extend to d.c. This, of course, is undesirable for many applications, particularly where a wanted a.c. signal may be superimposed on an unwanted d.c. voltage level or when the bandwidth of the amplifier greatly exceeds that of the signal that it is required to amplify. In such cases, capacitors of appropriate value may be inserted in series with the input resistor, $R_{IN}$, and in parallel with the feedback resistor, $R_F$, as shown in Fig. 8.8.

The value of the input and feedback capacitors, $C_{IN}$ and $C_F$ respectively, are chosen so as to roll-off the frequency response of the amplifier at the desired lower and upper cut-off frequencies, respectively. The effect of these two capacitors on an operational amplifier's frequency response is shown in Fig. 8.9.

By selecting appropriate values of capacitor, the frequency response of an inverting operational voltage amplifier may be very easily tailored to suit a particular set of requirements.

The lower cut-off frequency is determined by the value of the input capacitance, $C_{IN}$, and input resistance, $R_{IN}$. The lower cut-off frequency is given by:

$$f_1 = \frac{1}{2\pi C_{IN} R_{IN}} = \frac{0.159}{C_{IN} R_{IN}}$$

where $f_1$ is the lower cut-off frequency in hertz, $C_{IN}$ is in farads and $R_{IN}$ is in ohms.

Provided the upper frequency response it not limited by the gain × bandwidth product, the

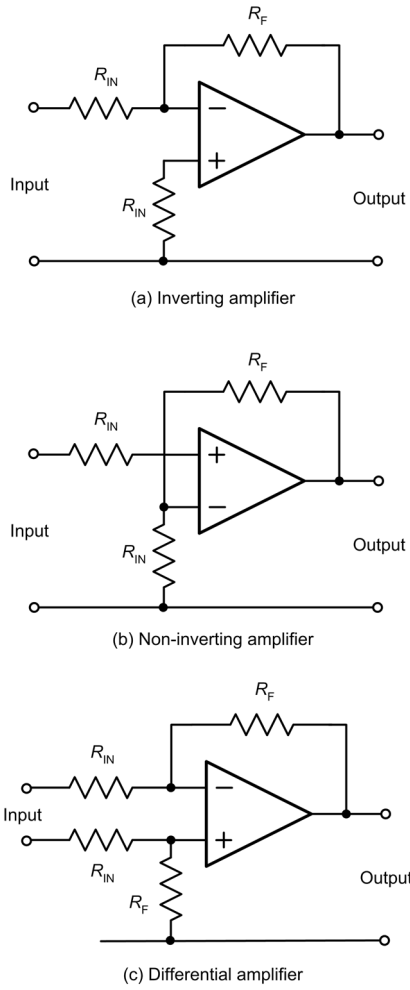


**Figure 8.7** The three basic configurations for operational voltage amplifiers

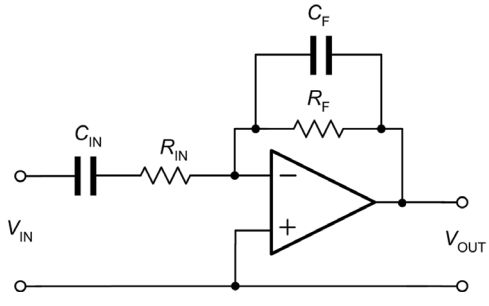


**Figure 8.8** Adding capacitors to modify the frequency response of an inverting operational amplifier

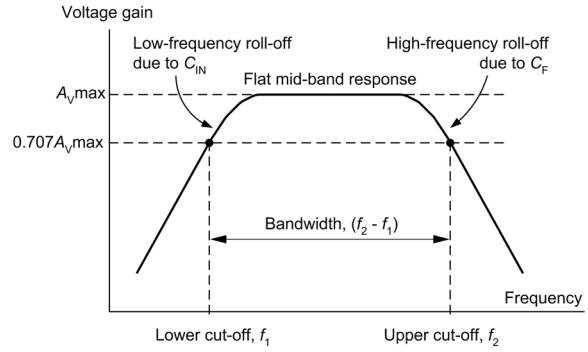


**Figure 8.9** Effect of adding capacitors, $C_{IN}$ and $C_F$, to modify the frequency response of an operational amplifier

upper cut-off frequency will be determined by the feedback capacitance, $C_F$, and feedback resistance, $R_F$, such that:

$$f_2 = \frac{1}{2\pi C_F R_F} = \frac{0.159}{C_F R_F}$$

where $f_2$ is the upper cut-off frequency in hertz, $C_F$ is in farads and $R_2$ is in ohms.

### Example 8.6

An inverting operational amplifier is to operate according to the following specification:

Voltage gain = 100
Input resistance (at mid-band) = 10 kΩ
Lower cut-off frequency = 250 Hz
Upper cut-off frequency = 15 kHz

Devise a circuit to satisfy the above specification using an operational amplifier.

### Solution

To make things a little easier, we can break the problem down into manageable parts. We shall base our circuit on a single operational amplifier configured as an inverting amplifier with capacitors to define the upper and lower cut-off frequencies, as shown in Fig. 8.9.

The nominal input resistance is the same as the value for $R_{IN}$. Thus:

$R_{IN}$ = 10 kΩ

To determine the value of $R_F$ we can make use of the formula for mid-band voltage gain:

$$A_v = \frac{R2}{R1}$$

thus $R2 = A_v \times R1 = 100 \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$

To determine the value of $C_{IN}$ we will use the formula for the low-frequency cut-off:

$$f_1 = \frac{0.159}{C_{IN}R_{IN}}$$

from which:

$$C_{IN} = \frac{0.159}{f_1 R_{IN}} = \frac{0.159}{250 \times 10 \times 10^3}$$

hence:

$$C_{IN} = \frac{0.159}{2.5 \times 10^6} = 63 \times 10^{-9}\text{F} = 63\ \text{nF}$$

Finally, to determine the value of $C_F$ we will use the formula for high-frequency cut-off:

$$f_2 = \frac{0.159}{C_F R_F}$$

from which:

$$C_F = \frac{0.159}{f_2 R_{IN}} = \frac{0.159}{15 \times 10^3 \times 100 \times 10^3}$$

hence:

$$C_F = \frac{0.159}{1.5 \times 10^9} = 0.106 \times 10^{-9}\text{F} = 106\ \text{pF}$$

For most applications the nearest preferred values (68 nF for $C_{IN}$ and 100 pF for $C_F$) would be perfectly adequate. The complete circuit of the operational amplifier stage is shown in Fig. 8.10.

## Operational amplifier circuits

As well as their application as a general-purpose amplifying device, operational amplifiers have a number of other uses, including voltage followers, differentiators, integrators, comparators and summing amplifiers. We shall conclude this section by taking a brief look at each of these applications.

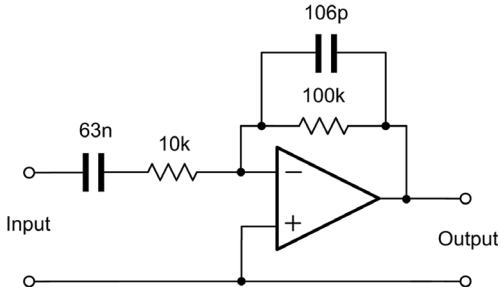


**Figure 8.10** See Example 8.6. This operational amplifier has a mid-band voltage gain of 10 over the frequency range 250 Hz to 15 kHz

### *Voltage followers*

A voltage follower using an operational amplifier is shown in Fig. 8.11. This circuit is essentially an inverting amplifier in which 100% of the output is fed back to the input. The result is an amplifier that has a voltage gain of 1 (i.e. unity), a very high input resistance and a very high output resistance. This stage is often referred to as a buffer and is used for matching a high-impedance circuit to a low-impedance circuit.

Typical input and output waveforms for a voltage follower are shown in Fig. 8.12. Notice how the input and output waveforms are both in-phase (they rise and fall together) and that they are identical in amplitude.

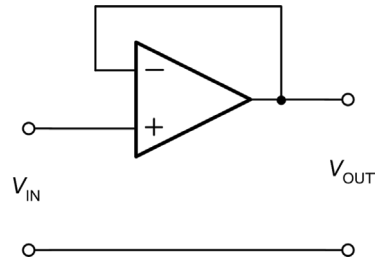


**Figure 8.11** A voltage follower

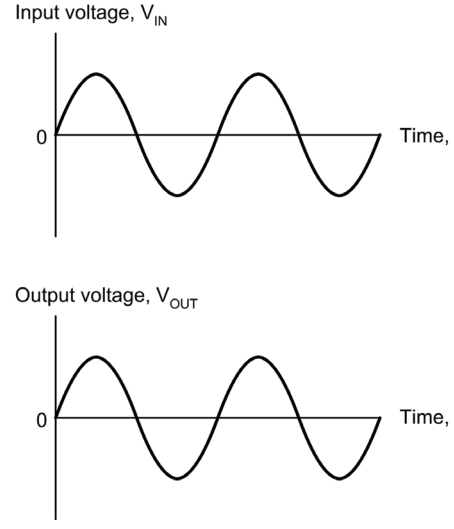


**Figure 8.12** Typical input and output waveforms for a voltage follower

*Differentiators*

A differentiator using an operational amplifier is shown in Fig. 8.13. A differentiator produces an output voltage that is equivalent to the rate of change of its input. This may sound a little complex but it simply means that if the input voltage remains constant (i.e. if it isn't changing) the output also remains constant. The faster the input voltage changes the greater will the output be. In mathematics this is equivalent to the differential function.

Typical input and output waveforms for a differentiator are shown in Fig. 8.14. Notice how the square wave input is converted to a train of short duration pulses at the output. Note also that the output waveform is inverted because the signal has been applied to the inverting input of the operational amplifier.

*Integrators*

An integrator using an operational amplifier is shown in Fig. 8.15. This circuit provides the opposite function to that of a differentiator (see earlier) in that its output is equivalent to the area under the graph of the input function rather than its rate of change. If the input voltage remains constant (and is other than 0 V) the output voltage will ramp up or down according to the polarity of the input. The longer the input voltage remains at a particular value the larger the value of output voltage (of either polarity) will be produced.

Typical input and output waveforms for an integrator are shown in Fig. 8.16. Notice how the square wave input is converted to a wave that has a triangular shape. Once again, note that the output waveform is inverted.

*Comparators*

A comparator using an operational amplifier is shown in Fig. 8.17. Since no negative feedback has been applied, this circuit uses the maximum gain of the operational amplifier. The output voltage produced by the operational amplifier will

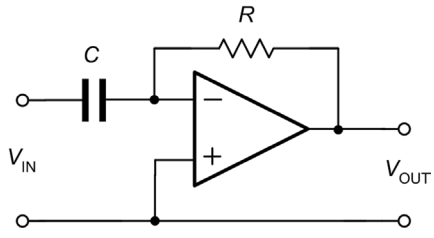


**Figure 8.13** A differentiator

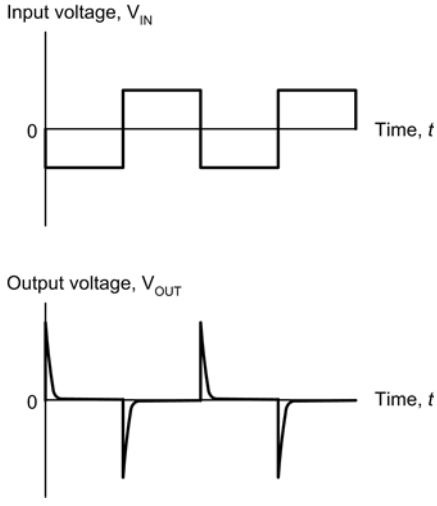


**Figure 8.14** Typical input and output waveforms for a differentiator

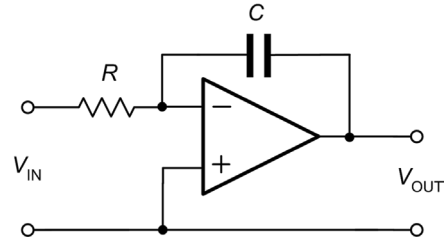


**Figure 8.15** An integrator

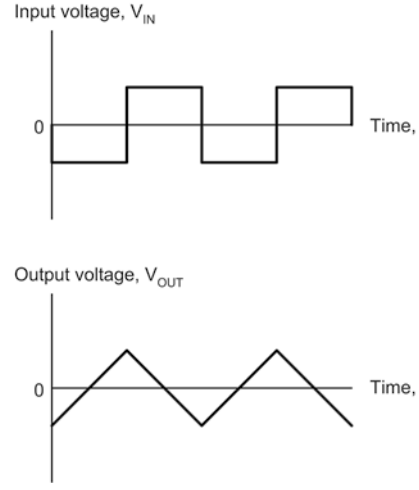


**Figure 8.16** Typical input and output waveforms for an integrator

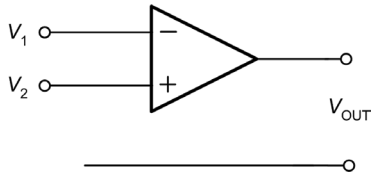


**Figure 8.17** A comparator

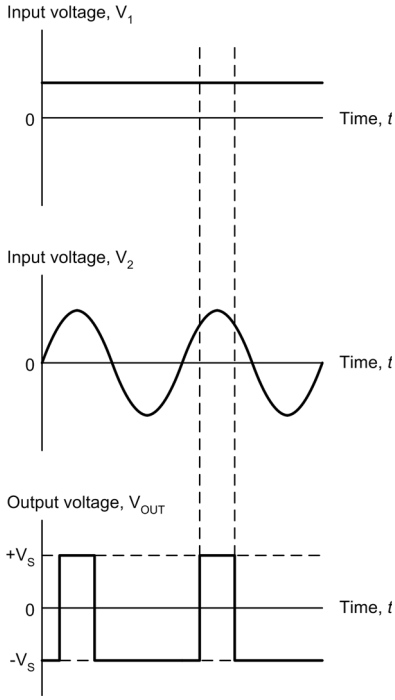


**Figure 8.18** Typical input and output waveforms for a comparator

thus rise to the maximum possible value (equal to the positive supply rail voltage) whenever the voltage present at the non-inverting input exceeds that present at the inverting input. Conversely, the output voltage produced by the operational amplifier will fall to the minimum possible value (equal to the negative supply rail voltage) whenever the voltage present at the inverting input exceeds that present at the non-inverting input.

Typical input and output waveforms for a comparator are shown in Fig. 8.18. Notice how the output is either +15 V or –15 V depending on the relative polarity of the two inputs. A typical application for a comparator is that of comparing a signal voltage with a reference voltage. The output will go high (or low) in order to signal the result of the comparison.

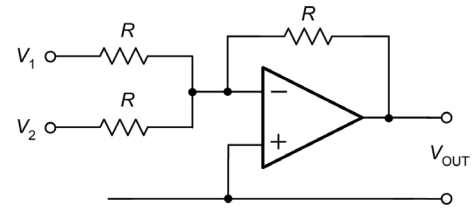


**Figure 8.19** A summing amplifier

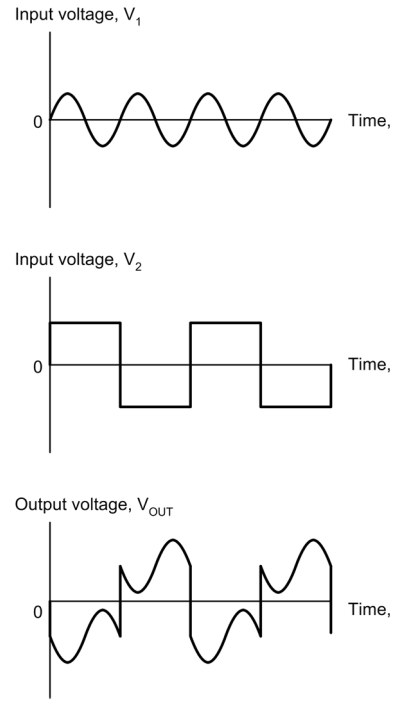


**Figure 8.20** Typical input and output waveforms for a summing amplifier

### *Summing amplifiers*

A summing amplifier using an operational amplifier is shown in Fig. 8.19. This circuit produces an output that is the sum of its two input voltages. However, since the operational amplifier is connected in inverting mode, the output voltage is given by:

$$V_{OUT} = -(V_1 + V_2)$$

where $V_1$ and $V_2$ are the input voltages (note that all of the resistors used in the circuit have the same value). Typical input and output waveforms for a summing amplifier are shown in Fig. 8.20. A typical application is that of 'mixing' two input signals to produce an output voltage that is the sum of the two.

## Positive feedback

In Chapter 7 we showed how negative feedback can be applied to an amplifier to form the basis of a stage which has a precisely controlled gain. An alternative form of feedback, where the output is fed back in such a way as to reinforce the input (rather than to subtract from it), is known as positive feedback.

Fig. 9.1 shows the block diagram of an amplifier stage with positive feedback applied. Note that the amplifier provides a phase shift of 180° and the feedback network provides a further 180°. Thus the overall phase shift is 0°. The overall voltage gain, *G*, is given by:

$$\text{Overall gain, } G = \frac{V_{out}}{V_{in}}$$

By applying Kirchhoff's Voltage Law

$$V_{in}' = V_{in} + \beta V_{out}$$

thus

$$V_{in} = V_{in}' - \beta V_{out}$$

and

$$V_{out} = A_v \times V_{in}$$

where *A*v is the internal gain of the amplifier. Hence:

$$\text{Overall gain, } G = \frac{A_v \times V_{in}'}{V_{in}' - \beta V_{out}} = \frac{A_v \times V_{in}'}{V_{in}' - \beta\left(A_v \times V_{in}'\right)}$$

$$\text{Thus, } G = \frac{A_v}{1 - \beta A_v}$$

Now consider what will happen when the loop gain, $\beta A_v$, approaches unity (i.e. when the loop gain is just less than 1). The denominator $(1 - \beta A_v)$ will become close to zero. This will have the effect of *increasing* the overall gain, i.e. the overall gain with positive feedback applied will be *greater* than the gain without feedback.

It is worth illustrating this difficult concept using some practical figures. Assume that you have an amplifier with a gain of 9 and one-tenth of the output is fed back to the input (i.e. $\beta = 0.1$). In this case the loop gain ($\beta \times A_v$) is 0.9.

With negative feedback applied (see Chapter 7) the overall voltage gain will be:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{9}{1 + (0.1 \times 9)} = \frac{9}{1 + 0.9} = \frac{9}{1.9} = 4.7$$

With positive feedback applied the overall voltage gain will be:

$$G = \frac{A_v}{1 - \beta A_v} = \frac{10}{1 - (0.1 \times 9)} = \frac{10}{1 - 0.9} = \frac{10}{0.1} = 90$$

Now assume that you have an amplifier with a gain of 10 and, once again, one-tenth of the output is fed back to the input (i.e. $\beta = 0.1$). In this example the loop gain ($\beta \times A_v$) is exactly 1.

With negative feedback applied (see Chapter 7) the overall voltage gain will be:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{10}{1 + (0.1 \times 10)} = \frac{10}{1 + 1} = \frac{10}{2} = 5$$

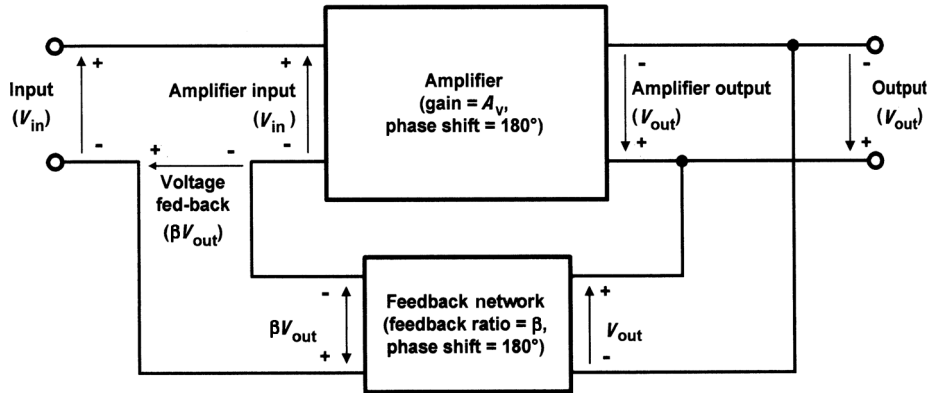


**Figure 9.1** Amplifier with positive feedback applied

With positive feedback applied the overall voltage gain will be:

$$G = \frac{A_v}{1-\beta A_v} = \frac{10}{1-(0.1\times 10)} = \frac{10}{1-1} = \frac{10}{0} = \infty$$

This simple example shows that a loop gain of unity (or larger) will result in infinite gain and an amplifier which is unstable. In fact, the amplifier will oscillate since any disturbance will be amplified and result in an output.

Clearly, as far as an amplifier is concerned, positive feedback may have an undesirable effect – instead of reducing the overall gain the effect is that of reinforcing any signal present and the output can build up into continuous oscillation if the loop gain is 1 or greater. To put this another way, oscillator circuits can simply be thought of as amplifiers that generate an output signal without the need for an input!

## Conditions for oscillation

From the foregoing we can deduce that the conditions for oscillation are:

**(a)** the feedback must be positive (i.e. the signal fed back must arrive back in-phase with the signal at the input);

**(b)** the overall loop voltage gain must be greater than 1 (i.e. the amplifier's gain must be sufficient to overcome the losses associated with any frequency selective feedback network).

Hence, to create an oscillator we simply need an amplifier with sufficient gain to overcome the losses of the network that provide positive feedback. Assuming that the amplifier provides 180° phase shift, the frequency of oscillation will be that at which there is 180° phase shift in the feedback network.

A number of circuits can be used to provide 180° phase shift, one of the simplest being a three-stage *C–R* ladder network that we shall meet next. Alternatively, if the amplifier produces 0° phase shift, the circuit will oscillate at the frequency at which the feedback network produces 0° phase shift. In both cases, the essential point is that the feedback should be positive so that the output signal arrives back at the input in such a sense as to reinforce the original signal.

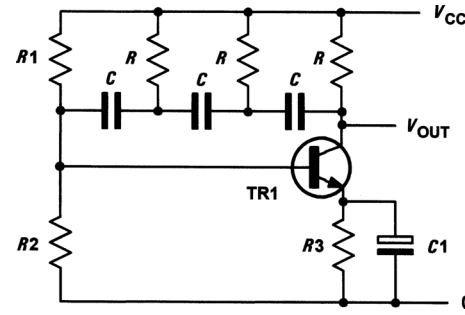


**Figure 9.2** Sine wave oscillator based on a three-stage *C–R* ladder network

## Ladder network oscillator

A simple phase-shift oscillator based on a three-stage *C–R* ladder network is shown in Fig. 9.2. TR1 operates as a conventional common-emitter amplifier stage with *R*1 and *R*2 providing base bias potential and *R*3 and *C*1 providing emitter stabilization.

The total phase shift provided by the *C–R* ladder network (connected between collector and base) is 180° at the frequency of oscillation. The transistor provides the other 180° phase shift in order to realize an overall phase shift of 360° or 0° (note that these are the same).

The frequency of oscillation of the circuit shown in Fig. 9.2 is given by:

$$f = \frac{1}{2\pi\times\sqrt{6}CR}$$

The loss associated with the ladder network is 29, thus the amplifier must provide a gain of *at least* 29 in order for the circuit to oscillate. In practice this is easily achieved with a single transistor.

### Example 9.1

Determine the frequency of oscillation of a three-stage ladder network oscillator in which $C = 10$ nF and $R = 10$ kΩ.

**Solution**

Using

$$f = \frac{1}{2\pi \times \sqrt{6}CR}$$

gives

$$f = \frac{1}{6.28 \times 2.45 \times 10 \times 10^{-9} \times 10 \times 10^{3}}$$

from which

$$f = \frac{1}{6.28 \times 2.45 \times 10^{-4}} = \frac{10^{4}}{15.386} = 647 \text{ Hz}$$

## Wien bridge oscillator

An alternative approach to providing the phase shift required is the use of a Wien bridge network (Fig. 9.3). Like the *C–R* ladder, this network provides a phase shift which varies with frequency. The input signal is applied to A and B while the output is taken from C and D. At one particular frequency, the phase shift produced by the network will be exactly zero (i.e. the input and output signals will be in-phase). If we connect the network to an amplifier producing 0° phase shift which has sufficient gain to overcome the losses of the Wien bridge, oscillation will result.

The minimum amplifier gain required to sustain oscillation is given by:

$$A_v = 1 + \frac{C1}{C2} + \frac{R2}{R1}$$

In most cases, $C1 = C2$ and $R1 = R2$, hence the minimum amplifier gain will be 3.

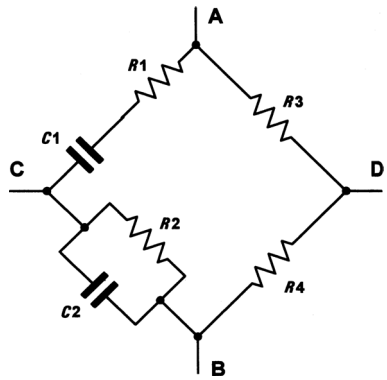


**Figure 9.3** A Wien bridge network

The frequency at which the phase shift will be zero is given by:

$$f = \frac{1}{2\pi \times \sqrt{C1\,C2\,R1\,R2}}$$

When $R1 = R2$ and $C1 = C2$ the frequency at which the phase shift will be zero will be given by:

$$f = \frac{1}{2\pi \times \sqrt{C^2R^2}} = \frac{1}{2\pi CR}$$

where $R = R1 = R2$ and $C = C1 = C2$.

**Example 9.2**

Fig. 9.4 shows the circuit of a Wien bridge oscillator based on an operational amplifier. If $C1 = C2 = 100$ nF, determine the output frequencies produced by this arrangement (a) when $R1 = R2 = 1$ kΩ and (b) when $R1 = R2 = 6$ kΩ.

**Solution**

**(a)** When $R1 = R2 = 1$ kΩ

$$f = \frac{1}{2\pi CR}$$

where $R = R1 = R1$ and $C = C1 = C2$.

Thus

$$f = \frac{1}{6.28 \times 100 \times 10^{-9} \times 1 \times 10^{3}}$$

$$f = \frac{10^{4}}{6.28} = 1.59 \text{ kHz}$$

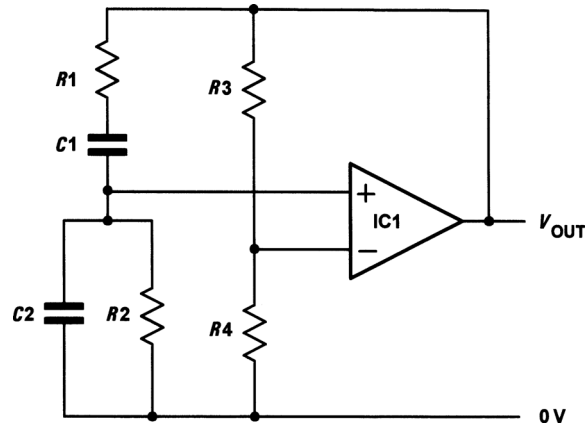


**Figure 9.4** Sine wave oscillator based on a Wien bridge network (see Example 9.2)

**(b)** When $R1 = R1 = 6\ k\Omega$

$$f = \frac{1}{2\pi CR}$$

where $R = R1 = R1$ and $C = C1 = C2$. Thus

$$f = \frac{1}{6.28 \times 100 \times 10^{-9} \times 6 \times 10^{3}}$$

$$f = \frac{10^{4}}{37.68} = 265\ Hz$$

## Multivibrators

There are many occasions when we require a square wave output from an oscillator rather than a sine wave output. Multivibrators are a family of oscillator circuits that produce output waveforms consisting of one or more rectangular pulses. The term 'multivibrator' simply originates from the fact that this type of waveform is rich in harmonics (i.e. 'multiple vibrations').

Multivibrators use regenerative (i.e. positive) feedback; the active devices present within the oscillator circuit being operated as switches, being alternately cut-off and driven into saturation.

The principal types of multivibrator are:

**(a) astable multivibrators** that provide a continuous train of pulses (these are sometimes also referred to as free-running multivibrators);

**(b) monostable multivibrators** that produce a single output pulse (they have one stable state and are thus sometimes also referred to as 'one-shot');

**(c) bistable multivibrators** that have two stable states and require a trigger pulse or control signal to change from one state to another.

## The astable multivibrator

Fig. 9.6 shows a classic form of astable multivibrator based on two transistors. Fig. 9.7 shows how this circuit can be redrawn in an arrangement that more closely resembles a two-stage common-emitter amplifier with its output connected back to its input. In Fig. 9.6, the values of the base resistors, *R*3 and *R*4, are such that

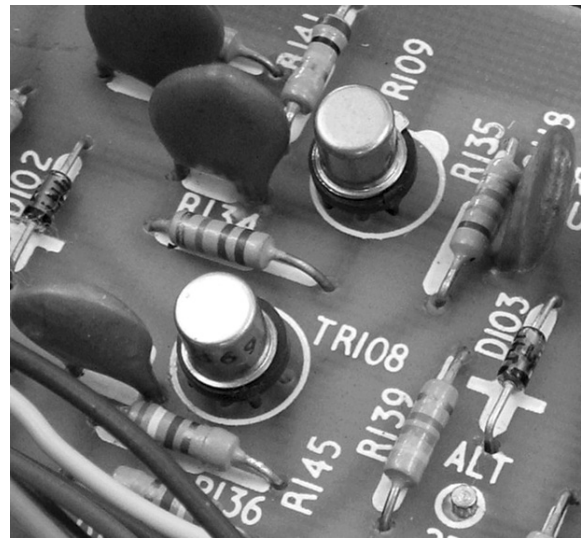


**Figure 9.5** This high-speed bistable multivibrator uses two general-purpose silicon transistors and works at frequencies of up to 1 MHz triggered from an external signal

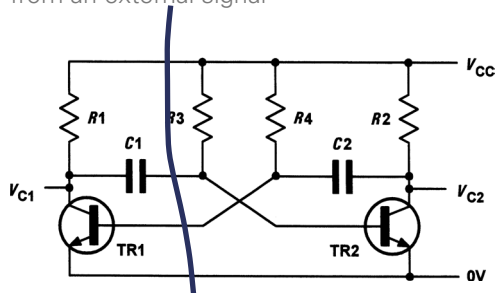


**Figure 9.6** Astable multivibrator using BJTs

the sufficient base current will be available to completely saturate the respective transistor. The values of the collector load resistors, *R*1 and *R*2, are very much smaller than *R*3 and *R*4. When power is first applied to the circuit, assume that TR2 saturates before TR1 when the power is first applied (in practice one transistor would always saturate before the other due to variations in component tolerances and transistor parameters).

As TR2 saturates, its collector voltage will fall rapidly from $+V_{CC}$ to 0 V. This drop in voltage will be transferred to the base of TR1 via *C*1. This negative-going voltage will ensure that TR1 is initially placed in the non-conducting state. As long as TR1 remains cut-off, TR2 will continue to be saturated. During this time, *C*1 will charge via *R*4 and TR1's base voltage will rise exponentially

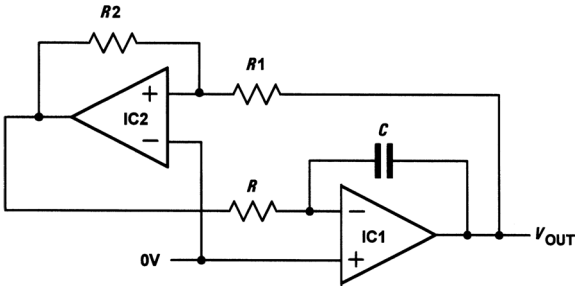


**Figure 9.9** Astable oscillator using operational amplifiers

Assume that the output from IC2 is initially at, or near, $+V_{CC}$ and capacitor, *C*, is uncharged. The voltage at the output of IC2 will be passed, via *R*, to IC1. Capacitor, *C*, will start to charge and the output voltage of IC1 will begin to fall.

Eventually, the output voltage will have *fallen* to a value that causes the polarity of the voltage at the non-inverting input of IC2 to change from positive to negative. At this point, the output of IC2 will rapidly fall to $-V_{CC}$. Again, this voltage will be passed, via *R*, to IC1. Capacitor *C* will then start to charge in the other direction and the output voltage of IC1 will begin to rise.

Some time later, the output voltage will have *risen* to a value that causes the polarity of the non-inverting input of IC2 to revert to its original (positive) state and the cycle will continue indefinitely.

The upper threshold voltage (i.e. the maximum positive value for $V_{out}$) will be given by:

$$V_{UT} = V_{CC} \times \left(\frac{R1}{R2}\right)$$

The lower threshold voltage (i.e. the maximum negative value for $V_{out}$) will be given by:

$$V_{LT} = -V_{CC} \times \left(\frac{R1}{R2}\right)$$

## Single-stage astable oscillator

A simple form of astable oscillator that produces a square wave output can be built using just one operational amplifier, as shown in Fig. 9.10. The circuit employs positive feedback with the output fed back to the non-inverting input via the potential

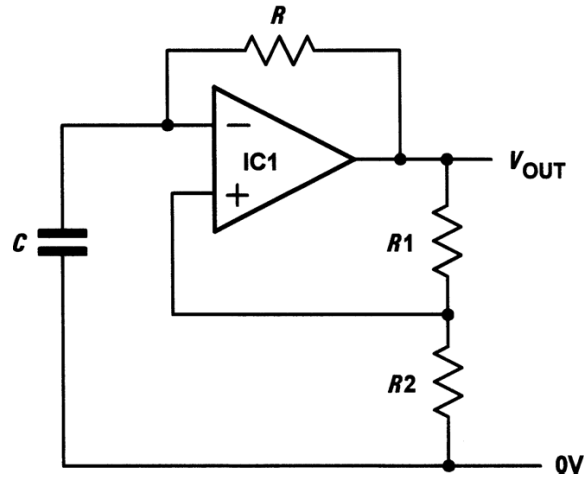


**Figure 9.10** Single-stage astable oscillator using an operational amplifier

divider formed by *R*1 and *R*2. This circuit can make a very simple square wave source with a frequency that can be made adjustable by replacing *R* with a variable or preset resistor.

Assume that *C* is initially uncharged and the voltage at the inverting input is slightly less than the voltage at the non-inverting input. The output voltage will rise rapidly to $+V_{CC}$ and the voltage at the inverting input will begin to rise exponentially as capacitor *C* charges through *R*.

Eventually the voltage at the inverting input will have reached a value that causes the voltage at the inverting input to exceed that present at the non-inverting input. At this point, the output voltage will rapidly fall to $-V_{CC}$. Capacitor *C* will then start to charge in the other direction and the voltage at the inverting input will begin to fall exponentially.

Eventually, the voltage at the inverting input will have reached a value that causes the voltage at the inverting input to be less than that present at the non-inverting input. At this point, the output voltage will rise rapidly to $+V_{CC}$ once again and the cycle will continue indefinitely.

The upper threshold voltage (i.e. the maximum positive value for the voltage at the inverting input) will be given by:

$$V_{UT} = V_{CC} \times \left(\frac{R2}{R1+R2}\right)$$

The lower threshold voltage (i.e. the maximum negative value for the voltage at the inverting input) will be given by:

$$V_{LT} = -V_{CC} \times \left(\frac{R2}{R1+R2}\right)$$

Finally, the time for one complete cycle of the output waveform produced by the astable oscillator is given by:

$$T = 2CR\ln\left(1+2\left(\frac{R2}{R1}\right)\right)$$

## Crystal controlled oscillators

A requirement of some oscillators is that they accurately maintain an exact frequency of oscillation. In such cases, a quartz crystal can be used as the frequency determining element. The quartz crystal (a thin slice of quartz in a hermetically sealed enclosure, see Fig. 9.11) vibrates whenever a potential difference is applied across its faces (this phenomenon is known as the piezoelectric effect). The frequency of oscillation is determined by the crystal's 'cut' and physical size.

Most quartz crystals can be expected to stabilize the frequency of oscillation of a circuit to within a few parts in a million. Crystals can be manufactured for operation in **fundamental mode** over a frequency range extending from 100 kHz to around 20 MHz and for **overtone** operation from 20 MHz to well over 100 MHz. Fig. 9.12 shows a simple crystal oscillator circuit in which the crystal provides feedback from the drain to the source of a junction gate FET.

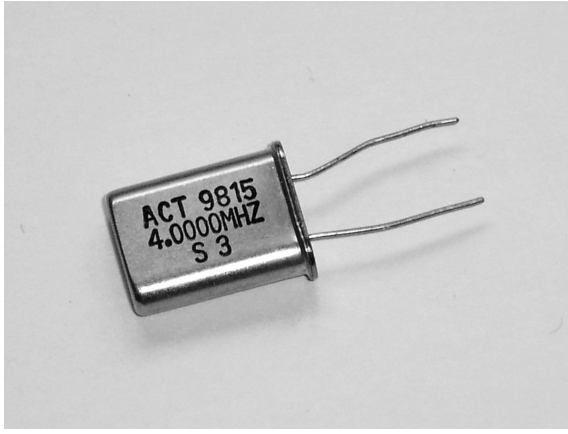


**Figure 9.11** A quartz crystal (this crystal is cut to be resonant at 4 MHz and is supplied in an HC18 wire-ended package)

## Practical oscillator circuits

Fig. 9.13 shows a practical sine wave oscillator based on a three-stage *C*–*R* ladder network. The circuit provides an output of approximately 1 V peak–peak at 1.97 kHz.

A practical Wien bridge oscillator is shown in Fig. 9.14. This circuit produces a sine wave output at 16 Hz. The output frequency can easily be varied by making *R*1 and *R*2 a 10 kΩ dual-gang potentiometer and connecting a fixed resistor of 680 Ω in series with each. In order to adjust the loop gain for an optimum sine wave output it may be necessary to make *R*3/*R*4 adjustable. One way of doing this is to replace both components with a 10 kΩ multi-turn potentiometer with the sliding contact taken to the inverting input of IC1.

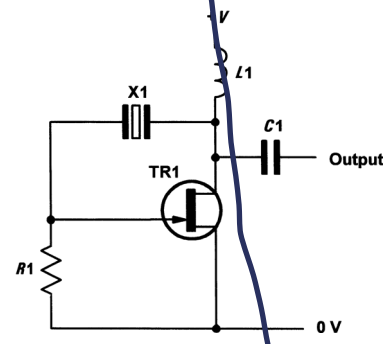


**Figure 9.12** A simple JFET oscillator

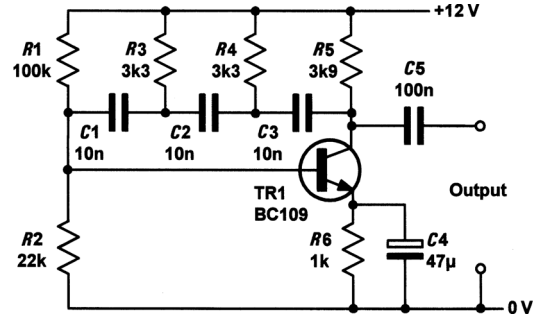


**Figure 9.13** A practical sine wave oscillator based on a phase shift ladder network