# counter

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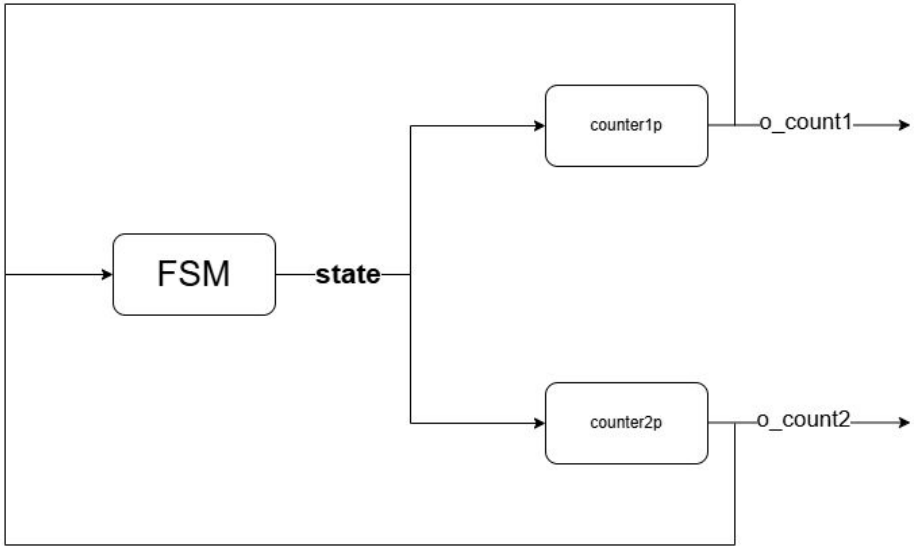
# 說明




**調節**：當counter數完後跟新state狀態

# 說明

```
fd:process(i_clk ,i_rst)
begin
if (i_rst = '0') then
    divclk <= (others => '0');
elsif (rising_edge(i_clk)) then
    divclk <= divclk +1 ;
end if;
end process fd;
fclk <= divclk(25);
```

除頻:將counter的clk改良為在
divclk在2^25時的狀態當作
clk

**除頻後肉眼才能看見**

# 說明

```
FSM:process(i_clk, i_rst)
begin
    if i_rst = '0' then
        state <= '0';
    elsif i_clk'event and i_clk ='1' then
        case state is
            when '0' =>
                if count1="1111" then
                    state <= '1';
                end if;
            when '1' =>
                if count2="0000" then
                    state <= '0';
                end if;
            when others =>
                null;
        end case;
    end if;
end process;
```

當count1 數到 1111時 , state為 1

當count2 數到 0000時 , state為 0

# 說明

```
counter1p:process(fclk, i_rst, state)
begin
    if i_rst = '0' then
        count1 <= "0000";
    elsif fclk'event and fclk ='1' then
        case state is
            when '0' =>
                count1 <= count1 + '1';
            when '1' =>
                null;
            when others =>
                null;
        end case;
    end if;
end process;
```

i_rst 為 0 時將 count1 重製

state為 0 時 + 1
state為 1 時 ,不動作

**counter2p反之亦然**

# Thank