2021 Digital IC Design Homework 4

NAME	李秉軒
Student ID	E24066755

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6,488,516 (ns)

(your pre-sim result)

```
#  Result image is correct !
#  ------------------- S U M M A R Y --------------------
#  Congratulations! Result image data have been generated successfully! The result is PASS!!
#  ** Note: $finish    : D:/4th,2nd_semester/DIC/HW4/file/testfixture.v(123)
#     Time: 6488508 ns  Iteration: 0  Instance: /testfixture
```

(your post-sim result)

```
#  Result image is correct !
#  ------------------- S U M M A R Y --------------------
#  Congratulations! Result image data have been generated successfully! The result is PASS!!
#  ** Note: $finish    : D:/4th,2nd_semester/DIC/HW4/file/testfixture.v(123)
#     Time: 6488516234 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result

Total logic elements	386 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)
Clock width (Cycle)	12ns

(your flow summary)

Flow Summary	
Flow Status	Successful - Sun Jun 13 01:32:32 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	MFE
Top-level Entity Name	MFE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	386 / 68,416 (< 1 %)
Total combinational functions	320 / 68,416 (< 1 %)
Dedicated logic registers	183 / 68,416 (< 1 %)
Total registers	183
Total pins	57 / 622 (9 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

I hide the latency of memory access inside the sorting algorithm. Since it takes around 30 cycles for the sorting algorithm, I give the circuit 3 cycles to compute the correct address for gray image. That's why I can achieve 12ns clock width.

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*