2021 Digital IC Design Homework 1

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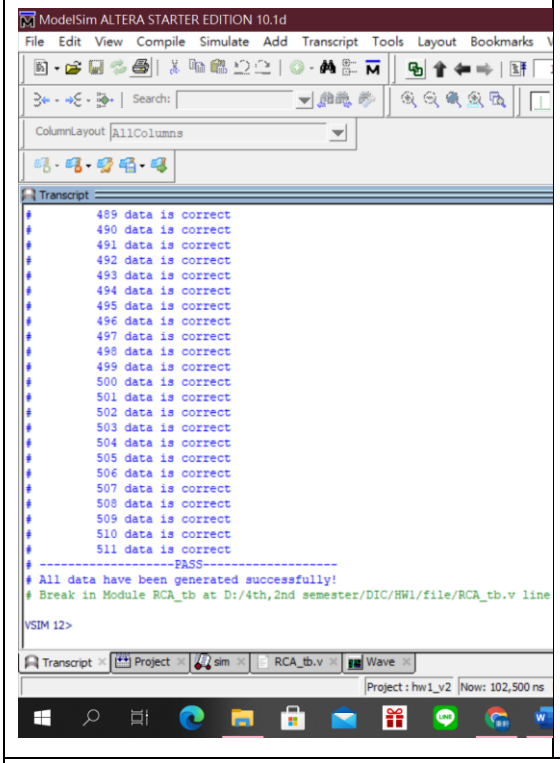
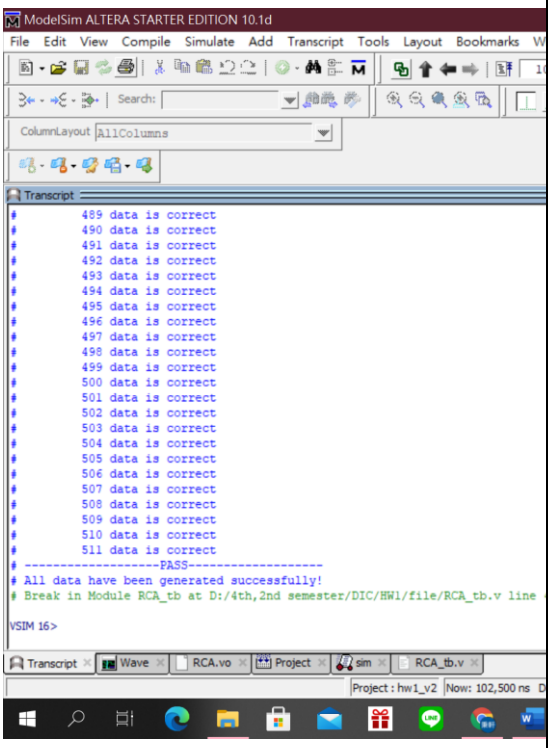
Simulation Result

Functional simulation	Success	Gate-level simulation	Success	Gate-level simulation time	

(your pre-sim result)



(your post-sim result)



Synthesis Result

Total logic elements	10 / 68,416 (< 1%)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)
Clock Width (Cycle)	100ns

Flow Summary	
Flow Status	Successful - Tue Apr 06 20:04:48 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	RCA
Top-level Entity Name	RCA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	10 / 68,416 (< 1 %)
Total combinational functions	10 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

A Ripple Carry Adder constructed with 4 Full Adder, which composed of 2 Half Adder. This design follows the circuit provided in homework description.