2021 Digital IC Design Homework 5

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	53850 (ns)

(your pre-sim result)

```
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : D:/4th,2nd_semester/DIC/HW5/file/testfixture2.v(241)
#    Time: 10770 ns  Iteration: 0  Instance: /testfixture1
# 1
```

(your post-sim result)

```
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : D:/4th,2nd_semester/DIC/HW5/file/testfixture1.v(240)
#    Time: 53850 ns  Iteration: 0  Instance: /testfixture1
# 1
```

Synthesis Result

Total logic elements	6,398 / 68,416 (9 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	46 / 300 (15 %)
Clock width (Cycle)	50ns

(your flow summary)

Flow Summary	
Flow Status	Successful - Tue Jun 29 09:42:05 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FAS
Top-level Entity Name	FAS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	6,398 / 68,416 (9 %)
Total combinational functions	5,925 / 68,416 (9 %)
Dedicated logic registers	1,085 / 68,416 (2 %)
Total registers	1085
Total pins	554 / 622 (89 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	46 / 300 (15 %)
Total PLLs	0 / 4 (0 %)

Description of your design

I implement the architecture on the homework description ,and design a controller – data path architecture. Since there are some tiny deviations at the fft_d1 output, I slightly tune the result, and the result is correct.

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*