2021 Digital IC Design Homework 3

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	61250 (ns)

(your pre-sim result)

```
#
# Object50: PASS
#
# ------------------------------------
# --     Simulation finish,   ALL PASS
# ------------------------------------
# ** Note: $finish    : D:/4th,2nd_seme
#    Time: 61250 ns  Iteration: 1  Inst
# 1
# Break in Module testfixture at D:/4th
```

(your post-sim result)

```
# Object48: PASS
#
# Object49: PASS
#
# Object50: PASS
#
# ----------------------------------------
# --     Simulation finish,   ALL PASS
# ----------------------------------------
# ** Note: $finish    : D:/4th,2nd_semester/
#    Time: 61250 ns  Iteration: 1  Instance:
# 1
# Break in Module testfixture at D:/4th,2nd_
VSIM 4>
```

Synthesis Result

Total logic elements	483 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	4 / 300 (1 %)
Clock width (Cycle)	50ns

(your flow summary)

Flow Summary

Flow Status	Successful - Mon May 17 22:37:00 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	PSE
Top-level Entity Name	PSE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	483 / 68,416 (< 1 %)
Total combinational functions	482 / 68,416 (< 1 %)
Dedicated logic registers	157 / 68,416 (< 1 %)
Total registers	157
Total pins	46 / 622 (7 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

本次設計採用 finite state machine 的設計方式，Input state 接收 tb 傳來的 input，並在 cal、cal_comp state 進行外積的運算，swap state 則根據外積結果決定是否需要做交換，並更新下一筆需要進行外積的向量。本設計並未特別使用 resource sharing 的概念，原因是發現 Total logic elements 反而會變大，可能是與 cycleii 內部的架構有關。

Scoring = Total logic elements