Kettering University

CE-210 Digital Systems I

Lab Exercise 2

Gates:
Basic Building Blocks of Digital Circuits

Spring 2019

Prelab: No experiment is required for assignments **2, 4, 6, 8, 12 and 14**, which are your **prelab**. You will answer these questions before your week02's lab time starts.

Note: Lab02 report is due by the end of today's lab session.

Section

Name **Number**

Lab Partner's Name and No

Purpose of this lab experiment

Objectives

- *Examine different logic gates and learn*
  - *how to obtain inverters from NAND or NOR gates,*
  - *what signal gating is,*
  - *what a programmable inverter is,*
  - *how to handle unused inputs,*
  - *how to obtain larger gates from smaller ones.*

What to Hand In

Turn in this lab handout after you have

- Completed the cover sheet
- Finished all the assignments/experiments
- Filled in all the truth tables
- Answered all the questions

Also, show your functional circuit in **Assignment 17** to the lab instructor.

Introduction

In the manual design (as opposed to computerized or automatic design) of digital circuits, and after the word description of problem has been translated into a truth table, we need a menu of basic building blocks or *gates* and also a design methodology. We use this methodology to identify the right devices from the menu, and properly connect them together to reach a digital circuit with a terminal behavior specified by the truth table. In last week's lab, you examined several gates, but only as black boxes, to obtain their truth tables. In this week's lab, you will closely study some gates in more detail, as explained in the "Assignments" Section. The design methodology will be covered in the coming weeks.

Notes

- Pin diagrams for the chips that you are going to use are shown in Appendix 1 on page 10.
- Add pin numbers to logic diagrams. This will help you in troubleshooting stage.
- Every chip has to be properly connected to V_{CC} and GND.
- Wire up your circuits neatly. Use short wires for inter-chip connections. The inter-chip wires should not jump over the chips.
- Use colored wires in meaningful ways. Use red for V_{CC} and black for GND. Also use the same color for the wires running between the same-signal nodes. This will significantly help you manage your (complex) circuits, especially in the debugging phase of your work.
- Connect the power rails of your breadboard to the positive (red) and negative (black) terminals of the power supply that you have on your workstation. In other words, you should have only two wires coming from the power supply to your breadboard: one red wire and one black wire.
- Be prepared for possible questions that you may be asked regarding different assignments in today's lab.
- **Definition:** The *dual* of an expression is another expression obtained through the following process:

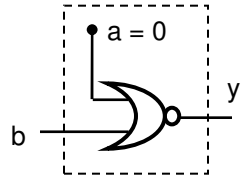
Swap 1s and 0s. Also swap ANDs and ORs[1]. We may abbreviate the process as $(1 \leftrightarrow 0)$ and $(. \leftrightarrow +)$.
For example, the dual of $(a \,.\, b)' + c$ is $(a + b)' \,.\, c$ and vice versa. Also, the dual of $a' + 0$ is $a' \,.\, 1$ and vice versa. **Hint:** Two dual expressions are not necessarily equal to each other or opposite of each other.

[1] Here, we assume that only the basic operators, AND, OR and NOT, may participate in the logic expression.

Assignments

NAND/NOR Conversion to Inverter

1. Wire up the circuit shown in Figure 1*a*, and then cross out the irrelevant rows in the NOR truth table shown in Figure 1*b*. By applying the two possible values to the circuit in Figure 1*a*, fill out the truth table in Figure 1*c*. What is the function of this circuit? Are the two truth tables obtained in Figure 1*b* and Figure 1*c* equivalent? Place your answers in the spaces provided in Figure 1.



(a)

a b	y
0 0	1
0 1	0
1 0	0
1 1	0

(b)

b	y
0	
1	

(c)

Fill in the blank: This circuit is functionally equivalent to …

← Are these 2 tables equivalent?

Yes No

Figure 1. For Assignment 1

Prelab: No experiment is required for assignments **2, 4, 6, 8, 12 and 14**, which are your prelab.

2. **No experiment required (Prelab)**: In the space provided for Figure 2*a*, draw the NAND-gate-based counterpart or *dual* of the circuit shown in Figure 1*a*, and then cross out the irrelevant rows in the NAND truth table shown in Figure 2*b*.

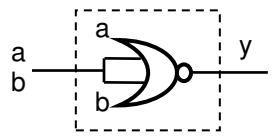
(a)

a b	y
0 0	1
0 1	1
1 0	1
1 1	0

(b)

Figure 2. For Assignment 2

3. Wire up the circuit shown in Figure 3*a*, and then cross out the irrelevant rows in the NOR truth table shown in Figure 3*b*. Apply the two possible values to the circuit in Figure 3*a* to fill out the truth table in Figure 3*c*. What is the function of this circuit? Are the two truth tables obtained in Figure 3*b* and Figure 3*c* equivalent? Place your answers in the spaces provided in Figure 3.



(a)

a b	y
0 0	1
0 1	0
1 0	0
1 1	0

(b)

a = b	y
0	
1	

(c)

Fill in the blank: This circuit is functionally equivalent to …

← Are these 2 tables equivalent?

Yes No

Figure 3. For Assignment 3

4. **No experiment required (Prelab)**: In the space provided for Figure 4*a*, draw the dual of the circuit shown in Figure 3*a*. Then cross out the irrelevant rows in the NAND truth table shown in Figure 4*b*.

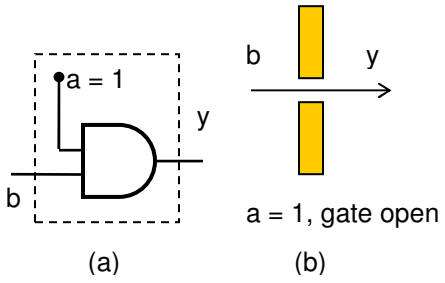
a b	y
0 0	1
0 1	1
1 0	1
1 1	0

(a) (b)

Figure 4. For Assignment 4

Signal Gating

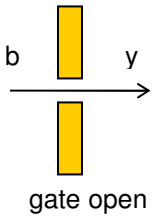
5. Hook up one of the inputs of a two-input AND gate to logic 1 (see Figure 5*a*), and then apply a time-varying signal to the other input. How can you generate a time varying signal in the lab by using only the features that you are familiar with so far? What do you see at the output of this gate? Put your answers in the spaces provided in Figure 5.



How do you generate a time-varying signal for input b?
What do you see at the output (y)?

Figure 5. For Assignment 5

6. **No experiment required, Prelab**: In the space provided for Figure 6*a*, draw the dual of the circuit shown in Figure 5*a*.



(a) (b)

Figure 6. For Assignment 6

7. Hook up one of the inputs of a two-input AND gate to logic 0 (Figure 7*a*), and then apply a time-varying signal to the other input. What do you see at the output of this gate? Place your answer in the space provided in Figure 7.

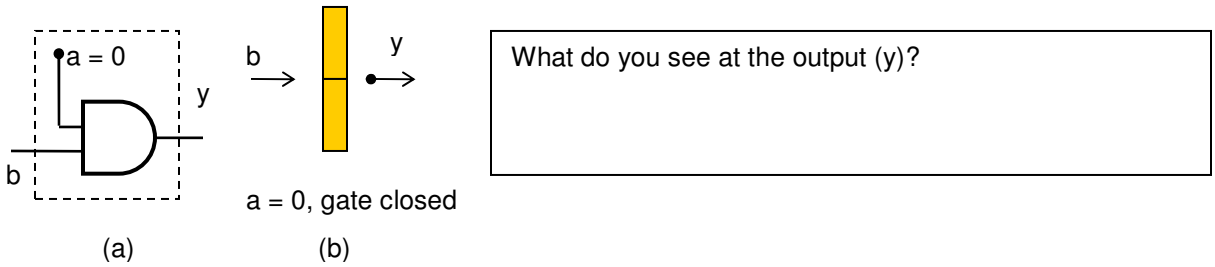
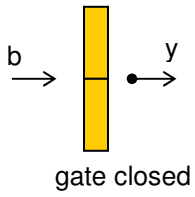


Figure 7. For Assignment 7

8. **No experiment required (Prelab)**: In the space provided in Figure 8*a*, draw the dual of the circuit shown in Figure 7*a*.

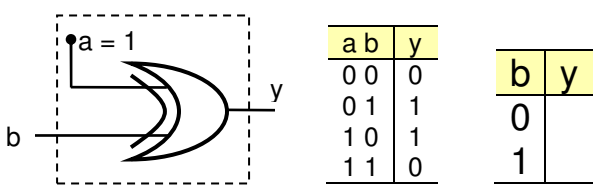


(a) (b)

Figure 8. For Assignment 8

Programmable Inverters

9. Fix one of the inputs of a two-input XOR gate at logic 1 (see Figure 9*a*) and then cross out the irrelevant rows in the XOR truth table shown in Figure 9*b*. Apply the two possible values to input b in Figure 9*a* to fill out the truth table shown in Figure 9*c*. What is the function of this circuit? Are the two truth tables obtained in Figure 9*b* and Figure 9*c* equivalent? Place your answers in the spaces provided in Figure 9.



(a)

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

b	y
0	
1	

(c)

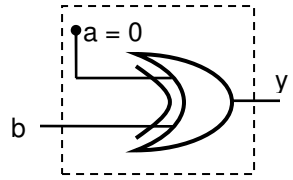
Fill in the blank: This circuit is functionally equivalent to …

← Are these 2 tables equivalent?

Yes No

Figure 9. For Assignment 9

10. Wire up the circuit illustrated in Figure 10*a*, and then cross out the irrelevant rows in the XOR truth table shown in Figure 10*b*. Apply the two possible values to input b in Figure 10*a* to fill out the truth table shown in Figure 10*c*. What is the function of this circuit? Are the two truth tables obtained in Figure 10*b* and Figure 10*c* equivalent? Place your answers in the spaces provided in Figure 10.



(a)

a b	y
0 0	0
0 1	1
1 0	1
1 1	0

(b)

b	y
0	
1	

(c)

Fill in the blank: This circuit is functionally equivalent to …

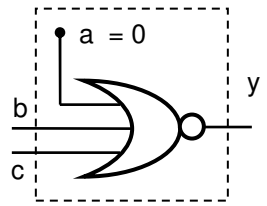
← Are these 2 tables equivalent?

Yes No

Figure 10. For Assignment 10

Unused Inputs

11. Fix one of the inputs of a 3-input NOR gate at logic 0 (see Figure 11*a*), and then cross out the irrelevant rows in the 3-input NOR truth table shown in Figure 11*b*. Apply all possible input combinations to inputs b and c (in Figure 11*a*) to fill out the truth table shown in Figure 11*c*. What is the function of this circuit? Are the two tables obtained in Figure 11 equivalent? Place your answers in the spaces provided in Figure 11.



(a)

Row	a b c	y
0	0 0 0	1
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
6	1 1 0	0
7	1 1 1	0

(b)

b c	y
0 0	
0 1	
1 0	
1 1	

(c)

Fill in the blank: This circuit is functionally equivalent to …

← Are these 2 tables equivalent?

Yes No

Figure 11. For Assignment 11

12. No experiment required (Prelab): In the space provided for Figure 12*a*, draw the dual of the circuit shown in Figure 11*a*, and then cross out the irrelevant rows in the 3-input NAND truth table shown in Figure 12*b*. What is the function of the circuit that you obtained in Figure 12*a*? Place your answer in the space provided in Figure 12.

(a)

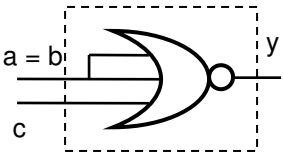
Row	a b c	y
0	0 0 0	1
1	0 0 1	1
2	0 1 0	1
3	0 1 1	1
4	1 0 0	1
5	1 0 1	1
6	1 1 0	1
7	1 1 1	0

(b)

Fill in the blank:
This circuit is functionally equivalent to …

Figure 12. For Assignment 12

13. Connect two inputs (a and b) of a three-input NOR gate together, as shown in Figure 13*a*, and then cross out the irrelevant rows in the 3-input NOR truth table shown in Figure 13*b*. Now, apply all possible input combinations to inputs b and c (in Figure 13*a*) to fill out the truth table shown in Figure 13*c*. What is the function of this circuit? Are the two tables obtained in Figure 13 equivalent? Place your answers in the spaces provided in Figure 13.



(a)

Row	a b c	y
0	0 0 0	1
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
6	1 1 0	0
7	1 1 1	0

(b)

b c	y
0 0	
0 1	
1 0	
1 1	

(c)

Fill in the blank: This circuit is functionally equivalent to …

← Are these 2 tables equivalent?

Yes No

Figure 13. For Assignment 13

14. No experiment required (Prelab): In the space provided for Figure 14*a*, draw the dual of the circuit shown in Figure 13*a*, and then cross out the irrelevant rows in the 3-input NAND truth table shown in Figure 14*b*. What is the function of the circuit that you obtained in Figure 14*a*? Place your answer in the space provided in Figure 14.

(a)

Row	a b c	y
0	0 0 0	1
1	0 0 1	1
2	0 1 0	1
3	0 1 1	1
4	1 0 0	1
5	1 0 1	1
6	1 1 0	1
7	1 1 1	0

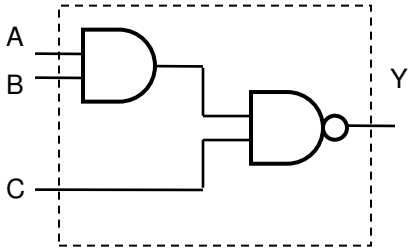
(b)

Fill in the blank:
This circuit is functionally equivalent to …

Figure 14. For Assignment 14

How to Obtain Larger Gates from Smaller Gates

15. Note: You need **two** chips in this assignment. Wire up the circuit shown in Figure 15*a*, and then apply all possible input combinations to the inputs of this circuit to fill out the truth table shown in Figure 15*b*. What is the function of this circuit? Place your answer in the space provided in Figure 15.



(a)

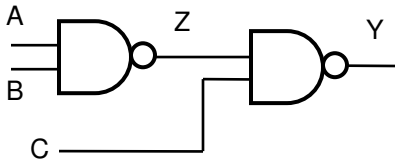
Fill in the blank:
This circuit is functionally equivalent to …

Row	A B C	Y

(b)

Figure 15. For Assignment 15

16. Note: You need only **one** chip in this assignment. Wire up the circuit shown in Figure 16 and then apply an input to prove that this circuit is NOT functionally equivalent to a three-input NAND gate.

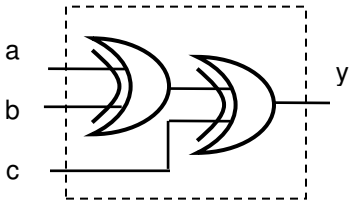


The input that you applied (counterexample) is:

A B C =

Figure 16. For Assignment 16

17. Note: You need only **one** chip in this assignment. Wire up the circuit shown in Figure 17*a*, and then apply all possible input combinations to this circuit to fill out the truth table shown in Figure 17*b*. What is the function of this circuit? Place your answer in the space provided in Figure 17. **Show your functional circuit to the lab instructor.**



(a)

Row	a b c	y
0	0 0 0	
1	0 0 1	
2	0 1 0	
3	0 1 1	
4	1 0 0	
5	1 0 1	
6	1 1 0	
7	1 1 1	

(b)

Fill in the blank:
This circuit is functionally equivalent to …

Figure 17. For Assignment 17

18. The circuit shown in Figure 17*a* is the solution for a familiar problem. Explain this problem briefly:

Appendix: Pin Diagrams for Some Frequently Used TTL Chips