



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-7525A

Stencil Design Guidelines

IPC-7525A

February 2007

A standard developed by IPC

Supersedes IPC-7525
May 2000

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1249
Tel. 847.615.7100 Fax 847.615.7105
www.ipc.org

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-7525A

Stencil Design Guidelines

Developed by the Stencil Design Task Group (5-21e) of the Assembly and Joining Processes Committee (5-20) of IPC

Supersedes:

IPC-7525 - May 2000

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Stencil Design Task Group (5-21e) of the Assembly and Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Assembly and Joining Processes Committee	Stencil Design Task Group	Technical Liaisons of the IPC Board of Directors
Chair Leo Lambert EPTAC Corporation	Co-Chairs William E. Coleman, Ph.D Photo Stencil Inc. Kathy Jenczewski MicroScreen, LLC	Peter Bigelow IMI Inc. Sammy Yi Flextronics International
Stencil Design Task Group		
Charles Dal Currier, Ambitech Inc. Christopher Sattler, AQS - All Quality & Services, Inc. Jay B. Hinerman, BAE Systems CNI Div. Gary M. Carabetta, Bose Corporation Richard Lieske, DEK USA Inc. Ricky Bennett, DEK USA Inc. Glenn Dody, Dody Consulting Ahne Oosterhof, Fine Line Stencil / A-Laser, Inc. Michael W. Yuen, Foxconn EMS, Inc. Frank V. Grano, GE Fanuc Embedded Systems Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information Richard R. Lathrop, Jr., Heraeus, Inc. JD Brown, Hewlett-Packard Co-ProCurve Networking Rongxiang (Davis) Yang, Huawei Technologies Co., Ltd.	Tim Jensen, Indium Corporation of America Kantesh Doss, Ph.D., Intel Corporation David P. Torp, Kester Maureen A. Brown, Kester Barry R. Goukler, Metal Etching Technology Bill Kunkle, Metal Etching Technology Holly Wise, MicroScreen, LLC Kathy Jenczewski, MicroScreen, LLC William Dean May, NSWC Crane Michael R. Burgess, Photo Stencil Inc. William E. Coleman, Ph.D., Photo Stencil Inc. Dale Kratz, Plexus Corp. Denis Jean, Plexus Corp. Timothy M. Pitsch, Plexus Corp.	Charlie Davis, RadiSys Corporation Robert Rowland, RadiSys Corporation David R. Nelson, Raytheon Company Jeff Shubrooks, Raytheon Company Mark J. Quealy, Schneider Automation Inc. Narinder Kumar, C.I.D., Solectron Invotronics George Oxx, Solectron Technology Inc. Sagid Quiroz, Sony Guillermo Velazquez, Sony de Tijuana Este S.A. de C.V. Vanessa Lopez, Sony de Tijuana Este S.A. de C.V. Steve Sangillo, Swemco Daan Terstegge, Thales Communications Jerry Cupples, VLSIP Technologies

Table of Contents

1 PURPOSE	1	3.2.2 Aperture Size Versus Board Land Size for Tin Lead Solder Paste	6
1.1 Terms and Definitions	1	3.2.3 Aperture Size versus Board Land Size for Lead Free Solder Paste	7
1.1.1 *Aperture	1	3.2.4 Glue Aperture Chip Component	8
1.1.2 *Aspect Ratio	1	3.2.5 Glue Apertures for Combination of Chip Components and Leaded Devices	8
1.1.3 *Area Ratio	1	3.3 Mixed Technology Surface-Mount/Through-Hole (Intrusive Reflow)	8
1.1.4 Border	1	3.3.1 Solder Paste Volume	9
1.1.5 Contained Paste Transfer Head	1	3.4 Mixed Technology Surface-Mount/Flip Chip	10
1.1.6 Etch Factor	1	3.4.1 Two-Print Stencil for Surface-Mount/Flip Chip	11
1.1.7 Fiducials	1	3.5 Step Stencil Design	11
1.1.8 Fine-Pitch BGA/Chip Scale Package (CSP)	1	3.5.1 Step-Down Stencil	11
1.1.9 *Fine-Pitch Technology (FPT)	1	3.5.2 Step-Up Stencil	11
1.1.10 Foil	1	3.5.3 Step Stencil for Contained Paste Transfer Heads	11
1.1.11 Frame	1	3.5.4 Relief-Etch Stencil	11
1.1.12 *Intrusive Soldering	1	3.6 Fiducials	12
1.1.13 *Land	1	3.6.1 Global Fiducials	12
1.1.14 Modification	1	3.6.2 Local Fiducials	12
1.1.15 *Overprinting	1	4 STENCIL FABRICATION	12
1.1.16 *Pad	1	4.1 Foils	12
1.1.17 *Squeegee	1	4.2 Frames	12
1.1.18 Standard BGA	1	4.3 Stencil Border	12
1.1.19 *Stencil	1	4.4 Stencil Fabrication Technologies	12
1.1.20 Step Stencil	1	4.4.1 Chemical Etch	12
1.1.21 *Surface-Mount Technology (SMT)	1	4.4.2 Laser-Cut Stencils	12
1.1.22 *Through-Hole Technology (THT)	1	4.4.3 Electroform	12
1.1.23 Ultra-Fine Pitch Technology	2	4.4.4 Hybrid	12
2 APPLICABLE DOCUMENTS	2	4.4.5 Trapezoidal Apertures	12
2.1 IPC	2	4.4.6 Additional Options	12
3 STENCIL DESIGN	2	5 STENCIL MOUNTING	13
3.1 Stencil Data	2	5.1 Location of Image on Metal	13
3.1.1 Data Format	2	5.2 Centering	13
3.1.2 Gerber® Format	2	5.3 Additional Design Guidelines	13
3.1.3 Aperture List	2	6 STENCIL ORDERING	13
3.1.4 Solder Paste Layer	2	7 STENCIL USER'S INSPECTION/VERIFICATION	13
3.1.5 Data Transfer	2	8 STENCIL CLEANING	13
3.1.6 Panelized Stencils	2	9 END OF LIFE	13
3.1.7 Step-and-Repeat	2	APPENDIX A EXAMPLE ORDER FORM	14
3.1.8 Image Orientation/Rotation	2		
3.1.9 Image Location	2		
3.1.10 Identification	3		
3.2 Aperture Design	3		
3.2.1 Aperture Size	3		

Figures

Figure 3-1	Area Ratio Chart Showing Recommendations for a 4 mil Thick Stencil	4
Figure 3-2	Area Ratio Chart Showing Recommendations for a 5 mil Thick Stencil	5
Figure 3-3	Area Ratio Chart Showing Recommendations for a 6 mil Thick Stencil	5
Figure 3-4	Area Ratio Chart Showing Recommendations for a 8 mil Thick Stencil	6
Figure 3-5	Cross-Sectional View of A Stencil	6
Figure 3-6	Home Plate Aperture Design	7
Figure 3-7	Bow Tie Aperture Design	7
Figure 3-8	Oblong Aperture Design	7
Figure 3-9	Aperture Design for MELF Components and Chip Components	7
Figure 3-10	Window Pane Design for Ground Plane	7
Figure 3-11	Glue Stencil Aperture Design	8
Figure 3-12	Chip Component and SOIC Present on Board	8

Figure 3-13	Print Only Mode 15 mil Thick Stencil	8
Figure 3-14	Glue Stencil with Glue Reservoir	9
Figure 3-15	Through-Hole Solder Paste Volume	9
Figure 3-16	Overprint without Step	10
Figure 3-17	Overprint with Step (Squeegee Side)	10
Figure 3-18	Overprint with Step (Contact/Board Side)	10
Figure 3-19	Two-Print Through-Hole Stencil	10
Figure 3-20	Two-Print Stencil for Mixed Technology	11
Figure 4-1	Trapezoidal Apertures	12

Tables

Table 3-1	General Aperture Design Guideline Examples for Selective Surface-Mount Devices (Tin Lead Solder Paste)	3
Table 3-2	Process Window for Intrusive Soldering - Maximum Limits Desirable	3

Stencil Design Guidelines

1 PURPOSE

This document provides guides for the design and fabrication of stencils for solder paste and surface-mount adhesive. It is intended as a guideline only as much of the content is based on the experience of stencil designers, fabricators and users. Printing performance depends on many different variables and therefore no single set of design rules can be established.

1.1 Terms and Definitions All terms and definitions used throughout this handbook are in compliance with IPC-T-50. Definitions denoted with an asterisk (*) below are reprints from IPC-T-50. Other specific terms and definitions, essential for the discussion of the subject, are provided below.

1.1.1 *Aperture An opening in the stencil foil.

1.1.2 *Aspect Ratio The ratio of the width of the aperture to the thickness of the stencil foil.

1.1.3 *Area Ratio The ratio of the area of aperture opening to the area of aperture walls.

1.1.4 Border Peripheral tensioned mesh, either polyester or stainless steel, which keeps the stencil foil flat and taut. The border connects the foil to the frame.

1.1.5 Contained Paste Transfer Head A stencil printer head that holds, in a single replaceable component, the squeegee blades and a pressurized chamber filled with solder paste.

1.1.6 Etch Factor Etch Factor = Etched Depth/Lateral; Etch in a chemical etching process

1.1.7 Fiducials Reference marks on the stencil foil (and other board layers) for aligning the board and the stencil when using a vision system in a printer.

1.1.8 Fine-Pitch BGA/Chip Scale Package (CSP) Ball grid array with less than 1 mm [39 mil] pitch. This is also known as Chip Scale Package (CSP) when the package size is no more than 1.2X the area of the original die size.

1.1.9 *Fine-Pitch Technology (FPT) A surface-mount assembly technology with component terminations on centers less than or equal to 0.625 mm [24.61 mil].

1.1.10 Foil The sheet used to create the stencil.

1.1.11 Frame This may be made of tubular or cast aluminum to which a tensioned mesh (border) is permanently bonded using an adhesive. The foil is bonded to the mesh. Some foils can be mounted into a re-usable tensioning master frame and do not require a mesh border and negate a permanent bonding of the foil to the frame.

1.1.12 *Intrusive Soldering Intrusive soldering may also be known as paste-in-hole, pin-in-hole, or pin-in-paste soldering. This is a process in which the solder paste for the through-hole components is applied using the stencil. The through-hole components are inserted and reflow-soldered together with the surface-mount components.

1.1.13 *Land A portion of a conductive pattern usually used for the connection and/or attachment of components.

1.1.14 Modification The process of changing an aperture in size or shape.

1.1.15 *Overprinting The use of stencils with apertures larger than the lands or annular rings on the board.

1.1.16 *Pad See land.

1.1.17 *Squeegee A metal or polymer blade used to wipe a material (ink or solder paste) across a stencil or silk screen to force the material through the openings in the screen or stencil, onto the surface of a printed board or mounting structure. Normally the squeegee is mounted at an angle such that the contacting edge of the squeegee trails behind the print head and the face of the squeegee slopes forward.

1.1.18 Standard BGA Ball grid array with 1 mm [39 mil] pitch or larger.

1.1.19 *Stencil A thin sheet of material containing openings to reflect a specific pattern, designed to transfer a paste-like material to a substrate for the purpose of component attachment.

1.1.20 Step Stencil A stencil with more than one foil thickness level.

1.1.21 *Surface-Mount Technology (SMT) The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

1.1.22 *Through-Hole Technology (THT) The electrical connection of components to a conductive pattern by the use of component holes.

1.1.23 Ultra-Fine Pitch Technology A surface-mount assembly technology with component terminations on centers less than or equal to 0.40 mm [15.7 mil]

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology (Offspring)

IPC-7095 Design and Assembly Process Implementation of BGAs

3 STENCIL DESIGN

3.1 Stencil Data

3.1.1 Data Format Regardless of the stencil fabrication method used, Gerber® is the preferred data format. Possible alternative formats are IPC-2581, DXF, HP-GL, Barco, and ODB++ etc; however, they may need to be converted to Gerber® format prior to the stencil manufacturing process.

Gerber® data describes the file format that provides a language for communicating with the photo plotting system to produce a tool for chemically etched stencils. It is also used to produce the laser cut or electroformed stencils. While the actual data format may vary from file to file depending on the software package or designer, the data format commonly used by photo plotter and laser equipment is known as Gerber®.

3.1.2 Gerber® Format There are two standard Gerber® formats available:

- RS-274X – in this commonly used format the Gerber® aperture list is embedded in the data file.
- RS-274D – requires a data file listing the X-Y coordinates on the stencil where apertures are to be placed and formed, and a separate Gerber® aperture list that describes the size and shape of the various Gerber® apertures used to prepare the image.

3.1.3 Aperture List The aperture list is an ASCII text file containing D codes that define the size and shape for all apertures used within the Gerber® file. Without the aperture list, the software and photo plotting system cannot read the Gerber® data. Only the X-Y coordinates would be available with no size and shape data.

3.1.4 Solder Paste Layer The solder paste layer data is necessary to produce a stencil. If fiducials and/or outline information are required on the stencil, they should also be included in the solder paste layer.

3.1.5 Data Transfer Data can be transmitted to the stencil supplier via modem, FTP (file transfer protocol), e-mail attachment or disk. To ensure data integrity after transmitting and to reduce the large size of data files, it is suggested that the files be compressed prior to sending data. It is recommended that the full data file (the solder paste, solder mask, silk screen and copper layers) sent to the printed circuit board manufacturer be supplied to the stencil manufacturer. This allows the stencil manufacturer to optimize or make recommendations on aperture sizes based on actual land sizes.

3.1.6 Panelized Stencils In those cases where it is desired to have more than one image on the stencil, the stencil patterns will be panelized (step-and-repeat) and included in the data file.

3.1.7 Step-and-Repeat In those cases where more than one image of the same design is to be printed, the data file for stencil fabrication should contain the stencil design in the step-and-repeat array. In those instances where the data file does not contain the step-and-repeat pattern, a readme file, panel drawing, or order information should specify:

- Total number of steps for the final array.
- Number of steps in the X-direction along with dimensions from a specific feature to corresponding feature (such as fiducials, component land locations, etc.).
- Number of steps in the Y-direction along with dimensions from a specific feature to corresponding feature (such as fiducials, component land locations, etc.).

3.1.8 Image Orientation/Rotation In those cases where image orientation is not parallel to the frame or the step and repeat is not recti-linear (one or more images is rotated), the data for stencil fabrication should contain the oriented image. In those cases where it does not, a readme file, panel drawing or order information should specify this information (X- and Y-offsets) referencing stencil features.

3.1.9 Image Location To accommodate specific printers, the stencil image may have to be located in different positions inside the frame:

- (a) Center image
- (b) Center board/panel - requires board/panel outlines
- (c) Offset board/panel - requires board/panel outlines and reference locations

1. www.ipc.org

In those cases where this data is not included in the Gerber® data, a read me file, panel drawing or order information should specify this information referencing stencil features.

3.1.10 Identification Stencil should contain identification information such as part number, revision number, thickness, supplier's name and control number, date and method of manufacture.

3.2 Aperture Design Clause 3.2.1.2 can be applied to stencils used with either tin lead or lead free solder paste. Clauses 3.2.2 through 3.2.2.7 provide guidance for stencils intended for use with tin lead solder paste. Clauses 3.2.3 through 3.2.3.7 provide guidance for stencils intended for use with lead free solder paste. Clause 3.2.4 provides support for glue apertures for chip components, and Clause 3.2.5 for glue apertures for combination of chip components and leaded devices.

3.2.1 Aperture Size The volume of solder paste applied to the board is mainly determined by the aperture size and foil thickness. Solder paste fills the stencil aperture during the squeegee cycle of the print operation. Small aperture sizes may require smaller solder paste particle sizes. A typical guideline is a minimum of four to five particles of paste powder across the width of the aperture. The paste

should completely release to the lands on the board during the board/stencil separation cycle of the print operation. From the stencil viewpoint, the ability of the paste to release from the inner aperture walls to the board land depends primarily on these major factors:

- (1) The area ratios/aspect ratios for the aperture design
- (2) The aperture side wall geometry
- (3) The aperture wall finish
- (4) The stencil-board separation speed

3.2.1.1 Aperture Position The position of the aperture in the stencil is important so that the solder paste can be printed on the printed circuit land and not misregistered with respect to the land. A guideline is the mismatch should be less than 0.00254 mm [0.1 mil] per every 25.4 mm [1 inch] of aperture pattern or 0.0254 mm (1 mil) whichever is larger. In general most lead free solder pastes do not wet the land as well as tin lead solder pastes. If part of the land is left uncovered with solder paste during the printing operation it remains uncovered after reflow. Therefore stencil aperture to board land registration is very important.

3.2.1.2 Area Ratio/Aspect Ratio A general design guide for acceptable paste release should be >1.5 for aspect ratio and >0.66 for area ratio. Advances in stencil technology

Table 3-1 General Aperture Design Guideline Examples for Selective Surface-Mount Devices (Tin Lead Solder Paste)

Part Type	Pitch	Land Footprint Width	Land Footprint Length	Aperture Width	Aperture Length	Stencil Thickness Range	Aspect Ratio Range	Area Ratio Range
PLCC	1.25 mm [49.2 mil]	0.65 mm [25.6 mil]	2.00 mm [78.7 mil]	0.60 mm [23.6 mil]	1.95 mm [76.8 mil]	0.15 - 0.25 mm [5.91 - 9.84 mil]	2.4 - 4.0	0.92-1.53
QFP	0.65 mm [25.6 mil]	0.35 mm [13.8 mil]	1.50 mm [59.1 mil]	0.30 mm [11.8 mil]	1.45 mm [57.1 mil]	0.15 - 0.175 mm [5.91 - 6.89 mil]	1.7 - 2.0	0.71- 0.83
QFP	0.50 mm [19.7 mil]	0.30 mm [11.8 mil]	1.25 mm [49.2 mil]	0.25 mm [9.84 mil]	[1.20 mm] 47.2 mil	0.125 - 0.15 mm [4.92 - 5.91 mil]	1.7 - 2.0	0.69 - 0.83
QFP	0.40 mm [15.7 mil]	0.25 mm [9.84 mil]	1.25 mm [49.2 mil]	0.20 mm [7.87 mil]	[1.20 mm] 47.2 mil	0.10 - 0.125 mm [3.94 - 4.92 mil]	1.6 - 2.0	0.69 - 0.86
QFP	0.30 mm [11.8 mil]	0.20 mm [7.87 mil]	1.00 mm [39.4 mil]	0.15 mm [5.91 mil]	0.95 mm [37.4 mil]	0.075 - 0.125 mm [2.95 - 4.92 mil]	1.2 - 2.0	0.52 - 0.86
0402	N/A	0.60 mm [19.7 mil]	0.65 mm [25.6 mil]	0.45 mm [17.7 mil]	0.60 mm [23.6 mil]	0.125 - 0.15 mm [4.92 - 5.91 mil]	N/A	0.86-1.03
0201	N/A	0.4 mm [9.84 mil]	0.45 mm [15.7 mil]	0.23 mm [9.06 mil]	0.35 mm [13.8 mil]	0.075 - 0.125 mm [2.95 - 4.92 mil]	N/A	0.56 - 0.93
01005	N/A	0.200 mm [7.87 mil]	0.300 mm [11.81 mil]	0.175 mm [6.89 mil]	0.250 mm [9.87 mil]	0.063 - 0.089 mm [2.5 - 3.5 mil]	N/A	0.58 - 0.81
BGA	1.25 mm [49.2 mil]	CIR 0.55 mm [21.6 mil]		CIR 0.52 mm [20.45 mil]		0.15 - 0.20 mm [5.91 - 7.87 mil]	N/A	0.65 - 0.86
Fine-pitch BGA	1.00 mm [39.4 mil]	CIR 0.45 mm [15.0 mil]		SQ 0.42 mm [13.8 mil]		0.115 - 0.135 mm [4.53 - 5.31 mil]	N/A	0.65 - 0.76
Fine-pitch BGA	0.50 mm [19.7 mil]	CIR 0.25 mm [11.8 mil]		SQ Overprint 0.28 mm [11.0 mil]		0.075 - 0.125 mm [2.95 - 4.92 mil]	N/A	0.56 - 0.93

Note:

1. It is assumed that the fine-pitch BGA lands are not solder mask defined.
2. N/A implies that only the area ratio should be considered.

(finishing processes, electroform, etc.), may result in lower guideline ratios. These ratios will affect solder paste release. The graphs shown in Figures 3-1 through 3-4 may be a useful guide to select the proper stencil technology per given aperture sizes and area ratios for 4, 5, 6 and 8 mil thick stencils. These graphs apply to tin lead as well as lead free solder pastes.

Note that Figures 3-1 through 3-4 are general design guides based on area ratios. It must be recognized that there are a wide variety of stencils available in the industry made with electroform, laser, chemical etch and high-precision processes. It is quite possible that some electroform stencils may not perform satisfactory with area ratios between 0.5 and 0.66. On the other hand it is possible that some laser-

cut stencils with post processing do perform satisfactory with area ratios between 0.5 and 0.66. Likewise it is possible that some chemical etch stencils using high precision processes will perform satisfactory with area ratios of 0.66 to 0.9.

When the stencil separates from the board, paste release encounters a competing process. Solder paste will either transfer to the land on the board or stick to the aperture side walls. When the area is greater than 0.66 of the inside aperture wall area, a complete paste transfer should occur for both laser and electroform stencils.

Both area ratio and aspect ratio are illustrated in Figure 3-5, using the formulas underneath the figure.

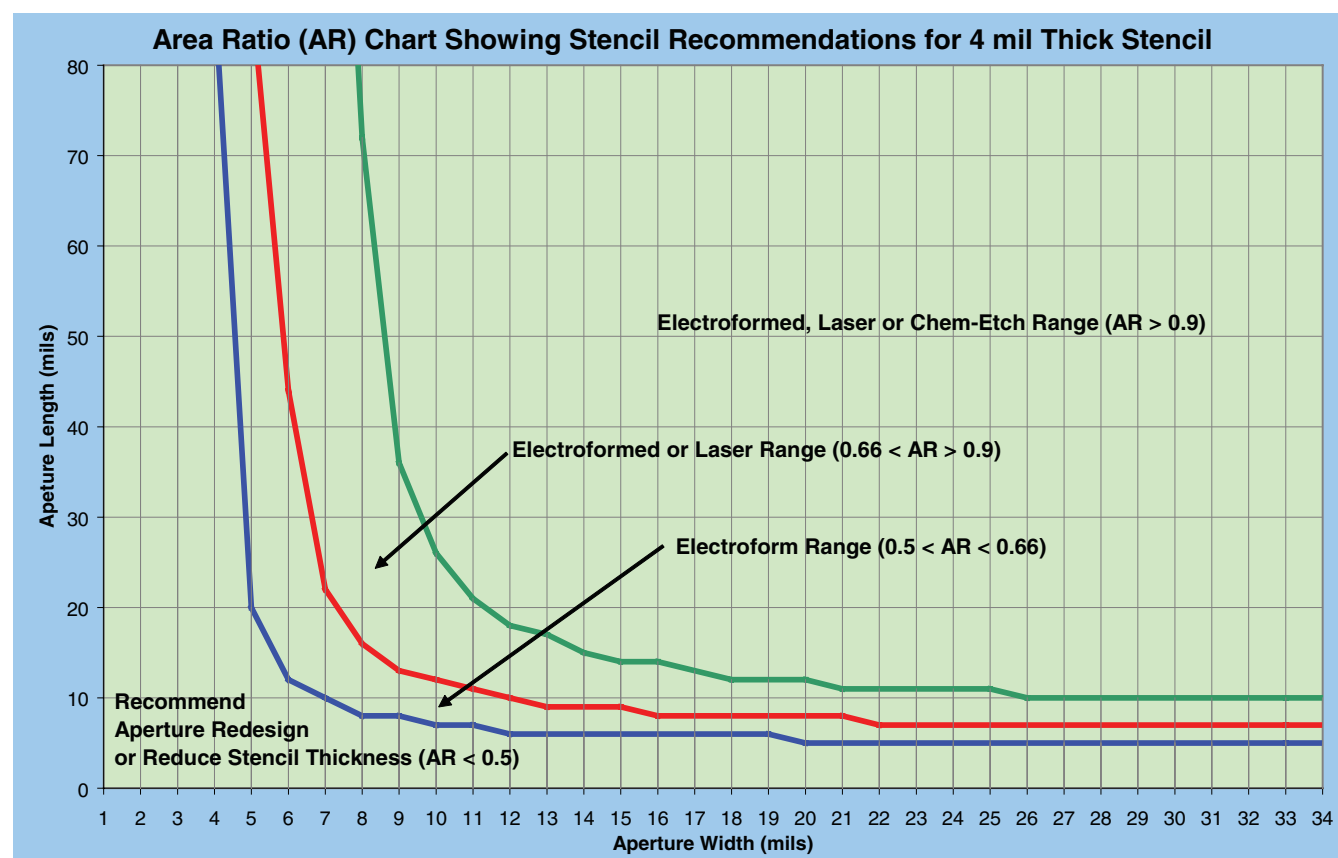


Figure 3-1 Area Ratio Chart Showing Recommendations for a 4 mil Thick Stencil

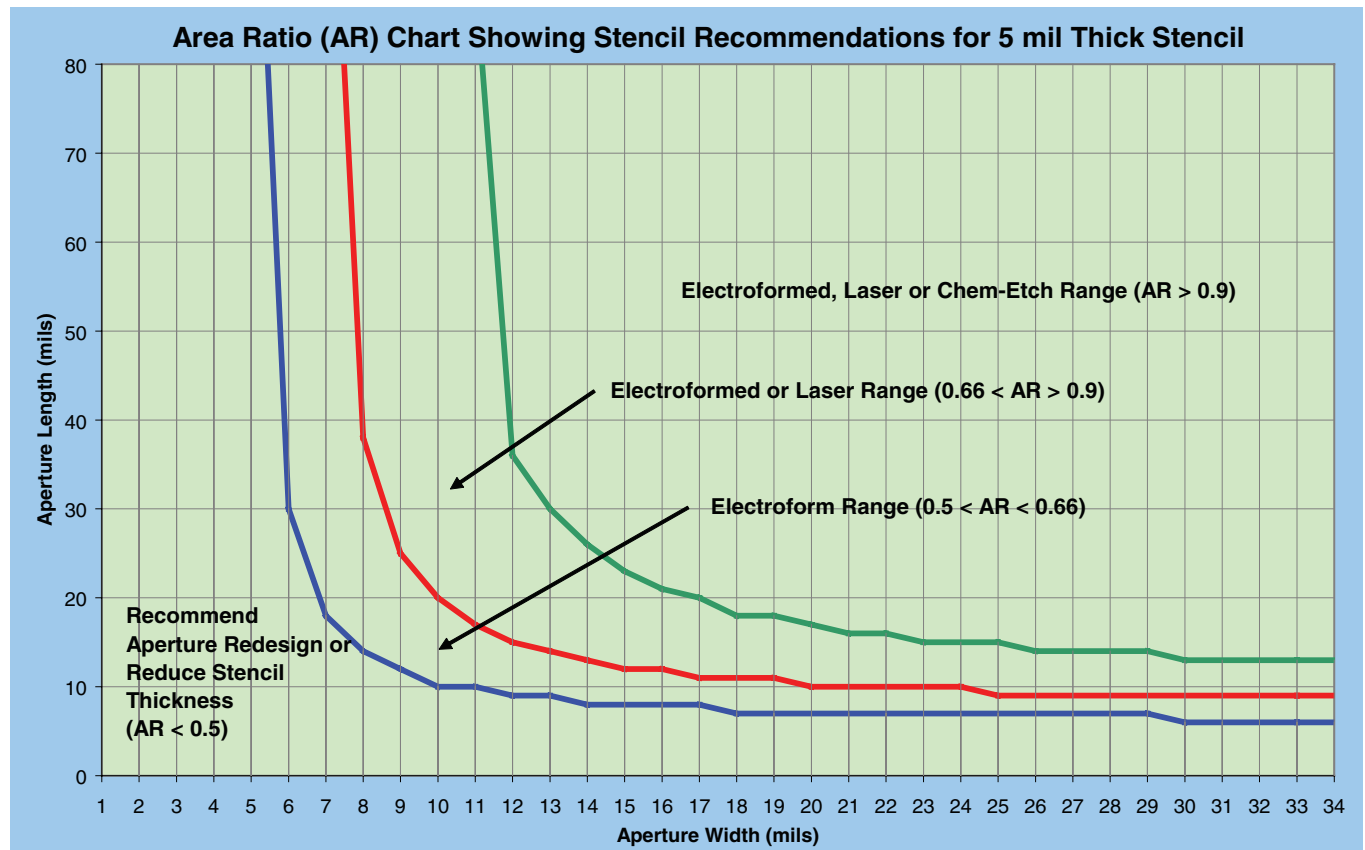


Figure 3-2 Area Ratio Chart Showing Recommendations for a 5 mil Thick Stencil

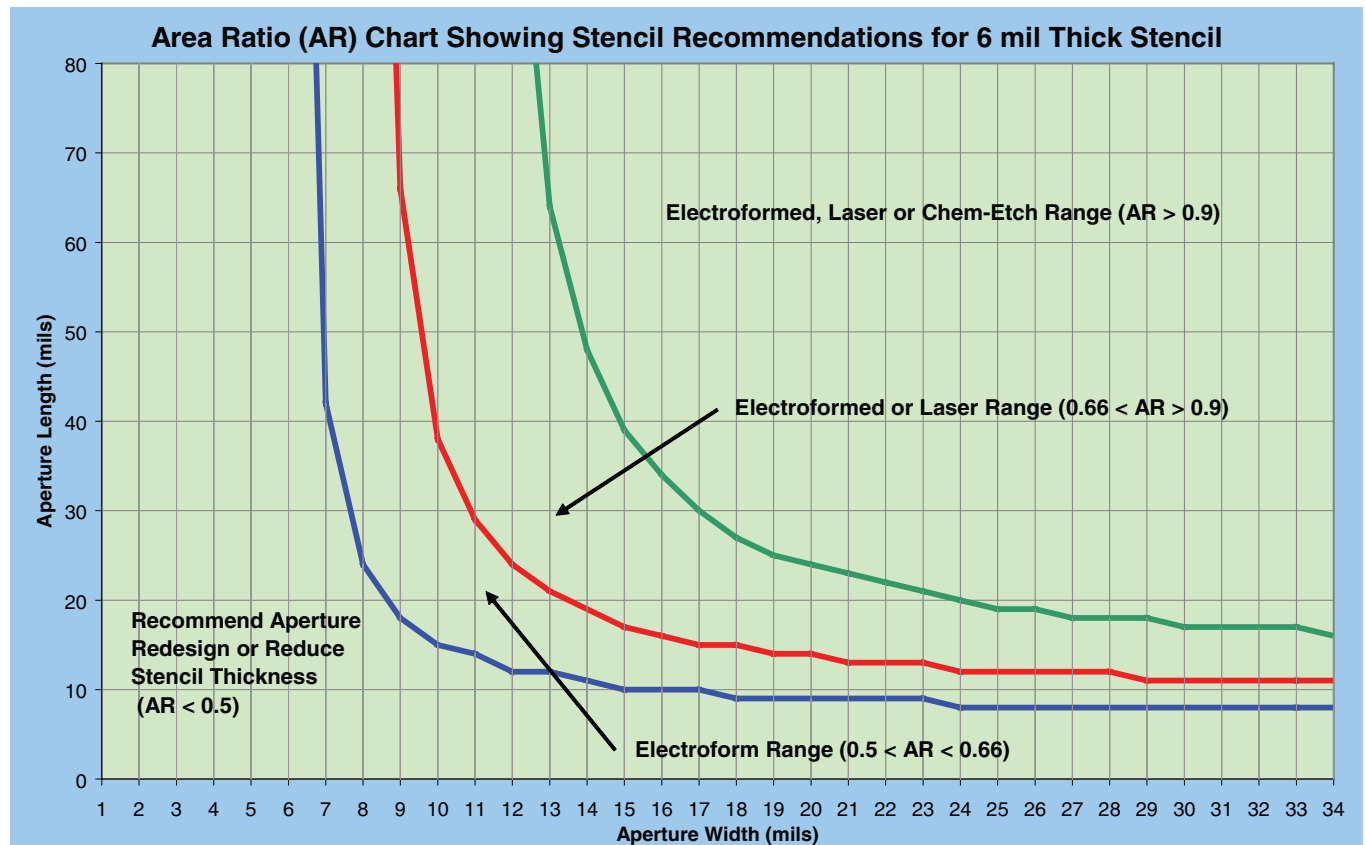


Figure 3-3 Area Ratio Chart Showing Recommendations for a 6 mil Thick Stencil

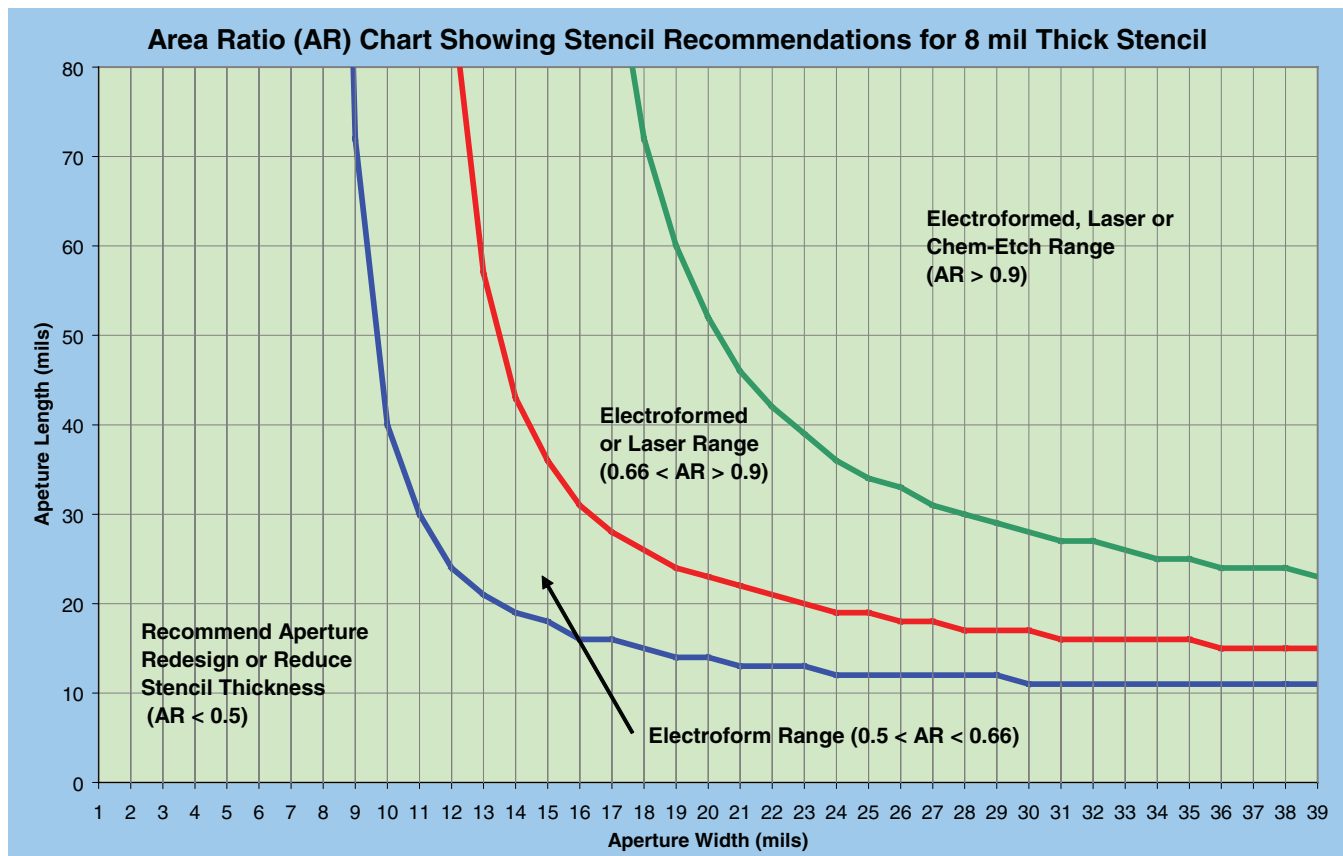


Figure 3-4 Area Ratio Chart Showing Recommendations for a 8 mil Thick Stencil

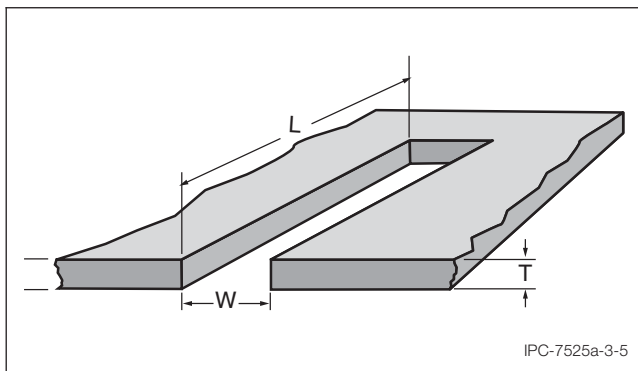


Figure 3-5 Cross-Sectional View of A Stencil

$$\text{Aspect Ratio} = \frac{\text{Width of Aperture}}{\text{Thickness of Stencil}} = \frac{W}{T}$$

$$\text{Area Ratio} = \frac{\text{Area of Aperture}}{\text{Area of Aperture Walls}} = \frac{L \times W}{2 \times (L + W) \times T}$$

3.2.2 Aperture Size Versus Board Land Size for Tin Lead Solder Paste As a general design guide, the aperture size should be reduced compared to the board land size. The stencil aperture is commonly modified with respect to the original land design. Reductions in the area or changes in aperture shape are often desirable to enhance the processes of printing, reflow, or stencil cleaning. For instance, reducing the aperture size will decrease the possibility of stencil aperture to board land misalignment. This reduces the chance for solder paste to be printed off the land, which

may lead to solder balls or solder bridging. Having a radiused corner for all apertures can promote stencil cleaning.

3.2.2.1 Leaded SMDs For leaded SMDs, e.g., J-leaded or gull-wing components with 1.3 - 0.4 mm [51.2 - 15.7 mil] pitch, the reduction is typically 0.03 - 0.08 mm [1.2 - 3.1 mil] in width and 0.05 - 0.13 mm [2.0 - 5.1 mil] in length.

3.2.2.2 Plastic BGAs Reduce circular aperture diameter by 0.05 mm [2.0 mil].

3.2.2.3 Ceramic Grid Arrays Ceramic Grid Array packages require a specific solder paste volume to ensure long-term reliability of the solder joint. Greater volume is required for ceramic ball grid arrays than for ceramic column grid arrays. Information regarding proper solder paste volumes for these packages can be found in IPC-7095.

3.2.2.4 Fine-Pitch BGA and CSP Make the apertures square with the width of the square equal to, or 0.025 mm [0.98 mil] less than, the diameter of the land circle on the board. The square should have rounded corners. A guideline is 0.06 mm [2.4 mil] radiused corners for a 0.25 mm [9.8 mil] square and 0.09 mm [3.5 mil] corners for a 0.35 mm [14 mil] square.

3.2.2.5 Chip Components - Resistors and Capacitors Several aperture geometries are effective in reducing the

occurrence of solder balls. All these designs are aimed at reducing excess solder paste trapped under the chip component. The most popular designs are shown in Figures 3-6, 3-7 and 3-8. These designs are commonly used for no-clean processes.

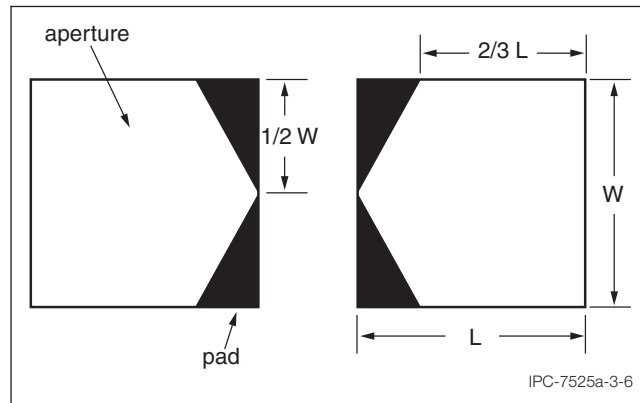


Figure 3-6 Home Plate Aperture Design

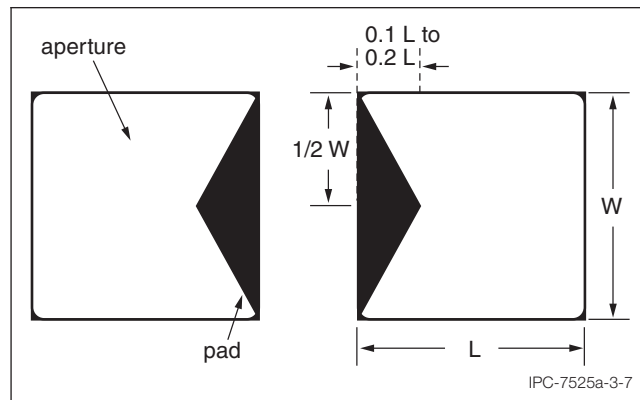


Figure 3-7 Bow Tie Aperture Design

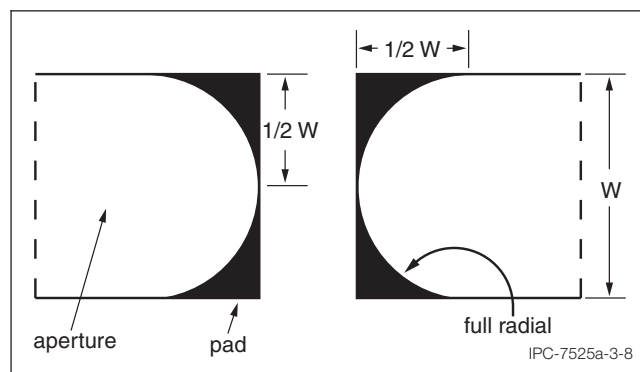


Figure 3-8 Oblong Aperture Design

3.2.2.6 MELF, Mini-MELF and Chip Components For MELF and mini-MELF as well as chip components, “C” shaped apertures are suggested (see Figure 3-9) but care has to be taken to prevent the parts from bouncing off their locations before reflow due to minimal paste contact and shaking conveyors. Dimensions of these apertures should be designed to match the geometry of component terminals.

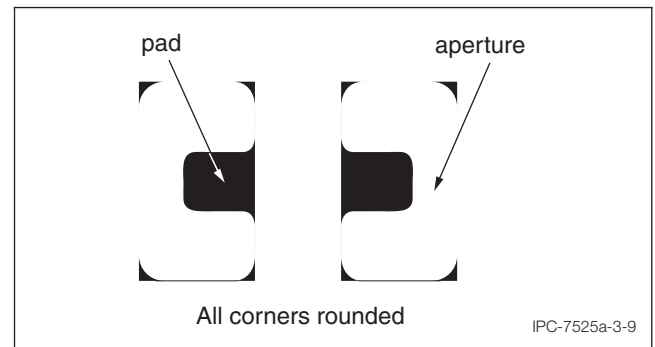


Figure 3-9 Aperture Design for MELF Components and Chip Components

3.2.2.7 QFN/LCC Devices Aperture sizes for the lead lands are the same size as recommended for the QFPs in 3.1 with the exception of the corner apertures. These apertures should be 1.25 to 1.5 times wider than the board land to assist in keeping the package from rotating during reflow.

The apertures for the Heat Sink/Ground Plane should be reduced from 50% to 80% of the area of the ground plane. This can be accomplished by window paning the apertures as shown in Figure 3-10.

If vias are imbedded in the ground land design, it is recommended that the web of the stencil grid be designed over the via to prevent the solder paste being screened directly into the via. This will prevent solder from wicking into the via. Solder wicking may not allow you to achieve a >50% solder coverage of the ground plane area.

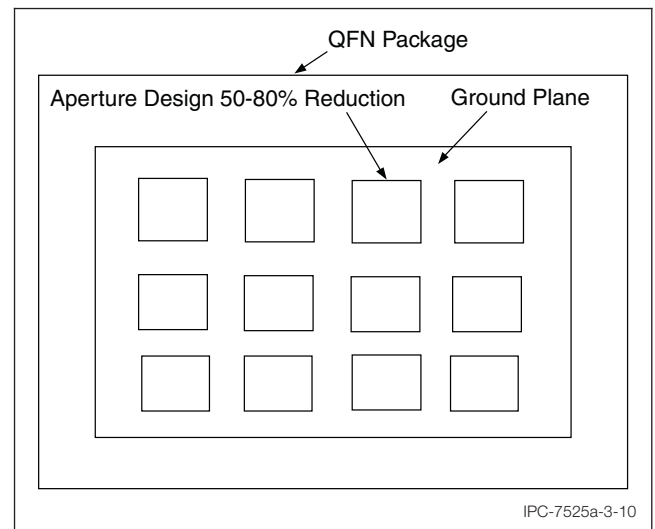


Figure 3-10 Window Pane Design for Ground Plane

3.2.3 Aperture Size versus Board Land Size for Lead Free Solder Paste As a general design guide, the aperture size should be very close to one to one compared to the board land size. This is done to assure complete coverage of the land with solder after reflow. Some slight reduction (0.5 mils (0.0127 mm) per side of land, for example) is acceptable since pushing the component into the solder

paste will cause the paste to spread and cover the land. Reduction of the aperture size for the ground plane of QFN or LCC devices is an exception and is desirable. Radiused corners are also acceptable as it reduces the chance of solder paste sticking in sharp corners of the aperture.

3.2.3.1 Leaded SMDs For leaded SMDs, e.g., J-leaded or gull-wing components with 1.3 - 0.4 mm [51.2 - 15.7 mil] pitch, the reduction is typically 0.254 [1.0 mil] in width and no reduction in length.

3.2.3.2 Plastic BGAs No reduction in the aperture compared to the land.

3.2.3.3 Ceramic Grid Arrays Ceramic Grid Array packages require a specific solder paste volume to ensure long-term reliability of the solder joint. Greater volume is required for ceramic ball grid arrays than for ceramic column grid arrays. Information regarding proper solder paste volumes for these packages can be found in IPC-7095.

3.2.3.4 Fine-Pitch BGA and CSP Square aperture with the width of the square equal to, the diameter of the land circle on the board. The square should have rounded corners. A guideline is 0.06 mm [2.4 mil] radiused corners for a 0.25 mm [9.8 mil] square and 0.09 [3.5 mil] corners for a 0.35 mm [14 mil] square. The square aperture with rounded corners should be kept within the confines of the solder mask

3.2.3.5 Chip Components - Resistors and Capacitors

Several aperture geometries are effective in reducing the occurrence of solder balls. All these designs are aimed at reducing excess solder paste trapped under the chip component. The most popular designs are shown in Figure 3-9 (same aperture design as the MELF diode) the C shaped aperture. This aperture design reduces the amount of solder paste under the Chip Component but maintains land coverage on the peripheral of the lands.

3.2.3.6 MELF, Mini-MELF Components For MELF and Mini-MELF components, “C” shaped apertures are suggested (see Figure 3-9). Dimensions of these apertures should be designed to match the geometry of component terminals. This design can also be used for Chip Components.

3.2.3.7 QFN/LCC Devices Aperture sizes for the lead pads are either no reduction or a slight reduction typically 0.254 [1.0 mil] in width and no reduction in length with the exception of the corner apertures. These apertures should be 1.25 to 1.5 times wider than the board pad to assist in keeping the package from rotating during reflow.

The apertures for the Heat Sink/Ground Plane should be reduced from 50% to 80% of the area of the ground plane. This can be accomplished by window paning the apertures as shown in Figure 3-10.

3.2.4 Glue Aperture Chip Component The glue stencil is typically 0.15 - 0.2 mm [5.9 - 7.9 mil] thick. The glue aperture is placed in the center of the component solder lands. It is 1/3 the spacing between lands and 110% of the component width (see Figure 3-11).

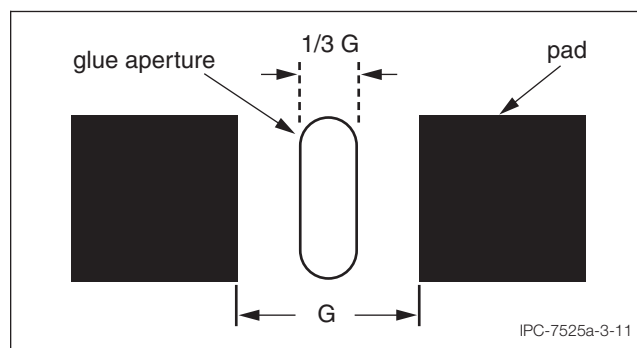


Figure 3-11 Glue Stencil Aperture Design

3.2.5 Glue Apertures for Combination of Chip Components and Leaded Devices

Chip components with a typical stand-off of between 0.102 - 0.127 mm [4 - 5 mils] require a stencil of 0.150 - 0.200 mm [5.9 - 7.9 mils] but leaded devices have much higher stand-offs ranging from 0.381 mm [15 mils] to more than 0.762 mm [30 mils]. In this case a thicker stencil is required. Figure 3-12 shows the off-sets for typical chip and leaded devices. Glue prints differently than paste in that by making the aperture small a defined height of glue is deposited from the glue aperture. Figure 3-13 shows a 0.381 mm [15 mil] thick stencil with a small aperture for printing 0.150 mm [5.9 mil] and a larger aperture for printing 0.381 mm [15 mil] of glue. In cases where higher glue prints are necessary (for instance 0.762 mm [30 mil]) a special stencil with a glue reservoir may be used. This is shown in Figure 3-14.

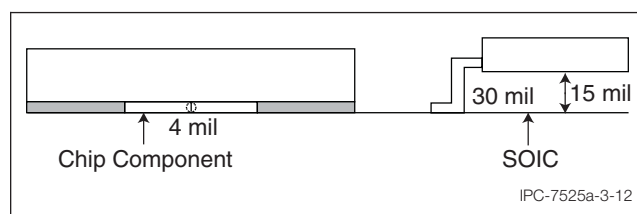


Figure 3-12 Chip Component and SOIC Present on Board

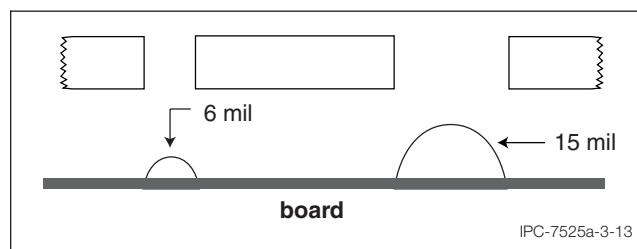


Figure 3-13 Print Only Mode 15 mil Thick Stencil

3.3 Mixed Technology Surface-Mount/Through-Hole (Intrusive Reflow) It is desirable to have a process where SMT and THT devices can both be:

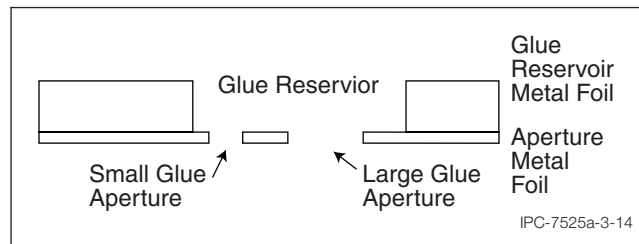


Figure 3-14 Glue Stencil with Glue Reservoir

- (1) Provided with printed solder paste
- (2) Placed on or in the board
- (3) Reflowed together.

The objective of stencil printing of solder paste for the intrusive reflow process is to provide enough solder volume after reflow to fill the hole and create acceptable solder fillets around the pins. Table 3-2 shows process window for a typical intrusive soldering process.

3.3.1 Solder Paste Volume A simple equation listed below describes the volume of solder paste required as shown in Figure 3-15. It is desirable to keep the copper land around the hole as small as possible. It is also desirable to keep the clearance between the pin and the through-hole and the length of the pin as small as possible. By doing this less solder paste volume will be required. Following are three stencil designs used to deliver the through-hole solder paste:

- (1) Non-step stencil
- (2) Step stencil
- (3) Two-print stencil

$$V = T_S (L_O \times W_O) + V_H$$

$$= \frac{1}{S} \{ T_B (A_H - A_P) + (F_T + F_B) + V_P \}$$

Where:

- V is volume of solder paste required
- V_P is the solder volume left on the top and/or bottom board land
- S is the solder paste shrink factor
- A_H is the cross-sectional area of the through-hole
- A_P is the cross-sectional area of the through-hole pin
- T_B is the thickness of the board
- $F_T + F_B$ is the total fillet volume required
- T_S is the thickness of the stencil foil
- L_O is the length of the overprint aperture
- L_P is the length of the pad

W_O is the width of the overprint aperture

W_P is the width of the land

V_H is solder paste filling the hole during the printing operation

Note: Solder paste volume filling the hole can vary from 0% to 100% depending on the print setup. Contained paste transfer heads are effective in delivering close to 100% or even more while metal squeegee blades with a high attack angle and high print speed will deliver minimum paste into the board hole.

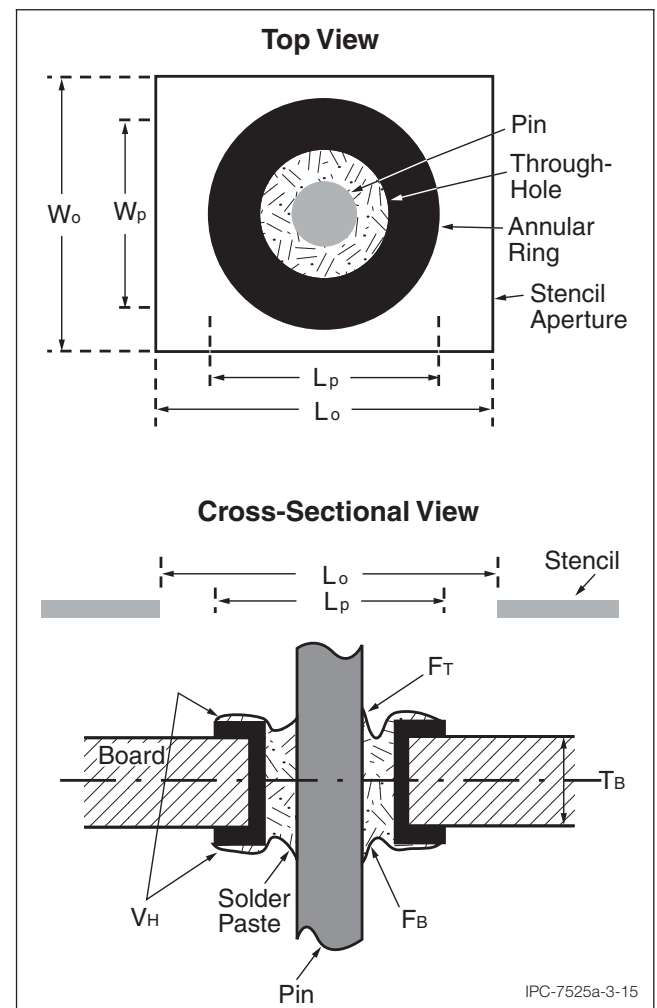


Figure 3-15 Through-Hole Solder Paste Volume

3.3.1.1 Overprint Without Step This is the stencil of choice when it can deliver enough solder paste to satisfy the through-hole requirement. A cross section of this type stencil is shown in Figure 3-16.

Table 3-2 Process Window for Intrusive Soldering - Maximum Limits Desirable

	Maximum Limits	Desirable
Hole Diameter	0.65 - 1.60 mm [25.6 - 63.0 mil]	0.75 - 1.25 mm [29.5 - 49.2 mil]
Lead Diameter	Up to hole diameter minus 0.075 mm [2.95 mil]	Hole diameter minus 0.125 mm [4.92 mil]
Paste Overprinting	6.35 mm [250 mil]	<4.0 mm [157 mil]
Stencil Thickness	0.125 - 0.635 mm [4.92 - 25.0 mil]	0.15 mm [7.87 mil], 0.20 mm [5.91 mil] for fine-pitch

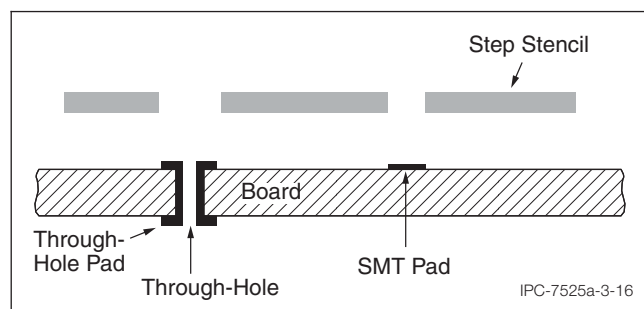


Figure 3-16 Overprint without Step

An example of when this stencil could be used is a two row connector on 2.5 mm [98.4 mil] pitch with 1.1 mm [43.3 mil] diameter through-holes, 0.9 mm [35.4 mil] diameter pins, 1.2 mm [47.2 mil] thick board and no other components within 3.8 mm [150 mil] of the through-hole openings. An overprint stencil aperture of 2.2 mm [86.6 mil] wide and 5.1 mm [200 mil] long with a stencil foil thickness of 0.15 mm [5.91 mil] can deliver sufficient solder paste.

3.3.1.2 Overprint With Step If the board is thicker, the hole is bigger, or the pin is smaller, more solder paste volume will be required. In this case, a step stencil may be needed to provide sufficient solder paste volume for the THT parts without providing too much paste on the SMT lands. An example of this type stencil is shown in Figure 3-17. K1 and K2 are keep-out distances. K2 is the distance between the through-hole aperture and the step edge. As a general design guide K2 can be as low as 0.65 mm [25.6 mil]. K1 is the distance from the step edge to the nearest aperture in the step-down area. As a general design guide, K1 should be 0.9 mm [35.4 mil] for every 0.025 mm [0.98 mil] of step-down thickness. As a simple guideline, K1 should be 36x the step-down thickness. For example, a 0.2 mm [7.9 mil] stencil foil with a step down to 0.15 mm [5.9 mil] would require a K1 keep-out distance of 1.8 mm [70.9 mil]. It is also possible to put the step on the contact side of the stencil instead of the squeegee side. This is shown in Figure 3-18. This type of step is sometimes more convenient when using metal squeegee blades and is highly recommended for contained paste transfer heads. The same keep-out rules apply.

When placing the step on the contact side of the foil, verify there are no ultra-fine pitch devices in close proximity to the edge of the step area.

3.3.1.3 Two-Print Stencil Some through-hole devices have small pins with large holes or dense spacing with thick boards. In either case insufficient solder paste volume is deliverable using the first two stencil designs. The two-print stencil can deliver large amounts of solder paste into the through-holes. In this design, a normal surface-mount stencil, typically 0.15 mm [5.9 mil] thick, is used to print

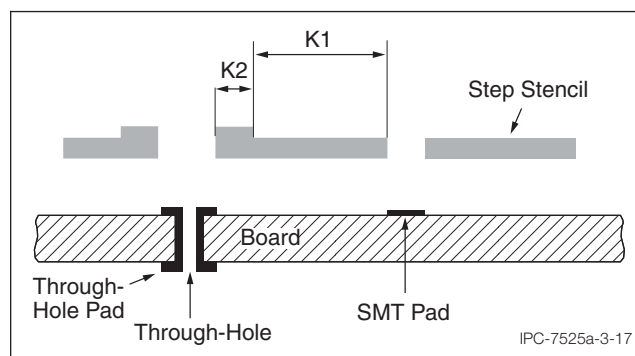


Figure 3-17 Overprint with Step (Squeegee Side)

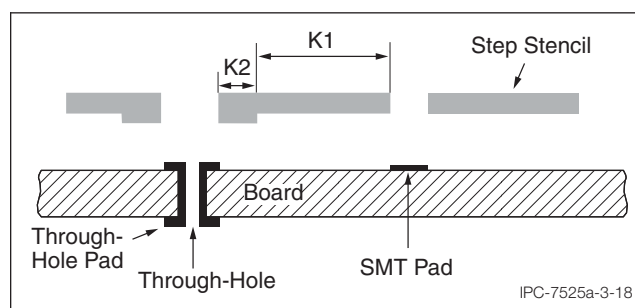


Figure 3-18 Overprint with Step (Contact/Board Side)

to the surface-mount lands. While the surface-mount paste is still tacky, a thick stencil is used to print the through-hole paste. Normally this requires a second stencil printer set up in line to perform this printing. This stencil can be as thick as required. However, 0.4 to 0.75 mm [16 to 30 mil] is typical. When stencil foil thickness requirements exceed 0.5 mm [20 mil], laser cut electropolished apertures provide better paste release and overall print performance due to the excellent wall geometry. The contact side of this stencil foil is relief etched at least 0.25 mm [9.84 mil] deep in any area where solder paste for has been previously printed on surface-mount lands. A cross section of the two-print through-hole stencil is shown in Figure 3-19.

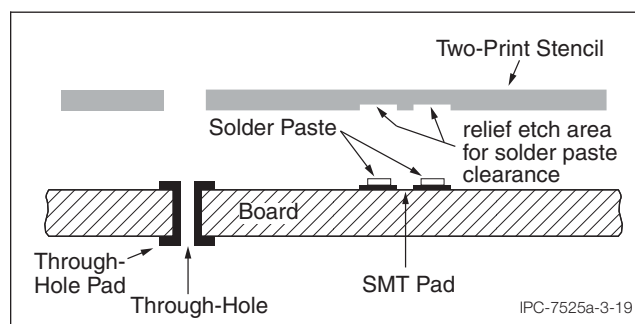


Figure 3-19 Two-Print Through-Hole Stencil

3.4 Mixed Technology Surface-Mount/Flip Chip A sample application for this technology is a PCMCIA card having flip chips, TSOPs, and chip components. It is desirable to place flip chip and SMT components on the card and reflow all the components simultaneously.

3.4.1 Two-Print Stencil for Surface-Mount/Flip Chip

The two-print stencil configuration can perform this task. The first step in this process is to print flip chip solder paste or flip chip flux on the board flip chip land sites. A stencil to do this is normally 0.05 or 0.075 mm [2.0 or 3.0 mil] thick with 0.13 to 0.18 mm [5.12 to 7.09 mil] apertures. While the flip chip paste/flux is still tacky, the surface mount stencil is used to print solder paste to the remaining surface mount lands. An example of this stencil would be one that is 0.18 mm [7.09 mil] thick with a relief etch of 0.10 mm [3.93 mil] in the area of the flip chip paste/flux. An example of a two-print stencil for this application is shown in Figure 3-20.

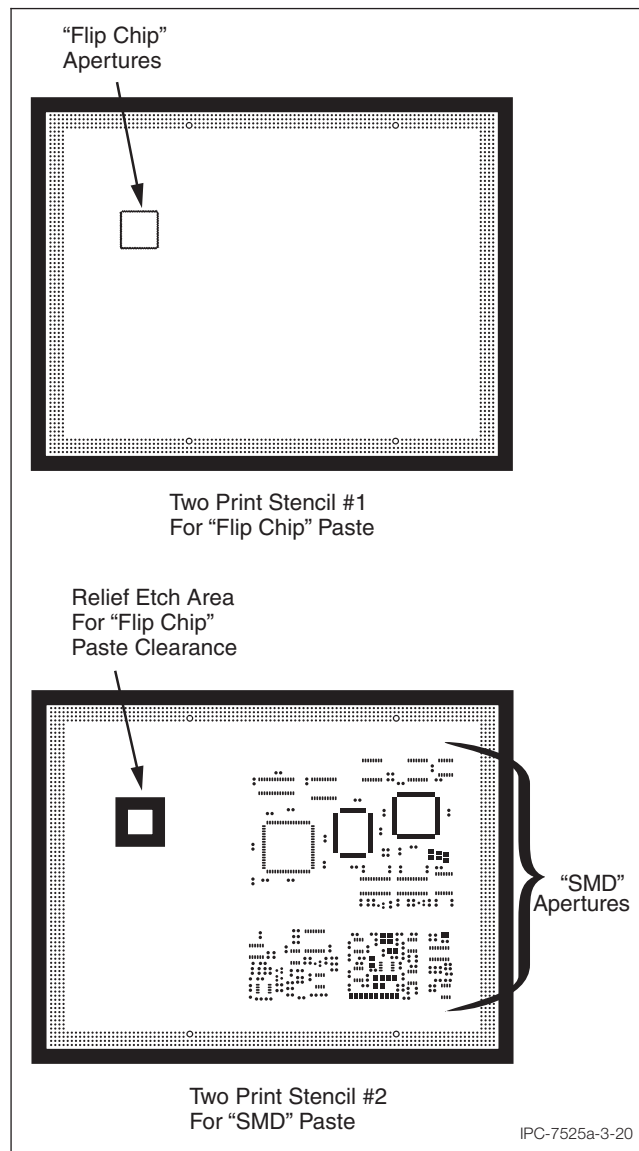


Figure 3-20 Two-Print Stencil for Mixed Technology

3.5 Step Stencil Design There are several applications where a stencil with multiple foil thicknesses may be desirable. These designs are outlined below.

3.5.1 Step-Down Stencil This type of stencil is useful when it is desirable to print fine-pitch devices using a thinner stencil foil but print other devices using a thicker stencil foil. For example there may be a fine-pitch BGA of 0.5 mm [20 mil] pitch that requires a 0.1 mm [3.9 mil] foil thickness to achieve an area ratio of greater than 0.66 but at the same time there are other devices on the same board that need a thickness of 0.13 to 0.15 mm [5.1 to 5.9 mil]. The stencil design would have a step area at 0.1 mm [3.9 mil] thick in the fine-pitch BGA portion while the remainder of the stencil foil is 0.15 mm [5.9 mil] thick. The step can be on the squeegee side or on the contact side. See 3.3.1.2 for keep-out design guidelines.

3.5.2 Step-Up Stencil This type stencil is useful when it is desirable to print thicker solder paste in a small portion of the stencil. An example would be a ceramic BGA where it is necessary to get 0.2 mm [7.9 mil] paste height because of ball coplanarity but 0.15 mm [5.9 mil] height on all other surface-mount component lands. In this case the stencil foil is stepped up from 0.15 mm [5.9 mil] to 0.2 mm [7.9 mil] in the area of the ceramic BGA. Another example is a through-hole edge connector that requires additional solder paste volume. In this case the stencil foil may be 0.15 mm [5.9 mil] thick everywhere except in the area of the edge connector where the stencil foil may be 0.3 mm [12 mil] thick.

3.5.3 Step Stencil for Contained Paste Transfer Heads As a general design guide; step should not exceed 0.05 mm [2.0 mil].

3.5.4 Relief-Etch Stencil This type of stencil has relief step pockets on the contact/board side of the stencil foil. There are several applications where relief-etch stencils are useful. Some examples are:

- Relief pocket for a bar code label on the board. The stencil foil might be 0.15 mm [5.9 mil] thick with a 0.08 mm [3.1 mil] relief for the bar code label.
- Test via relief pockets. The stencil foil has relief pockets over each raised test via to allow the stencil foil to sit flat and gasket to the board.
- Two-print stencil. This stencil foil has deep relief pockets in the areas where surface-mount solder paste was previously printed (see 3.3.1.3 and 3.4.1). An example of this stencil would be a stencil 0.5 mm [20 mil] thick for printing paste in and around through-hole with relief step on the contact side 0.3 mm [12 mil] thick to clear surface mount solder paste previously printed.
- Use of solder mask pedestals at the corners of ceramic components. A relief etch on the stencil foil provides good gasketing. The standoff of ceramic leadless components can be increased to accommodate cleaning under the component and to increase the length of solder joint.

3.6 Fiducials Depending on the vision system, fiducials are located on the squeegee or contact side and engraved or filled with a contrasting color epoxy. Typically, they are solid, round dots 1.0 to 1.5 mm [39.4 to 59.1 mil] in diameter. They may be half-etched, laser engraved or etched through the stencil.

3.6.1 Global Fiducials Fiducials that are placed a minimum of 5 mm [0.20 in] from the board corners in three locations.

3.6.2 Local Fiducials Fiducials that are placed near critical components, e.g., fine-pitch QFP are useful for pick and place machines, but useless for stencil printing. For the printing process the best fiducials are as far apart as possible.

4 STENCIL FABRICATION

4.1 Foils Stainless steel is the preferred metal for chemical etch and laser cut technology. Other metals, as well as plastics, may be specified. For electroform technology, a hard nickel alloy is preferred.

4.2 Frames Refer to the stencil printer operation manual for available frame sizes. Frames may be tubular or cast aluminum with the tensioned mesh border permanently mounted using an adhesive. Some foils can be mounted into a tensioning master frame and do not require a mesh border or a permanent fixturing of the foil to the frame.

4.3 Stencil Border Polyester is the standard material; stainless steel is optional.

4.4 Stencil Fabrication Technologies The fabrication process for stencils may involve additive or subtractive methods. In additive processes such as electroforming, metal is added to form stencil foils. In subtractive processes, material is removed from foils to create apertures. Laser cut and chemical etch are examples of subtractive processes.

4.4.1 Chemical Etch Chemically etched stencils are produced using photo-imageable resist laminated on both sides of metal foils cut to specific frame sizes. A double-sided phototool, held in precise alignment usually with registration pins, is used to expose the stencil aperture image onto the resist. Aperture images exposed on the resists are reduced in size compared with the desired aperture dimensions to account for the etch factor. The etch factor describes the amount of lateral etching that takes place as the chemical etches through the thickness of metal foil. The exposed resist is then developed, leaving bare metal where apertures are desired. The metal foil is etched from both sides in a liquid chemical, creating apertures as specified. The remaining resist is then stripped away and a stencil foil is produced.

Chemical etching is also used to provide a step down or step up area of the stencil, for standard stencils (does not include additive processes stencils). This process set up is critical to provide a smooth surface for the paste to roll on and squeegee to wipe clean in the step area.

4.4.2 Laser-Cut Stencils Laser-cut stencils are produced from data prepared by software of the laser equipment. Unlike chemically etched stencils, no phototool is required. A tapered aperture wall is an inherent part of laser cut stencils. Unless otherwise specified, the stencil is cut so that the apertures are larger on the contact side than on the squeegee side (see 4.4.5). Laser cutting can also be done in Kapton.

4.4.3 Electroform Electroforming is an additive stencil fabrication method utilizing photo-imageable resist and an electroplating process. Photo-imageable resist is placed on a metal mandrel. Thickness of the resist is greater than the final stencil thickness desired. The apertures are imaged onto the resist and the resist is developed, leaving resist pillars where apertures are desired. The mandrel with resist pillars is placed in a nickel plating tank where nickel is electroplated onto the mandrel. When the desired stencil thickness is reached, the mandrel is removed from the plating tank. Lastly, the resist pillars are stripped and the nickel stencil foil is separated from the mandrel.

4.4.4 Hybrid Where a mixture of standard and fine-pitch assemblies is present on a board, the stencil fabrication process may be a combination of laser cut and chemical etch. The stencils produced are referred to as laser-chem combination or hybrid stencils.

4.4.5 Trapezoidal Apertures A trapezoidal aperture may be used to enhance solder paste release. In chemical etch processes, the trapezoidal dimension, Z , (see Figure 4-1) can be specified. For laser cut or electroform processes trapezoidal aperture is an inherent part of process. Stencil vendors should be contacted for dimensions.

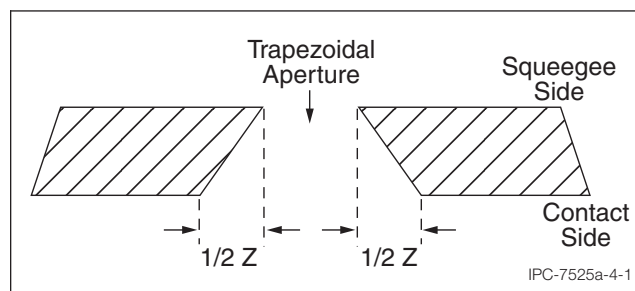


Figure 4-1 Trapezoidal Apertures

4.4.6 Additional Options Further processing may be desired on certain methods of stencil fabrication to reduce friction between solder paste and side walls for improved paste release. Choices of further processing are:

- **Polishing:** A subtractive process; either chemical polishing or electropolishing process.
- **Nickel Plating:** An additive process applying a thin layer of nickel on the stencil.

5 STENCIL MOUNTING

5.1 Location of Image on Metal The image is centered or offset in the stencil. Board corner marks or the board outline can be used to indicate its location. Global fiducials or the actual board outline is to be used for alignment. Where more than one board or panel image is placed on one stencil, a minimum of 50 mm [2.0 in] is recommended between the images.

5.2 Centering It is recommended that the stencil be centered on the frame for most uniform mechanical tensioning and print results. The image can be offset to meet specific requirements of the stencil printer.

5.3 Additional Design Guidelines Unless otherwise specified, additional design guidelines are:

- Minimum 20 mm [0.79 in] border is recommended from the edge of frame to the edge of metal.
- Minimum 50 mm [2.0 in] from the inside edge of glue border to the edge of image is suggested for solder paste storage and squeegee travel.

6 STENCIL ORDERING

Stencil information is typically communicated between the user and supplier through an order form (or checklist) created by the supplier. File data, types of material, fabrication methods, and special requests are examples of what is typically included on an order form (see Appendix A).

7 STENCIL USER'S INSPECTION/VERIFICATION

After receiving a stencil from the supplier, users are recommended to generate an inspection checklist to verify that the stencil has been fabricated correctly and that no damage has occurred during the shipping process. The following items can be used as a guideline for inspecting an incoming stencil:

- The foil should be inspected for chemical corrosion.
- The foil should be inspected for handling damage (e.g., dents, creases, metal voids).

- Tension of border should be checked.
- Correct spacing between the image and the frame should be verified (based on printer manufacturer's specification). A printed wiring board or transparent image of the board (e.g., mylar film with backlighting equipment) should be held up against the image of stencil to check for correct spacing between the board and the edge of stencil frame.
- The image of the stencil should be observed to match the image of the board. Modifications of aperture size and/or shape should be verified.
- Border should be checked for proper adhesion to the foil and for any handling damage.
- The size, type, flatness, etc., of the frame should be checked.
- Correct part number and revision number, etched or engraved in the stencil should be verified.
- Foil thickness should be verified.
- For a step stencil, the correct step level should be verified.
- Fiducial quality and location (correct side of foil) should be inspected.
- The stencil cleanliness should be verified to be free of lint, fibers or loose particles.

8 STENCIL CLEANING

Proper setup and cleaning of stencil helps ensure continued repeatable printing performance. Cleaning processes need to be compatible with materials used in the manufacture of stencils. Paste or adhesive manufacturers, stencil manufacturers, and cleaning equipment manufacturers should be consulted as life of stencils, integrity of fiducials, and quality of glue bead may be affected.

9 END OF LIFE

Stencils should be inspected periodically for damage that would contribute to decreased printing performance. Refer to Section 7 for inspection guidelines.

Users are invited to submit recommendations based on their experience for determining end of life. The committee is particularly interested in repeatable methods that measure tension on the stencil after use. These will be considered for a future amendment or revision.

APPENDIX A: EXAMPLE ORDER FORM

Customer / Contact Name: _____

Ship To: _____ Bill To: _____

Shipping Method: _____ Due Date: _____

Stencil Part Number and Revision Number: _____
(to be half-etched or engraved on squeegee / contact side of stencil)

File(s) Name: _____ File Type: _____

Data Transmitted By: ☐ Modem ☐ Email ☐ FTP ☐ DiskStencil Fabrication Method: ☐ Chemical Etch ☐ Laser Cut ☐ Laser-Chem Hybrid
☐ Electroform ☐ _____

Frame Size: _____

Provided By: ☐ Customer ☐ Stencil SupplierFrame Coated: ☐ Yes ☐ No

Metal Thickness: _____

Step-Down Thickness: _____ (Drawing Required for Step Locations)

Metal Type: ☐ Stainless Steel ☐ _____Location of Pattern on Stencil: ☐ Center Image ☐ Center Board ☐ Offset (Drawings Required)Fiducials: ☐ None
☐ Half Etch / Engraved Contact Side
☐ Half Etch / Engraved Squeegee Side
☐ Full Etch / Cut Through, Not Filled
☐ Full Etch / Cut Through, Filled with Contrasting Epoxy☐ Panelization Provided By: ☐ Customer ☐ Stencil Supplier
Dimensions Required: _____☐ Step-and-Repeat Provided By: ☐ Customer ☐ Stencil Supplier
Dimensions Required: _____Border: ☐ Polyester ☐ Stainless SteelPolish: ☐ Yes ☐ NoNickel Plate: ☐ Yes ☐ No

Special Modifications, Editing, or Instructions: _____

(This page is authorized for copying/local reproduction.)



ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249
Fax: 847 615.7105

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

- ☐ This is a **NEW** term and definition being submitted.
☐ This is an **ADDITION** to an existing term and definition(s).
☐ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ☐ Not Applicable ☐ Required ☐ To be supplied

☐ Included: Electronic File Name: _____

Document(s) to which this term applies: _____

Committees affected by this term: _____

Office Use	
IPC Office	Committee 2-30
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: <input type="checkbox"/> Accepted <input type="checkbox"/> Rejected
Revision Inclusion: _____	<input type="checkbox"/> Accept Modify
IEC Classification	
Classification Code • Serial Number	
Terms and Definition Committee Final Approval Authorization: Committee 2-30 has approved the above term for release in the next revision.	
Name: _____ Committee: IPC 2-30 Date: _____	

This Page Intentionally Left Blank

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel: 847-615-7100

fax: 847-615-7105

www.ipc.org

e-mail: answers@ipc.org

IPC World Wide Web Page www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignersCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, job opportunities and certification. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Trainingnews@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC Training Products.

leadfree.ipc.org

This forum acts as a peer interaction resource for staying on top of lead elimination activities worldwide and within IPC.

IPC_New_Releases@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC publications, updates and standards.

ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e. <mail list> @ipc.org), as it would be distributed to all the subscribers.

Example for subscribing:

To: LISTSERV@IPC.ORG

Subject:

Message: subscribe TechNet Joseph H. Smith

Example for signing off:

To: LISTSERV@IPC.ORG

Subject:

Message: signoff DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words, if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org. Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:

To: TechNet@IPC.ORG

Subject: <your subject>

Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori

tel: 847-597-2815

fax: 847-615-5615

e-mail: sasako@ipc.org

www.ipc.org/emailforums

Education and Training

IPC conducts local educational workshops and national conferences to help you better understand conventional and emerging technologies. Members receive discounts on registration fees. Visit www.ipc.org to see what programs are coming to your area.

IPC Certification Programs

IPC provides world-class training and certification programs based on several widely-used IPC standards, including IPC-A-600, IPC-A-610, IPC/WHMA-A-620, J-STD-001 and IPC-7711A/7721A Rework and Repair. IPC-sponsored certification gives your company a competitive advantage and your workforce valuable recognition.

For more information on these programs:

tel: 847-597-2814

fax: 847-615-7105

e-mail: certification@ipc.org

www.ipc.org/certification

Designer Certification (C.I.D.)/Advanced Designer Certification (C.I.D.+)

Contact:

tel: 847-597-2827

fax: 847-615-5627

e-mail: christipoulsen@ipc.org

<http://dc.ipc.org>

EMS Program Manager Certification

Contact:

tel: 847-597-2884

fax: 847-615-5684

e-mail: susanfilz@ipc.org

www.ipc.org/certification

IPC Video Tapes and CD-ROMs

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness. Members receive discounts on purchases.

For more information on IPC Video/CD Training, contact Mark Pritchard

tel: 505/758-7937 ext. 202

fax: 505/758-7938

e-mail: markp@ipcvideo.org

<http://training.ipc.org>

IPC Printed Circuits Expo, APEX and the Designers Summit



This yearly event is the largest electronics interconnection event in North America. With technical paper presentations, educational courses, standards development meetings networking opportunities and designers certification, there's something for everyone in the industry. The premier technical conference draws experts from around the globe. 500 exhibitors and 6,000 attendees typically participate each year. You'll see the latest in technologies, products and services and hear about the trends that affect us all. Go to www.GoIPCShows.org or contact shows@ipc.org for more information.

Exhibitor information:

Mary Mac Kinnon

Alicia Balonek

Director, Show Sales

Director, Trade Show Operations

847-597-2886

847-597-2898

MaryMacKinnon@ipc.org

AliciaBalonek@ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:

Jeanette Ferdman, Membership Director

tel: 847-597-2809

fax: 847-597-7105

e-mail: JeanetteFerdman@ipc.org

www.ipc.org

Application for Site Membership

Thank you for your decision to join IPC members on the “Intelligent Path to Competitiveness”! IPC Membership is **site specific**, which means that IPC member benefits are available to all individuals employed at the site designated on the other side of this application.

To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category. *(Check one box only.)*

☐ Independent Printed Board Manufacturers

This facility manufactures and sells to other companies, printed wiring boards (PWBs) or other electronic interconnection products on the merchant market. What products do you make for sale?

- ☐ One-sided and two-sided rigid printed boards ☐ Multilayer printed boards ☐ Other interconnections
☐ Flexible printed boards

Name of Chief Executive Officer/President _____

☐ Independent Electronic Assembly EMSI Companies

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Name of Chief Executive Officer/President _____

☐ OEM—Manufacturers of any end product using PCB/PCAs or Captive Manufacturers of PCBs/PCAs

This facility purchases, uses and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line? _____

☐ Industry Suppliers

This facility supplies raw materials, machinery, equipment or services used in the manufacture or assembly of electronic interconnection products.

What products do you supply? _____

☐ Government Agencies/Academic Technical Liaisons

We are representatives of a government agency, university, college, technical institute who are directly concerned with design, research, and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)



Application for Site Membership

Site Information:

Company Name _____

Street Address _____

City _____ State _____ Zip/Postal Code _____ Country _____

Main Switchboard Phone No. _____ Main Fax _____

Name of Primary Contact _____

Title _____ Mail Stop _____

Phone _____ Fax _____ e-mail _____

Company e-mail address _____ W _____

Please Check One:

- ☐ \$1,000.00 Annual dues for Primary Site Membership (Twelve months of IPC membership begins from the time the application and payment are received)
- ☐ \$800.00 Annual dues for Additional Facility Membership: Additional membership for a site within an organization where another site is considered to be the primary IPC member.
- ☐ \$600.00** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than \$1,000,000.00. **Please provide proof of annual sales.
- ☐ \$250.00 Annual dues for Government Agency/not-for-profit organization

TMRC Membership ☐ Please send me information about membership in the Technology Market Research Council (TMRC)

Payment Information:

Enclosed is our check for \$ _____

Please bill my credit card: (circle one) MC AMEX VISA DINERS

Card No. _____ Exp date _____

Authorized Signature _____

Mail application with check or money order to:

IPC
3491 Eagle Way
Chicago, IL 60678-1349

Fax/Mail application with credit card payment to:

IPC
3000 Lakeside Drive, Suite 309 S
Bannockburn, IL 60015-1249
Tel: 847-615-7100
Fax: 847-615-7105
<http://www.ipc.org>

Please attach business card
of primary contact here



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

Standard Improvement Form

IPC-7525A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249
Fax 847 615.7105
E-mail: answers@ipc.org

1. I recommend changes to the following:

___ Requirement, paragraph number _____
___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error
___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name

Telephone

Company

E-mail

Address

City/State/Zip

Date



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1249
Tel. 847.615.7100 Fax 847.615.7105
www.ipc.org