ภาคผนวก

• LS TTL Logic •
• CMOS Logic •

LS TTL Logic	
1.	74LS00
2.	74LS01
3.	74LS02
4.	74LS04
5.	74LS05
6.	74LS08
7.	74LS13
8.	74LS14
9.	74LS32
10.	74LS42
11.	74LS47
12.	74LS48
13.	74LS74A
14.	74LS75
15.	74LS77

LS TTL Logic	
16.	74LS76A
17.	74LS83A
18.	74LS85
19.	74LS90
20.	74LS92
21.	74LS93
22.	74LS122
23.	74LS123
24.	74LS125A
25.	74LS126A
26.	74LS147
27.	74LS148
28.	74LS748
29.	74LS153
30.	74LS155
31.	74LS156

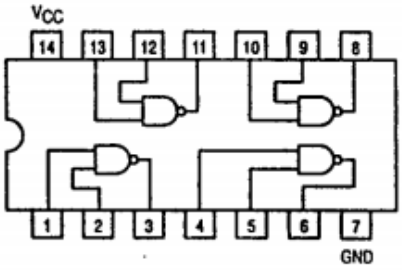
CMOS Logic	
1.	4001B
2.	4002B
3.	4025B
4.	4078B
5.	4009UB
6.	4010B
7.	4011B
8.	4012B
9.	4023B
10.	4068B
11.	4011UB
12.	4049UB
13.	4050B
14.	4070B
15.	4071B
16.	4072B
17.	4075B

หมายเหตุ ข้อมูลจากผลิตภัณฑ์ของ MOTOROLA

QUAD 2-INPUT NAND GATE

SN54/74LS00

QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

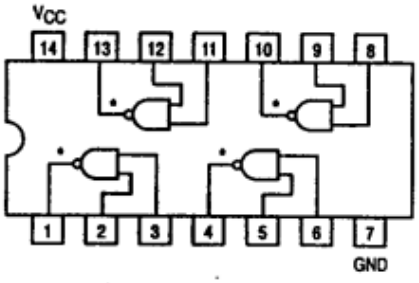
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

QUAD 2-INPUT NAND GATE

SN54/74LS01

QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

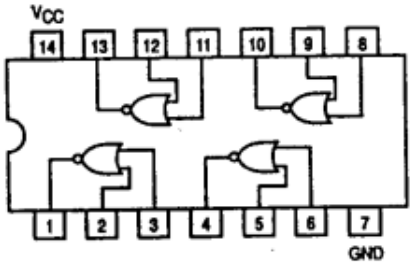
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

QUAD 2-INPUT NOR GATE

SN54/74LS02

QUAD 2-INPUT NOR GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

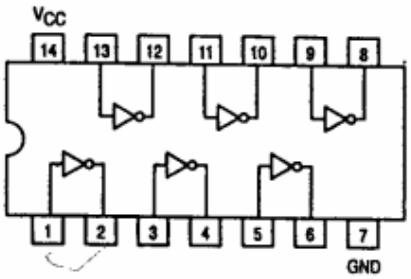
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

HEX INVERTER

SN54/74LS04

HEX INVERTER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

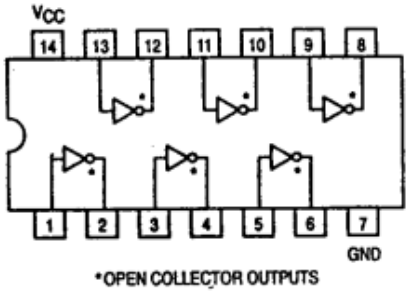
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

HEX INVERTER

SN54/74LS05

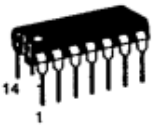
HEX INVERTER

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

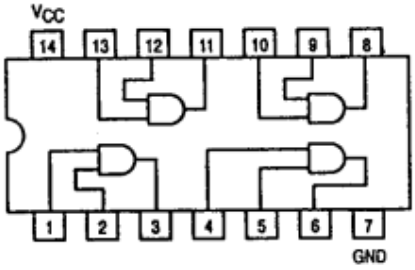
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

QUAD 2-INPUT AND GATE

SN54/74LS08



QUAD 2-INPUT AND GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

SCHMITT TRIGGERS
DUAL GATE/HEX INVERTER

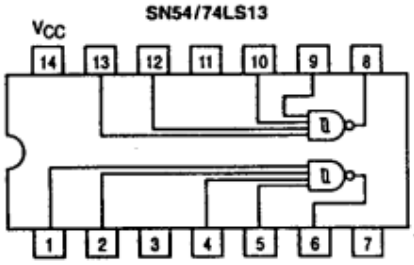
SN54/74LS13
SN54/74LS14

SCHMITT TRIGGERS
DUAL GATE/HEX INVERTER

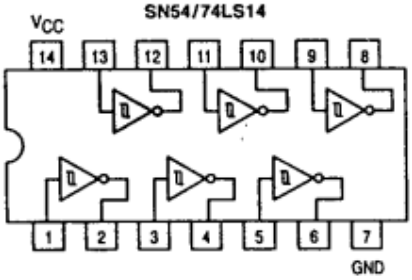
LOW POWER SCHOTTKY

LOGIC AND CONNECTION DIAGRAMS

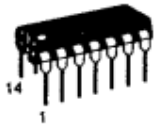
SN54/74LS13



SN54/74LS14



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

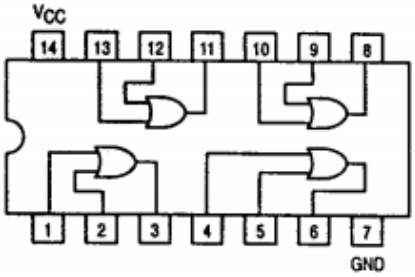
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

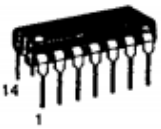
QUAD 2-INPUT OR GATE

SN54/74LS32

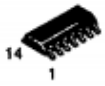
QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

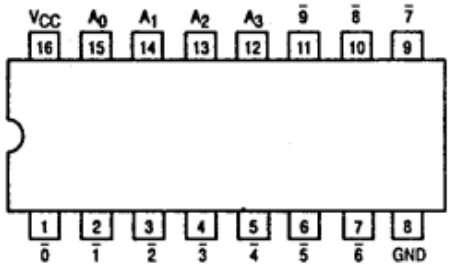
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

ONE-OF-TEN DECODER

The LSTTL/MSI SN54/74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Mutually Exclusive Outputs
- Demultiplexing Capability
- Input Clamp Diodes Limit High Speed Termination Effects

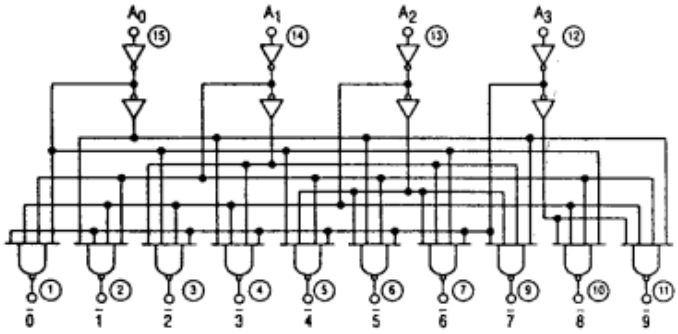
CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS42

ONE-OF-TEN DECODER
LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

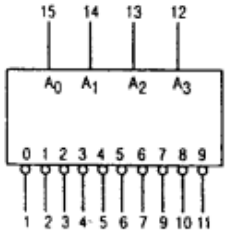
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

The SN54/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

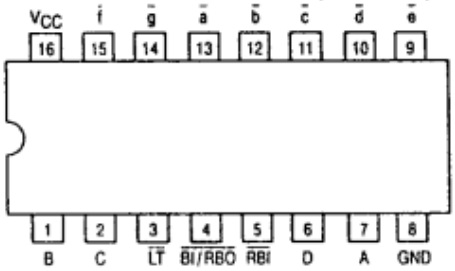
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 µA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

		LOADING (Note a) HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple-Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp-Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple-Blanking Output	1.2 U.L.	2.0 U.L.
$\overline{a}$ to $\overline{g}$	Outputs	Open-Collector	15 (7.5) U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 µA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

BCD TO 7-SEGMENT DECODER/DRIVER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

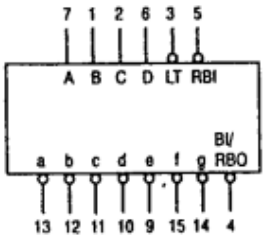
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

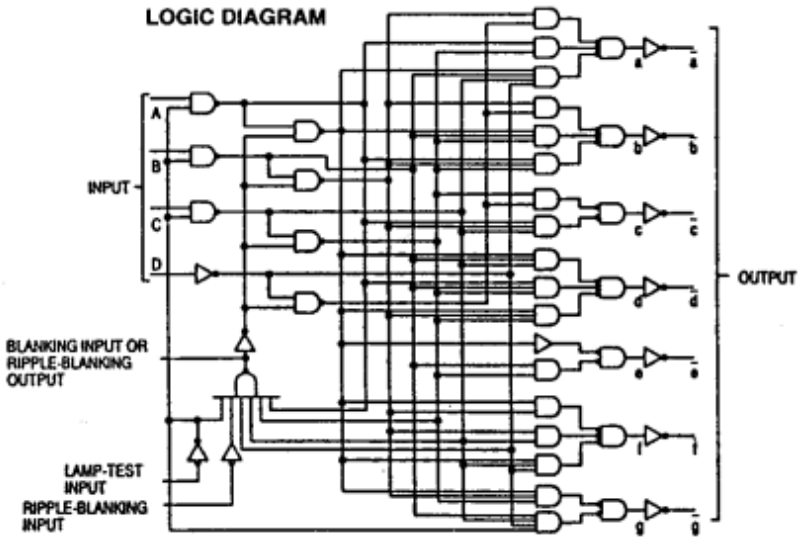
LOGIC SYMBOL

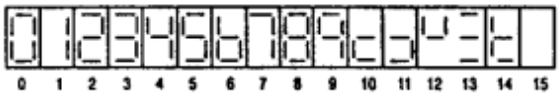


V_{CC} = PIN 16
GND = PIN 8

SN54/74LS47

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

SN54/74LS48

BCD TO 7-SEGMENT DECODER

BCD TO 7-SEGMENT DECODER

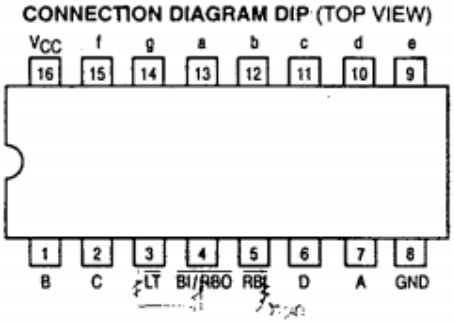
LOW POWER SCHOTTKY

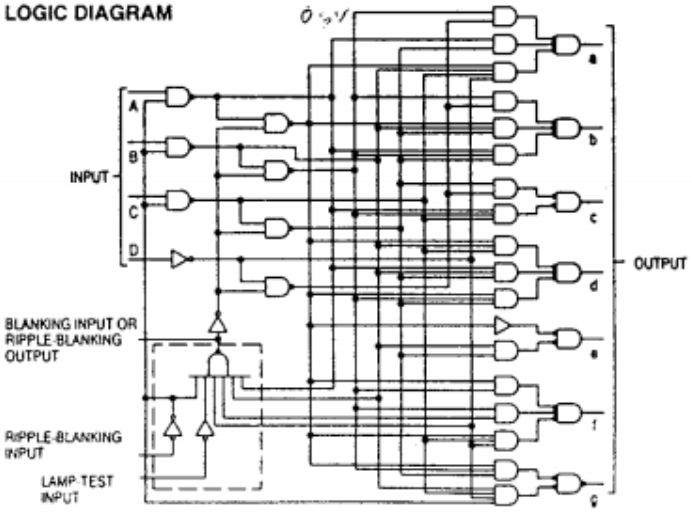
The SN54/74LS48 is a BCD to 7-Segment Decoder consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48.

The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Internal Pull-Ups Eliminate Need for External Resistors
- Input Clamp Diodes Eliminate High-Speed Termination Effects





J SUFFIX
CERAMIC
CASE 620-09

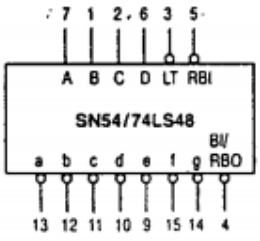
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



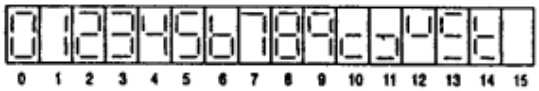
V_{CC} = PIN 16
GND = PIN 8

SN54/74LS48

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple-Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp-Test (Active Low) Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or Ripple-Blanking Output (Active Low)	0.5 U.L. 1.2 U.L.	0.75 U.L. 2(1) U.L.
$\overline{BI}$	Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
		Open-Collector	3.75 (1.25) U.L. (48)

NOTES:
a) Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW
b) Outut current measured at V_{OUT} = 0.5 V
Output LOW drive factor is SN54LS/74LS48: 1.25 U.L. for Military (54), 3.75 U.L. for Commercial (74).



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE
SN54/74LS48

	INPUTS						OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:
(1) $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.
(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
(3) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).
(4) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

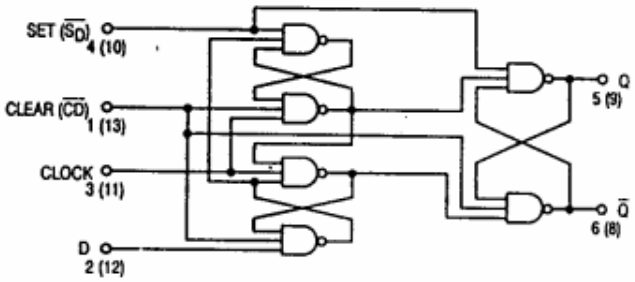
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

SN54/74LS74A

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S_D}$	$\overline{S_D}$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

J SUFFIX
CERAMIC
CASE 632-08

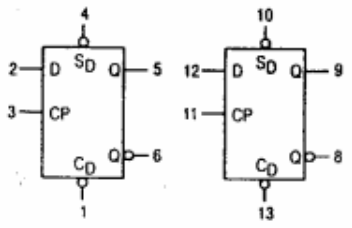
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



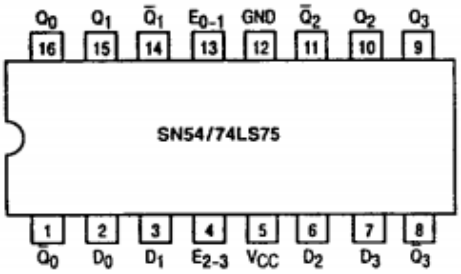
V_{CC} = PIN 14
GND = PIN 7

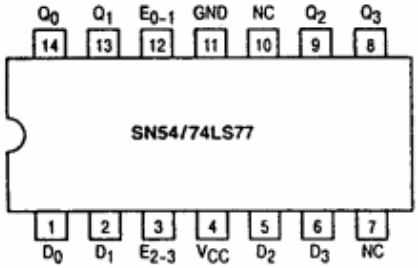
4-BIT D LATCH

The TTL/MSI SN54/74LS75 and SN54/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54/74LS77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

CONNECTION DIAGRAMS DIP (TOP VIEW)





PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_1$–$\overline{Q}_4$	Complimentary Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

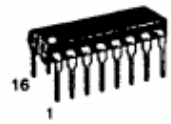
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

SN54/74LS75
SN54/74LS77

4-BIT D LATCH
LOW POWER SCHOTTKY

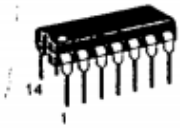
J SUFFIX
CERAMIC
CASE 620-09



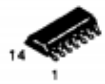
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

DUAL JK FLIP-FLOP WITH SET AND CLEAR

SN54/74LS76A

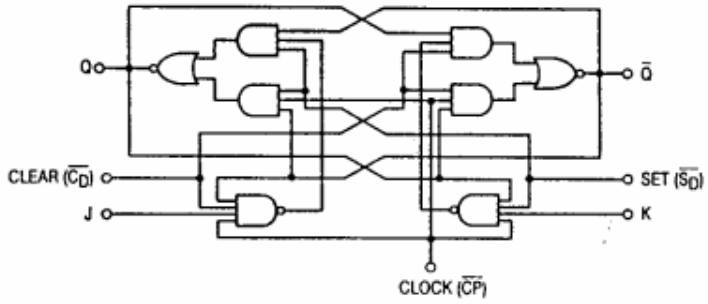
DUAL JK FLIP-FLOP WITH SET AND CLEAR

LOW POWER SCHOTTKY

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 620-09

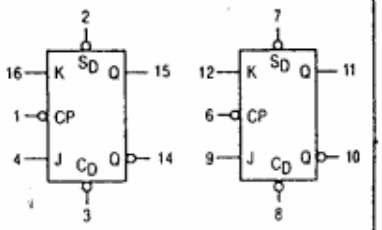
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 5
GND = PIN 13

4-BIT BINARY FULL ADDER WITH FAST CARRY

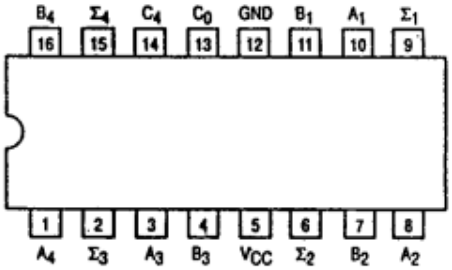
SN54/74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

CONNECTION DIAGRAM DIP (TOP VIEW)

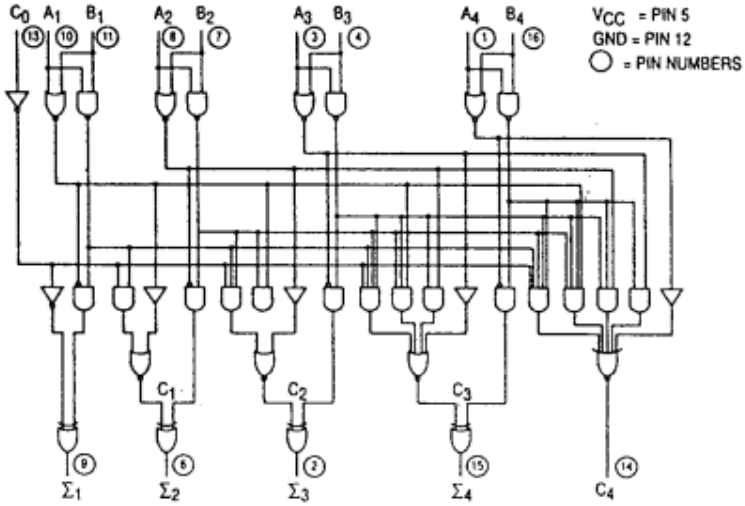


PIN NAMES

		LOADING (Note a) HIGH	LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

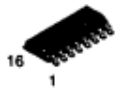
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

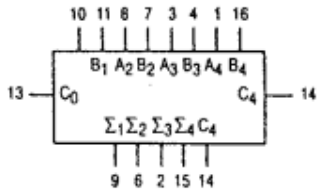


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

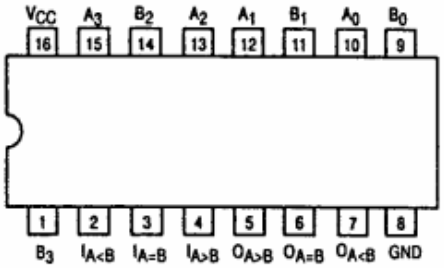
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



4-BIT MAGNITUDE COMPARATOR

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES		LOADING (Note a)	
		HIGH	LOW
A_0-A_3, B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS85

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

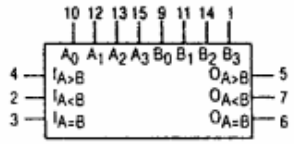
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

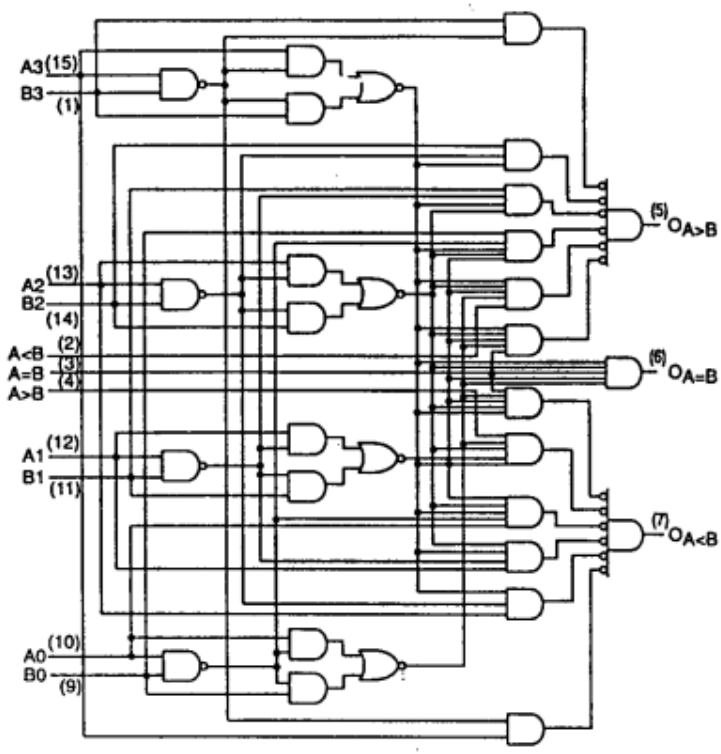
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS85

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER

LOW POWER SCHOTTKY

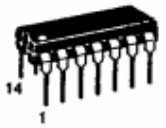
The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to +2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to +5 Section (LS90), +6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to +8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from +2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from +5 (LS90), +6 (LS92), +8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

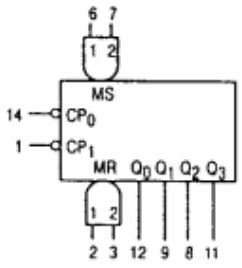
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

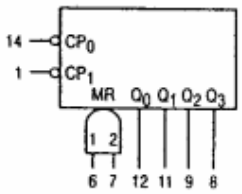
LOGIC SYMBOL

LS90



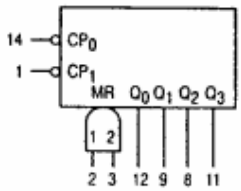
V_{CC} = PIN 5
GND = PIN 10
NC = PINS 4, 13

LS92



V_{CC} = PIN 5
GND = PIN 10
NC = PINS 2, 3, 4, 13

LS93

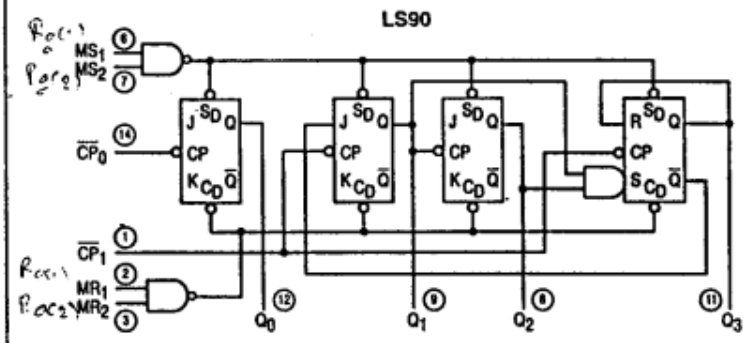


V_{CC} = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

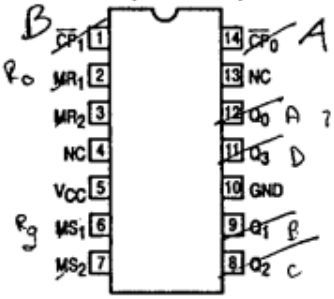
LOGIC DIAGRAM

LS90



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

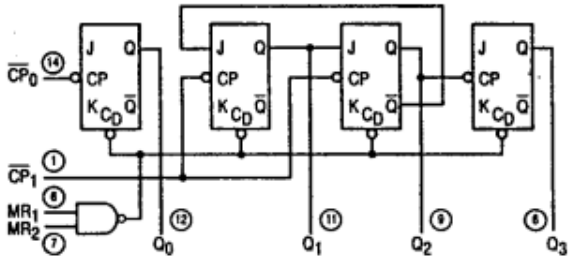


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

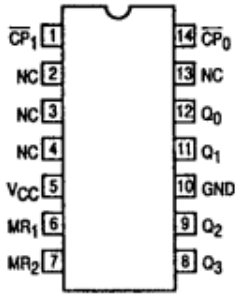
LOGIC DIAGRAM

LS92



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

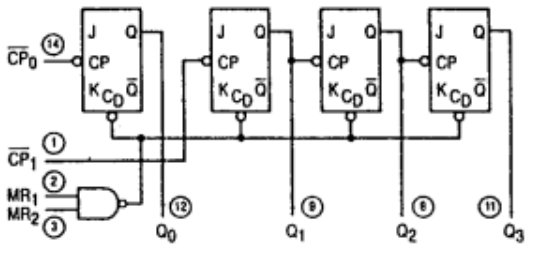


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

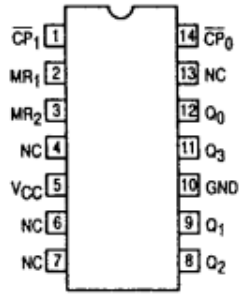
LOGIC DIAGRAM

LS93



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$ for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$.

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SN54/74LS122
SN54/74LS123

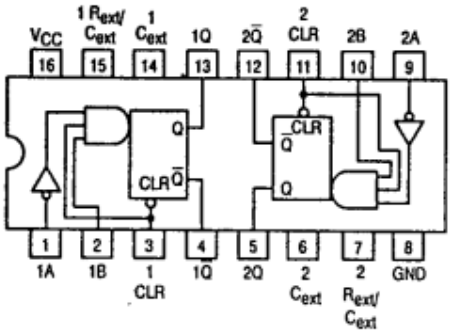
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

LOW POWER SCHOTTKY

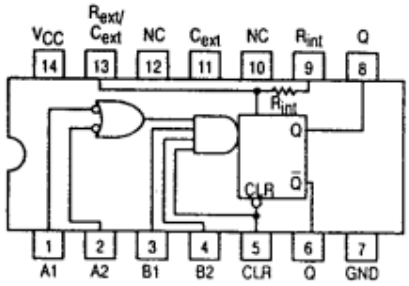
These dc triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- DC Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Internal Timing Resistors on LS122

SN54/74LS123 (TOP VIEW)
(SEE NOTES 1 THRU 4)



SN54/74LS122 (TOP VIEW)
(SEE NOTES 1 THRU 4)



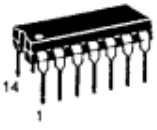
NC — NO INTERNAL CONNECTION.

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS122 • SN54/74LS123

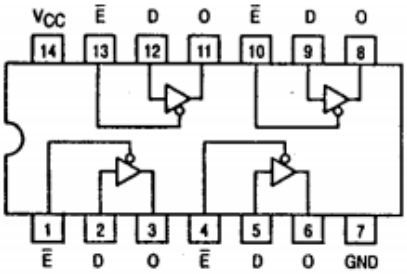
LS122
FUNCTIONAL TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

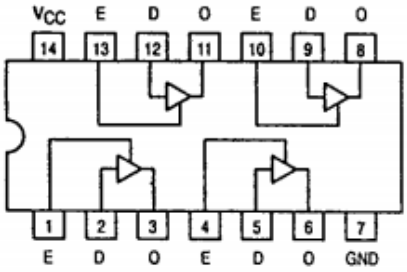
LS123
FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

QUAD 3-STATE BUFFERS



LS125A



LS126A

TRUTH TABLES

LS125A

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	L
L	H	H
H	X	(Z)

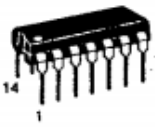
LS126A

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

SN54/74LS125A
SN54/74LS126A

QUAD 3-STATE BUFFERS
LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

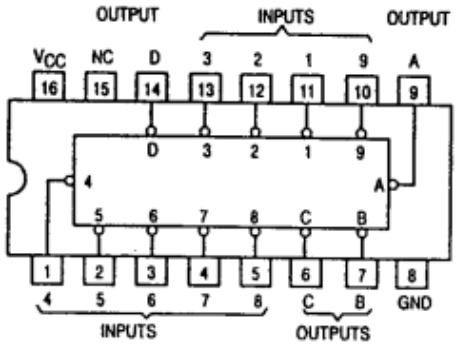
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

GUARANTEED OPERATING RANGES

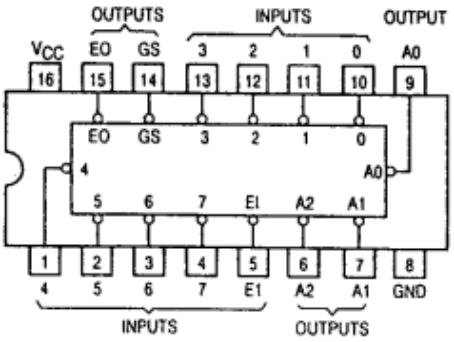
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

SN54/74LS147
(TOP VIEW)



SN54/74LS148
SN54/74LS748
(TOP VIEW)

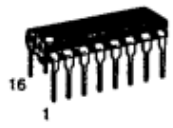


SN54/74LS147
SN54/74LS148
SN54/74LS748

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

SN54/74LS147
FUNCTION TABLE

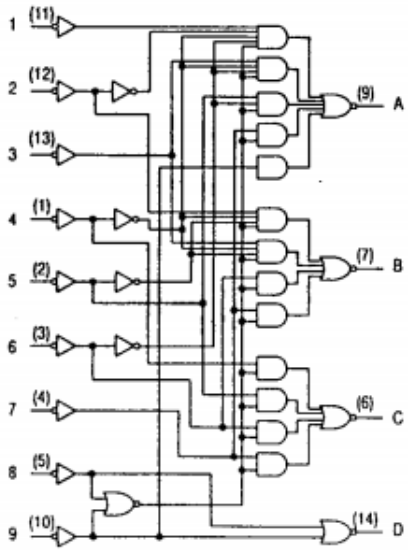
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

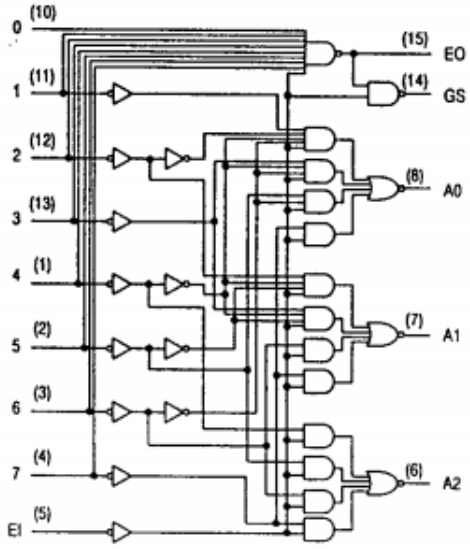
SN54/74LS148
SN54/74LS748
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

FUNCTIONAL BLOCK DIAGRAMS



SN54/74LS147



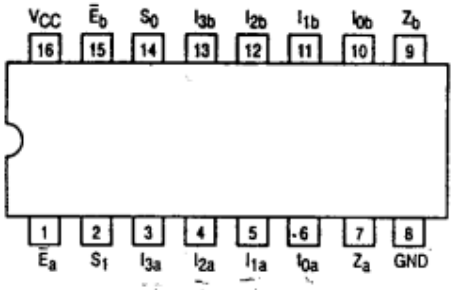
SN54/74LS148

DUAL 4-INPUT MULTIPLEXER

The LSTTL/MSI SN54/74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Non-Inverting Outputs
- Separate Enable for Each Multiplexer
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

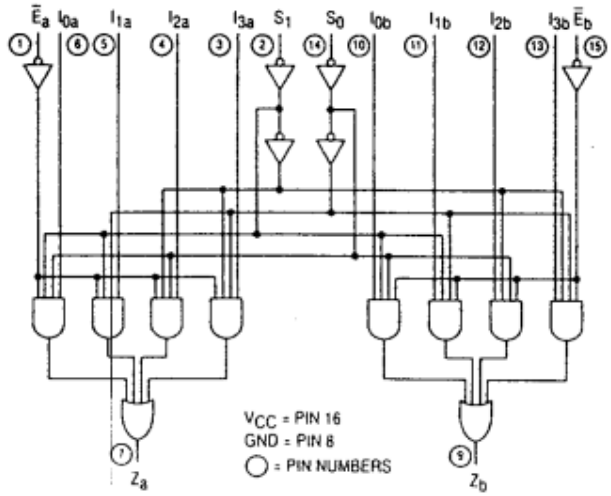


PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



SN54/74LS153

DUAL 4-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

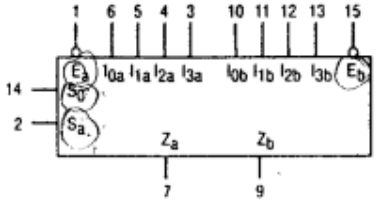
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

SN54/74LS155
SN54/74LS156

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

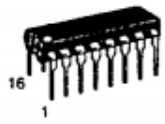
LS156-OPEN-COLLECTOR LOW POWER SCHOTTKY

The SN54/74LS155 and SN54/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

J SUFFIX
CERAMIC
CASE 620-09



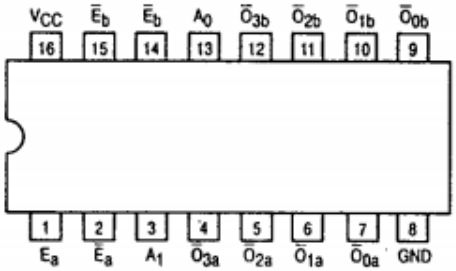
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

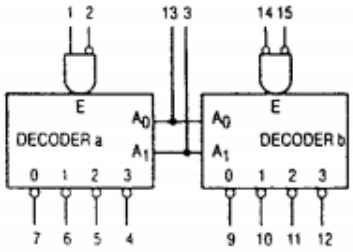


PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a$, $\overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

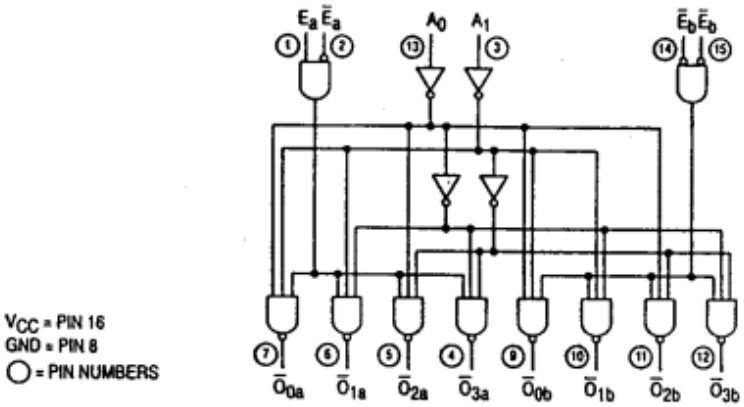
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS155 • SN54/74LS156

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

TRUTH TABLE

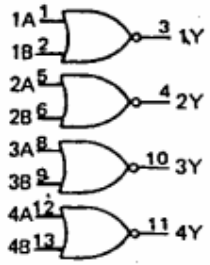
ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

CMOS NOR GATES

SCL4001B – Quad 2-Input NOR
SCL4002B – Dual 4-Input NOR
SCL4025B – Triple 3-Input NOR
SCL4078B – 8-Input NOR

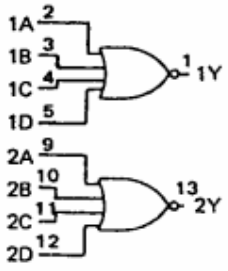
FUNCTION DIAGRAMS

SCL4001B



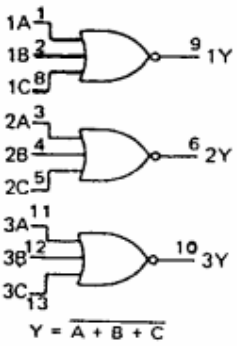
$Y = \overline{A + B}$

SCL4002B



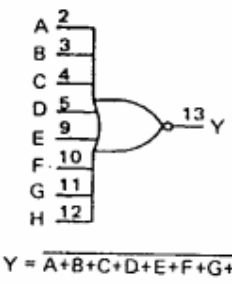
$Y = \overline{A + B + C + D}$

SCL4025B



$Y = \overline{A + B + C}$

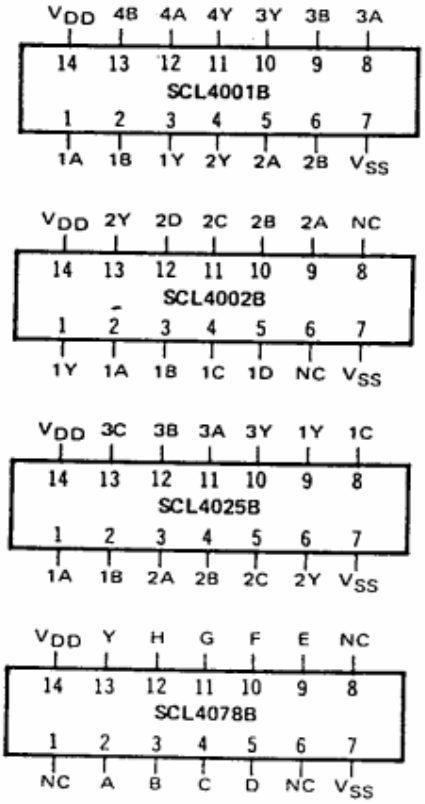
SCL4078B



$Y = \overline{A+B+C+D+E+F+G+H}$

V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

CONNECTION DIAGRAMS
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

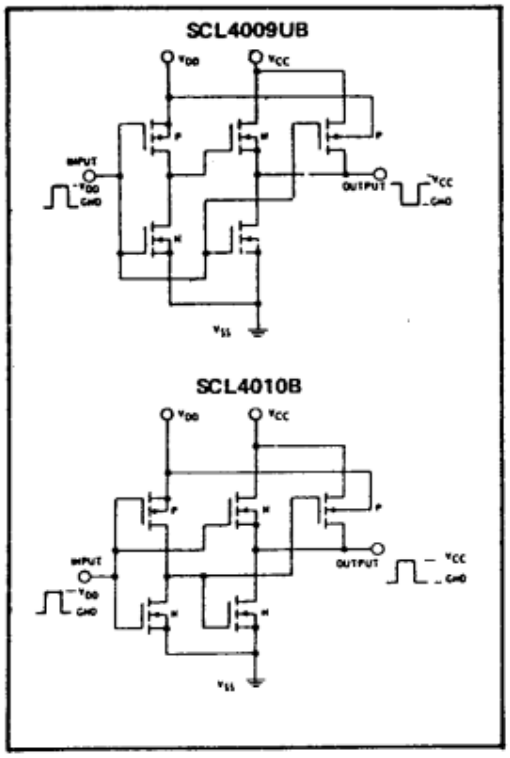
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

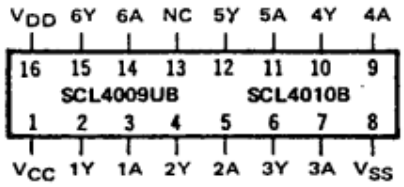
CMOS
HEX BUFFERS/CONVERTERS

SCL4009UB Inverting
SCL4010B Non-Inverting

SCHEMATIC DIAGRAMS



CONNECTION DIAGRAM
(all packages)



Add Suffix for Package:

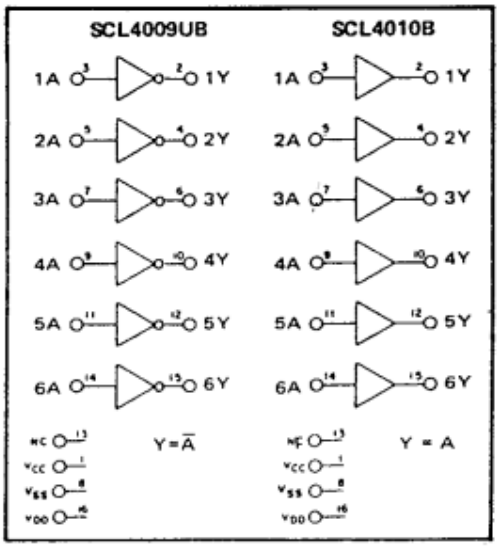
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
	$V_{CC} - V_{SS}$	3 to 15	Vdc
	$V_{CC} \leqslant V_{DD}$		
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

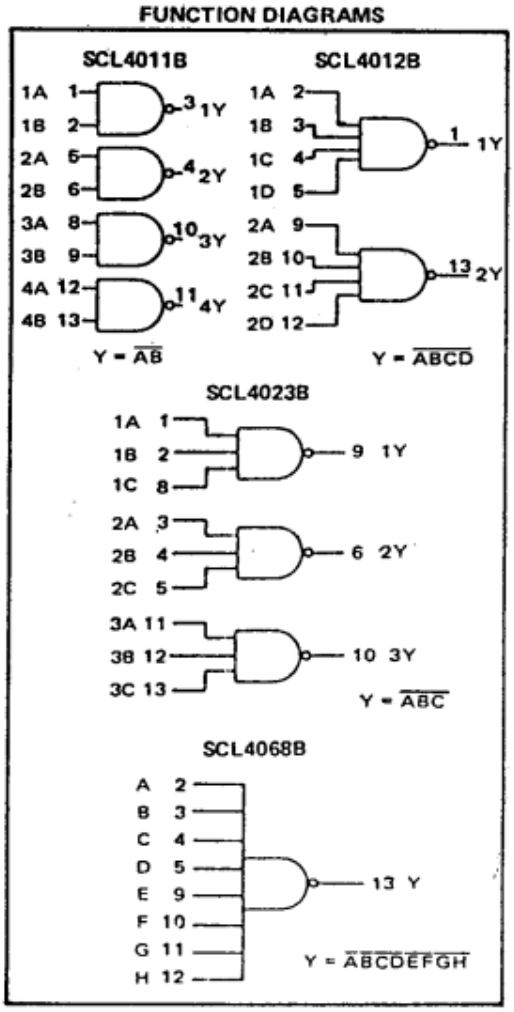
LOGIC DIAGRAMS



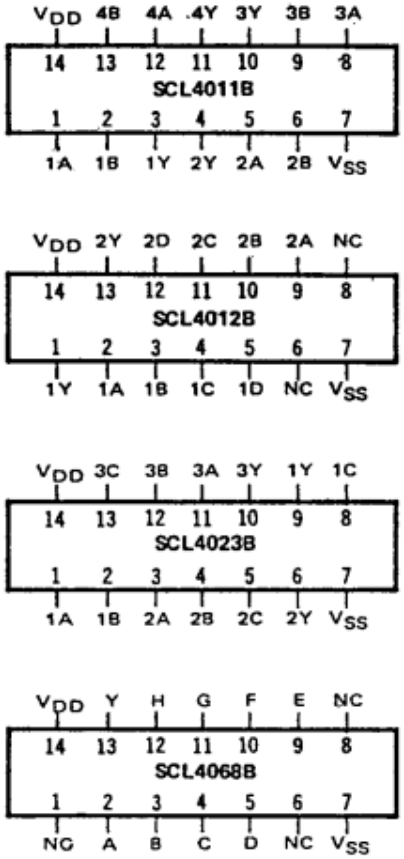
CMOS NAND GATES

SCL4011B – Quad 2-Input NAND
SCL4012B – Dual 4-Input NAND
SCL4023B – Triple 3-Input NAND
SCL4068B – 8-Input NAND

FUNCTION DIAGRAMS



CONNECTION DJAGRAMS
(all packages)



Add suffix to package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

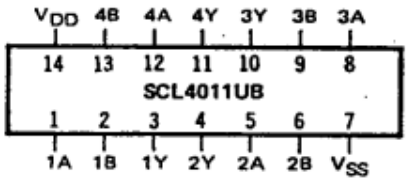
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

CMOS NAND GATE
(Unbuffered)

SCL4011UB

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

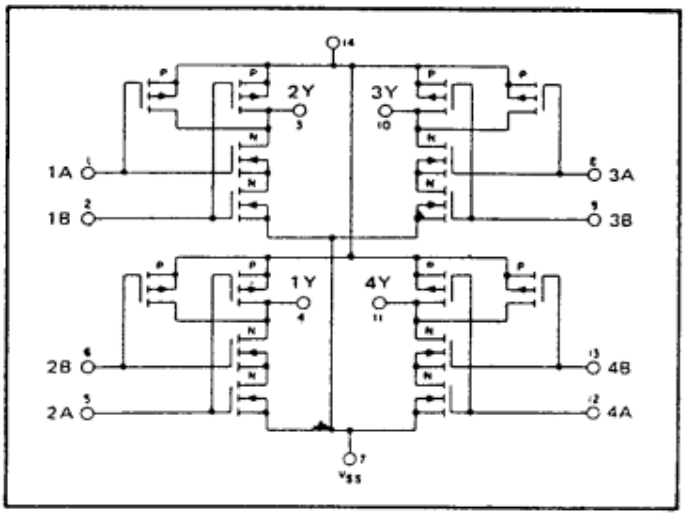
C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

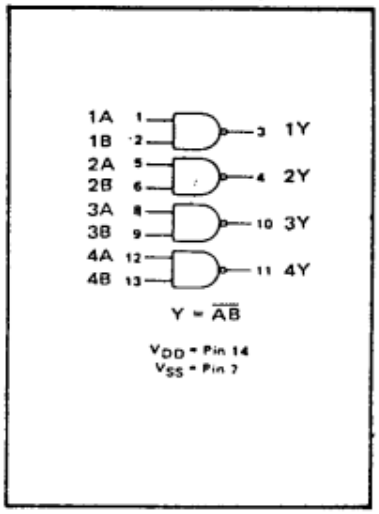
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



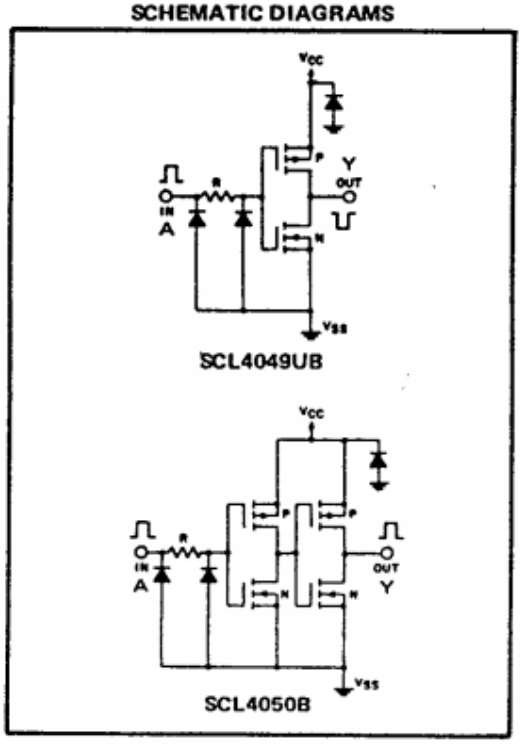
LOGIC DIAGRAM



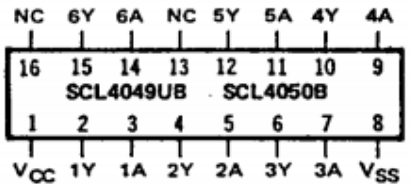
CMOS
HEX BUFFERS/CONVERTERS

SCL4049UB Inverting
SCL4050B Non-Inverting

SCHEMATIC DIAGRAMS



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

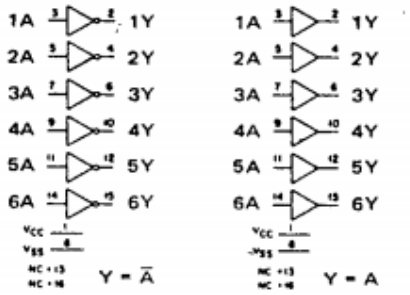
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{CC} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: These devices contain input protection networks to V_{SS} only. Therefore, V_{IH} (max) may exceed V_{CC} without damage (subject to absolute maximum ratings).

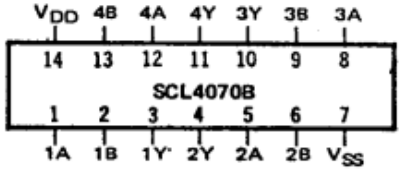
LOGIC DIAGRAMS



CMOS
QUAD EXCLUSIVE-OR GATE

SCL4070B

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

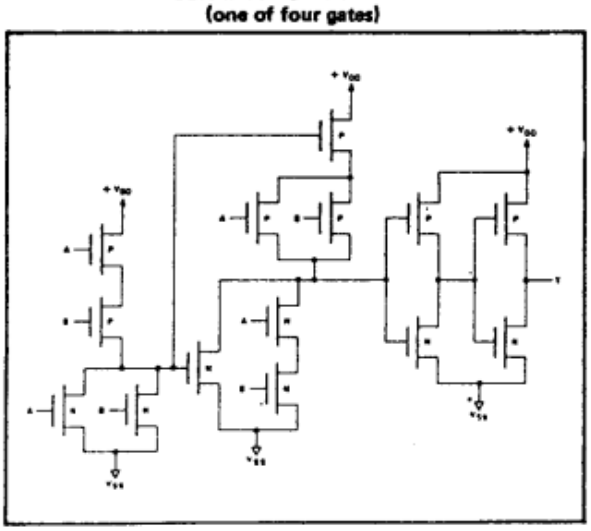
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

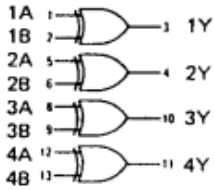
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: The SCL4070B is identical to the SCL4030B; the devices are fully interchangeable in all applications.

SCHEMATIC DIAGRAM
(one of four gates)



FUNCTION DIAGRAM



$Y = A \oplus B$

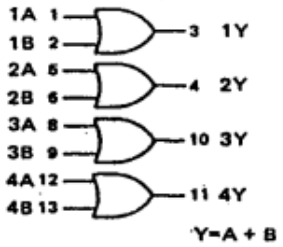
V_{DD} = Pin 14
V_{SS} = Pin 7

CMOS OR GATES

SCL4071B - Quad 2-Input OR
SCL4072B - Dual 4-Input OR
SCL4075B - Triple 3-Input OR

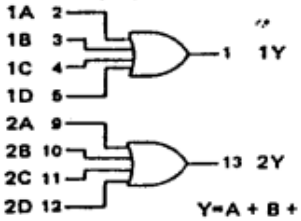
FUNCTION DIAGRAMS

SCL4071B



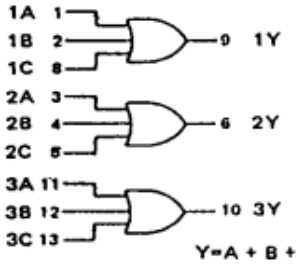
Y=A + B

SCL4072B



Y=A + B + C + D

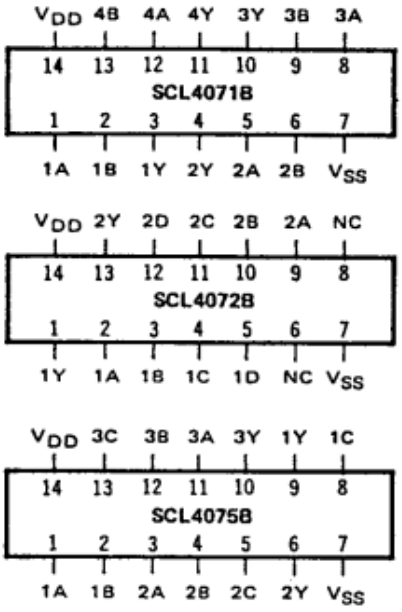
SCL4075B



Y=A + B + C

V_{DD} = Pin 14
V_{SS} = Pin 7
for all Devices

CONNECTION DIAGRAMS
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C